MIC4223/MIC4224/MIC4225

Dual 4A, 4.5V to 18V, 15ns Switch Time, Low-Side MOSFET Drivers with Enable

General Description

The MIC4223/MIC4224/MIC4225 are a family of a dual 4A, High-Speed, Low-side MOSFET drivers with logic-level driver enables. The devices are fabricated on Micrel's Bipolar/CMOS/DMOS (BCD) process and operate from a 4.5V to 18V supply voltage. The devices parallel Bipolar and CMOS output stage architecture provides high-current throughout the MOSFETs Miller Region allowing the driver to sink and source 4A of peak current from a 12V supply and quickly charge and discharge a 2000pF load capacitance in under 15ns, while allowing the outputs to swing within 0.3V of V_{DD} and 0.16V of ground.

The MIC4223/MIC4224/MIC4225 driver and enable inputs feature TTL and CMOS logic-level thresholds which are independent of supply voltage. Each driver features a dedicated active-high enable input which is internally pulled high to V_{DD} through 100kΩ, allowing the pins to be left unconnected if it is not required to disable the driver outputs. The driver inputs have been designed to protect against ground bounce and are protected to withstand -5V of voltage swing at -40mA. Driver outputs are also protected to withstand 500mA of reverse current.

The MIC4223/MIC4224/MIC4225 are available in three configurations using industry standard pin out; dual inverting (MIC4223), dual non-inverting (MIC4224) and complimentary (MIC4225). They are available in 8-pin SOIC and thermally enhanced e-PAD 8-pin MSOP and support operating junction temperatures from -40°C to +125°C.

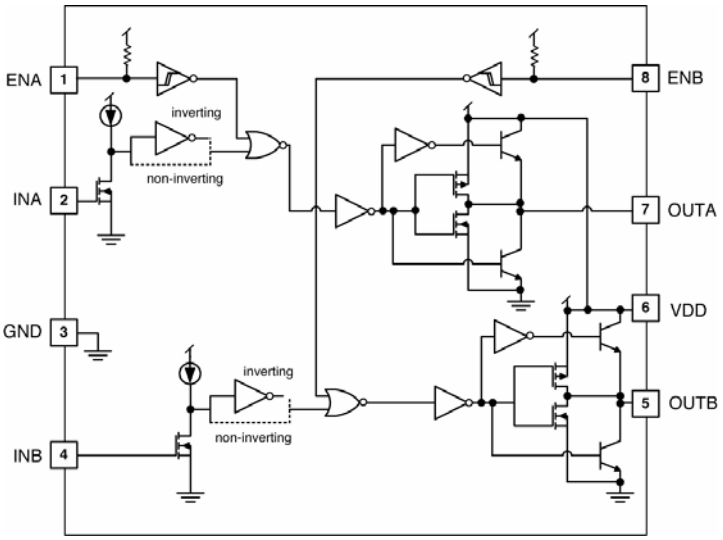
Applications

- High-Efficiency MOSFET switching
- Switch mode power supplies
- DC-to-DC converters
- Motor and solenoid drivers
- Clock and line drivers
- Synchronous rectifiers
- Pulse transformer drive
- Class D switching amplifiers

Features

- 4.5V to 18V supply voltage operating range
- High peak source/sink current
  - ±3A at V_{DD} = 8V
  - ±4A at V_{DD} = 12V
- 15ns/15ns Rise and Fall times with 2000pF load
- 25ns/35ns (Rising/Falling) input propagation delay
- 20ns/45ns (Rising/Falling) enable propagation delay
- Active-high driver enable inputs with 100kΩ pull-ups
- CMOS and TTL logic input and enable thresholds independent of supply voltage
- Driver input protection to -5V at -40mA
- Output Latch-up protection to >500mA reverse current
- Industry standard pin out with two package options
  - ePAD MSOP-8 (θ_{JA} = 60°C/W)
  - 8-pin SOIC (θ_{JA} = 120°C/W)
- Available in dual-inverting (MIC4223), dual non-inverting (MIC4224) and complementary (MIC4225)
- Dual output drive by paralleling channels
- -40°C to +125°C operating junction temperature range

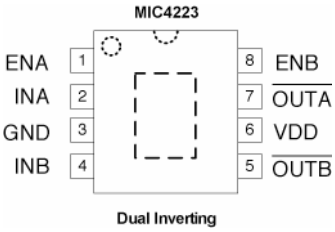
Block Diagram



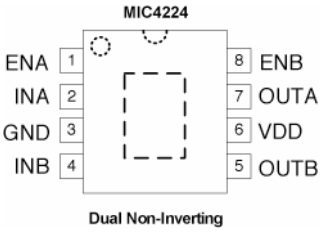
Ordering Information

Part Number	Configuration	Junction Temp. Range	Package	Lead Finish
MIC4223YM	Dual Inverting	–40° to +125°C	8-pin SOIC	Pb-Free
MIC4223YMME	Dual Inverting	–40° to +125°C	8-pin EPAD-MSOP	Pb-Free
MIC4224YM	Dual Non-inverting	–40° to +125°C	8-pin SOIC	Pb-Free
MIC4224YMME	Dual Non-inverting	–40° to +125°C	8-pin EPAD-MSOP	Pb-Free
MIC4225YM	Inverting + Non-inverting	–40° to +125°C	8-pin SOIC	Pb-Free
MIC4225YMME	Inverting + Non-inverting	–40° to +125°C	8-pin EPAD-MSOP	Pb-Free

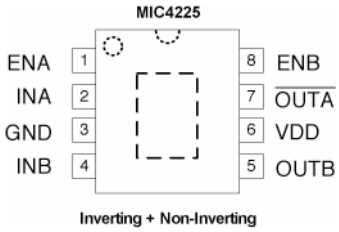
Pin Configuration



8-Pin SOIC (YM)
8-Pin ePAD MSOP (YMME)



8-Pin SOIC (YM)
8-Pin ePAD MSOP (YMME)



8-Pin SOIC (YM)
8-Pin ePAD-MSOP (YMME)

Pin Description

Pin Number	Pin Name	Pin Function
1	ENA	Enable pin for output A. TTL/CMOS-compatible logic input. A logic-level high enables the device. An internal pull-up enables the part if pin is open. A logic-level low disables the device and the output will be low regardless of the input state.
2	INA	Control Input A: TTL/CMOS-compatible logic input. Connect to V_{DD} or ground if not used and connect ENA to ground to disable driver A.
3	GND	Ground
4	INB	Control Input B: TTL/CMOS compatible logic input. Connect to V_{DD} or ground if not used and connect ENB to ground to disable driver B.
5	OUTB	Output B: Parallel Bipolar/CMOS output.
6	VDD	Voltage Supply Input: +4.5V to +18V
7	OUTA	Output A: Parallel Bipolar/CMOS output.
8	ENB	Enable pin for output B. TTL/CMOS-compatible logic input. A logic-level high enables the device. An internal pull-up enables the part if pin is open. A logic-level low disables the device and the output will be low regardless of the input state.
EP	GND	Exposed thermal pad for ePad MSOP package only (Not available on SOIC-8L package). Connect to ground. Must make a full connection to the ground plane to maximize thermal performance of the package.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +20V
Input Voltage (V_{INA}, V_{INB}) ..... V_{DD} + 0.3V to GND - 5V
Enable Voltage (V_{ENA}, V_{ENB}) ..... 0.3V to V_{DD} + 0.3V
Junction Temperature (T_J) ..... -55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (10 sec.) ..... 300°C
ESD Rating ..... HBM = 2kV, MM = 200V[3]

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +4.5V to +18V
Junction Temperature (T_J) ..... –40°C to +125°C
Package Thermal Resistance
EPAD MSOP (θ_{JA}) ..... 60°C/W
SOIC (θ_{JA}) ..... 120°C/W

Electrical Characteristics

4.5V ≤ V_{DD} ≤ 18V; C_L = 2000pF. T_A = 25°C, bold values indicate full operating junction temperature range, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input						
V_{IH}	Logic 1 Input Voltage		**2.4**	2.2		V
V_{IL}	Logic 0 Input Voltage			1.95	**0.8**	V
Hysteresis				0.25		V
I_{IN}	Input Current	$0 \le V_{IN} \le V_{DD}$	–1 **–10**		1 **10**	µA µA
		V_{IN} = -5V		-40		mA
Output						
V_{OH}	High Output Voltage	I_{OUT} = -10mA, V_{DD} = 18V	**V_{DD} - 0.45**			V
V_{OL}	Low Output Voltage	I_{OUT} = 10mA, V_{DD} = 18V			**0.30**	V
RO	Output Resistance – Source Output Resistance – Sink	I_{OUT} = -10mA, V_{DD} = 18V I_{OUT} = 10mA, V_{DD} = 18V		30 16	**45** **30**	Ω
IPK	Peak Output Current	V_{DD} = 8V		±3		A
		V_{DD} = 12V		±4		
I	Latch-Up Protection	Withstand reverse current		>500		mA
Switching Time						
t_R	Rise Time	Test Figure 1; C_L = 2000pF		15	**40**	ns
t_F	Fall Time	Test Figure 1; C_L = 2000pF		15	**40**	ns
t_{D1}	Delay Time	Test Figure 1; C_L = 2000pF		25	**45**	ns
t_{D2}	Delay Time	Test Figure 1; C_L = 2000pF		35	**50**	ns
Enable (ENA, ENB)						
V_{EN_H}	High Level Enable Voltage	LO to HI transition	**2.4**	1.9		V
V_{EN_L}	Low Level Enable Voltage	HI to LO transition		1.55	**0.8**	V
Hysteresis				0.35		V
R_{EN}	Enable Impedance	V_{DD} = 18V, V_{ENA} = V_{ENB} = GND		100		kΩ
t_{D3}	Propagation Delay Time	C_L = 2000pF		20	**60**	ns
t_{D4}	Propagation Delay Time	C_L = 2000pF		45	**150**	ns
Power Supply						
I_{SH}	Power Supply Current	V_{INA} = V_{INB} = 3.0V, V_{ENA} = V_{ENB} = open		1.7	**2.5**	mA
I_{SL}	Power Supply Current	V_{INA} = V_{INB} = 0.0V, V_{ENA} = V_{ENB} = open		0.7	**1.5**	mA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.

Test Circuit

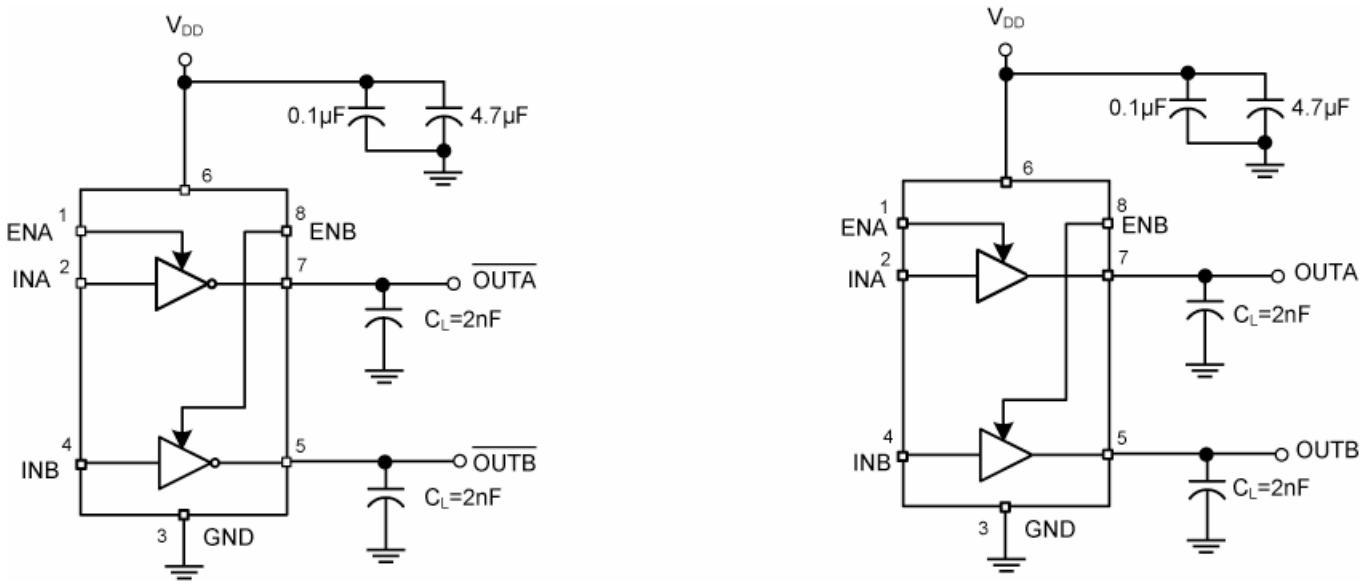
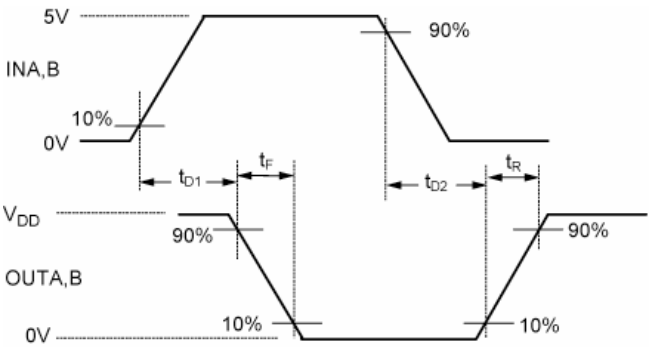
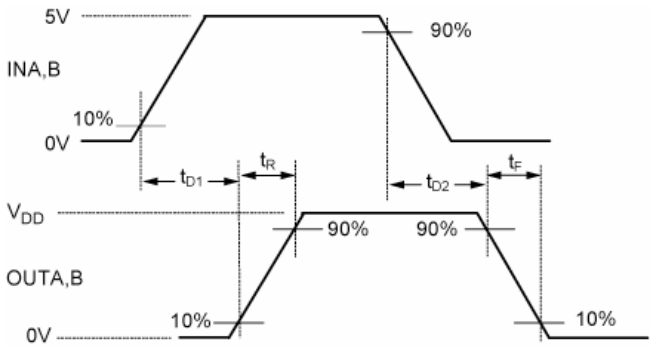


Figure 1. Test Circuit

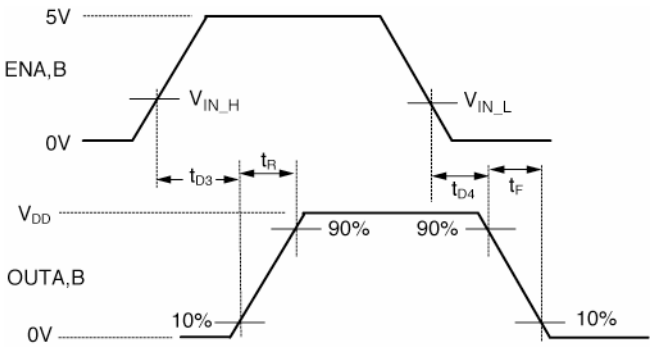
Timing Diagram



Inverting Driver



Non-Inverting Driver

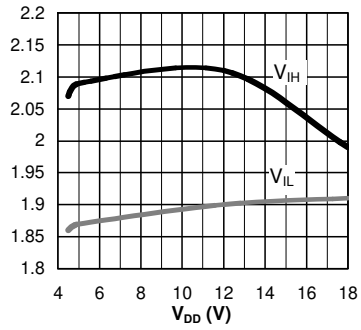


Enable to Output Timing Diagram

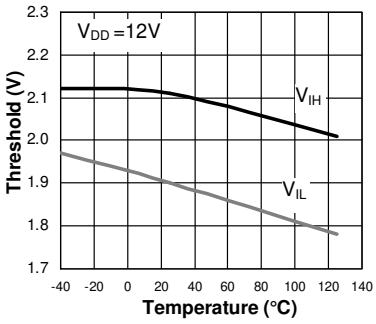
Typical Characteristics

Conditions: T_A =25ºC.

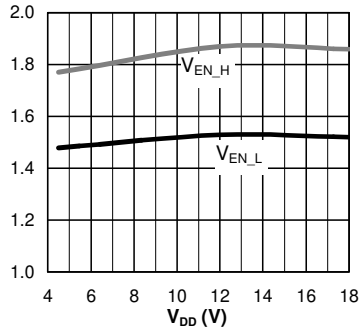
$V_{INA, B}$ Threshold vs. V_{DD}



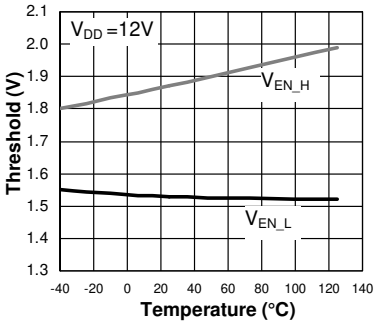
$V_{INA, B}$ Threshold vs. Temperature



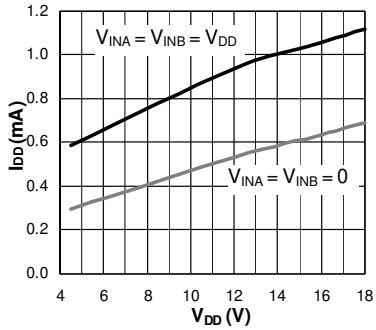
$V_{ENA, B}$ Threshold vs. V_{DD}



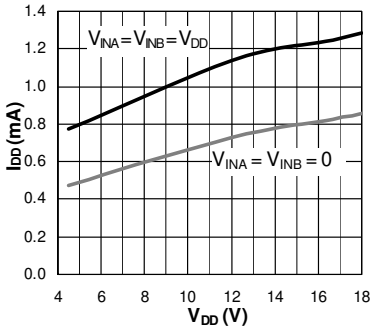
Enable Threshold vs. Temperature



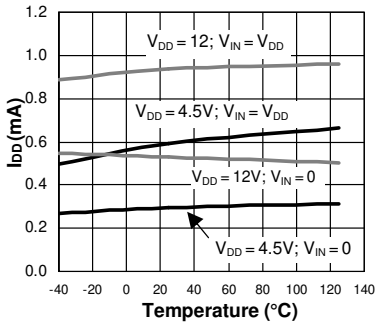
I_{DD} vs. V_{DD} (Disabled)



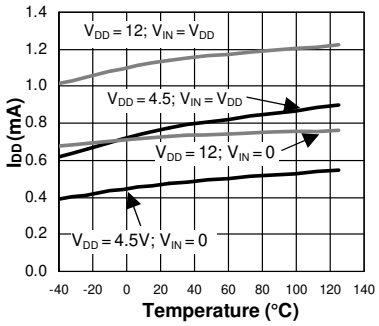
I_{DD} vs. V_{DD} (Enabled)



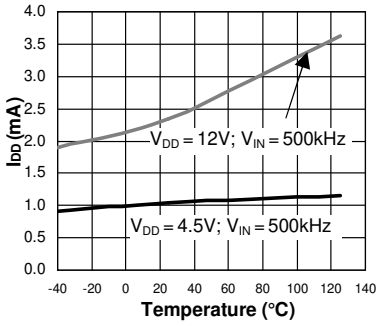
I_{DD} vs. Temperature (Disabled)



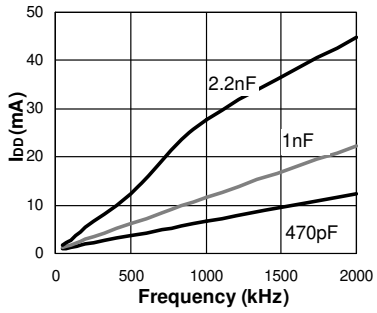
I_{DD} vs. Temperature (Enabled)



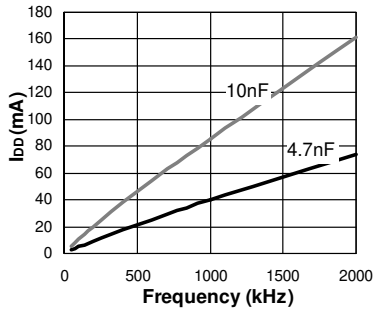
I_{DD} vs. Temperature (Switching)



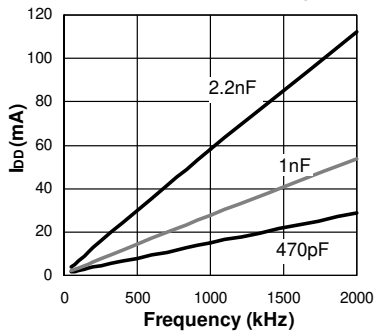
I_{DD} vs. Frequency (V_{DD} = 5V)
Both Drivers Switching



I_{DD} vs. Frequency (V_{DD} = 5V)
Both Drivers Switching

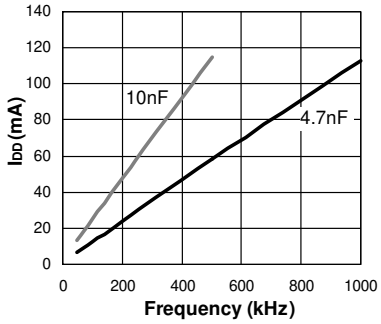


I_{DD} vs. Frequency (V_{DD} = 12V)
Both Drivers Switching

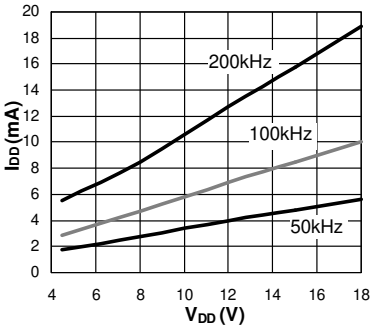


Conditions: T_A = 25ºC.

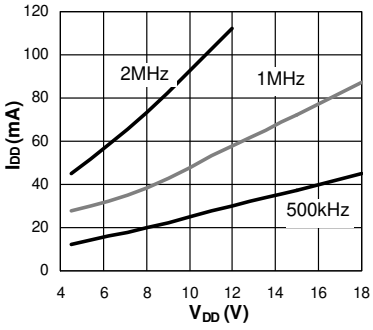
I_{DD} vs. Frequency (V_{DD} = 12V)
Both Drivers Switching



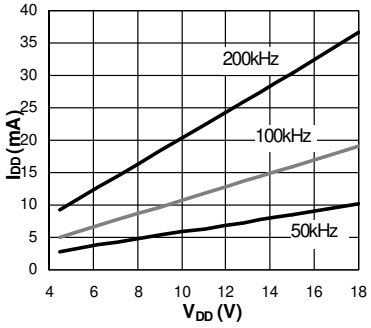
I_{DD} vs. V_{DD} (C_L = 2.2nF)
Both Drivers Switching



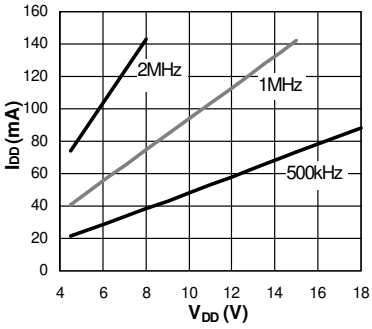
I_{DD} vs. V_{DD} (C_L = 2.2nF)
Both Drivers Switching



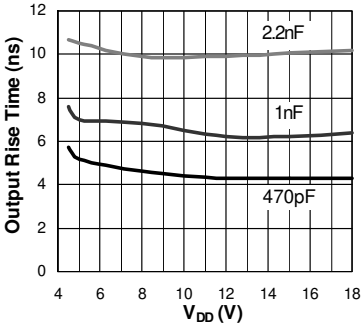
I_{DD} vs. V_{DD} (C_L = 4.7nF)
Both Drivers Switching



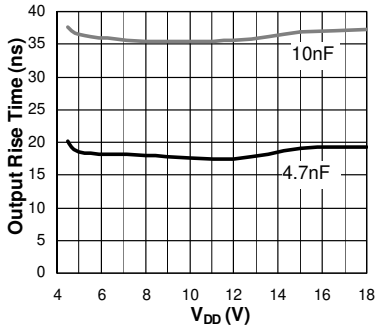
I_{DD} vs. V_{DD} (C_L = 4.7nF)
Both Drivers Switching



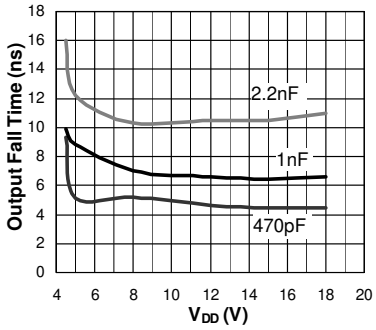
Output Rise Time vs. V_{DD}



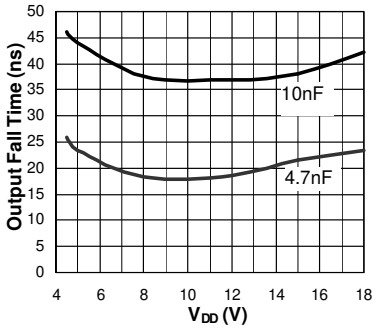
Output Rise Time vs. V_{DD}



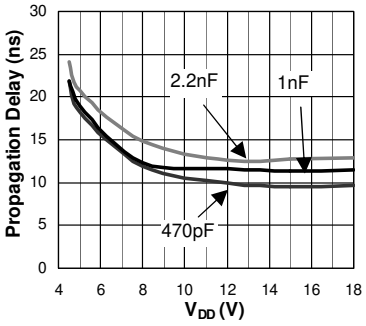
Output Fall Time vs. V_{DD}



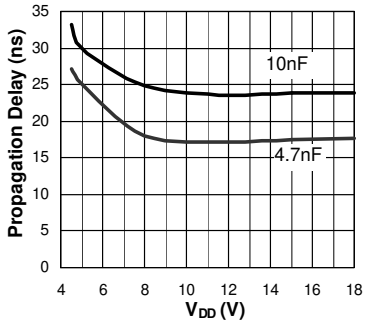
Output Fall Time vs. V_{DD}



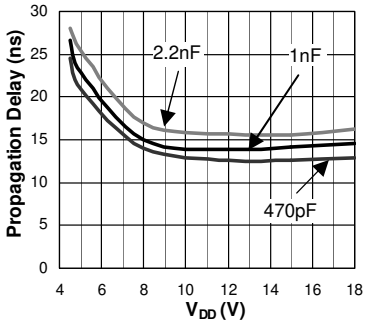
Propagation Delay (t_{D1}) vs. V_{DD}



Propagation Delay (t_{D1}) vs. V_{DD}

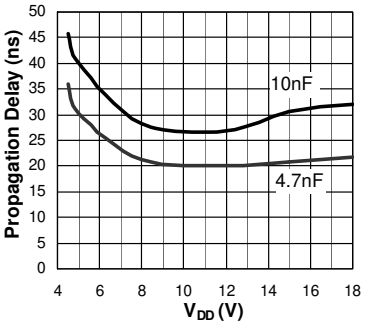


Propagation Delay (t_{D2}) vs. V_{DD}

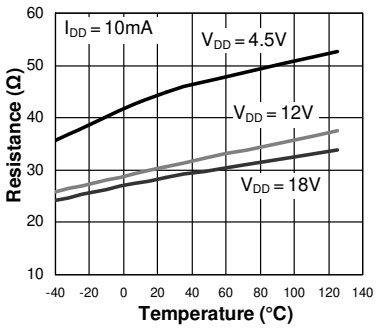


Conditions: T_A = 25ºC.

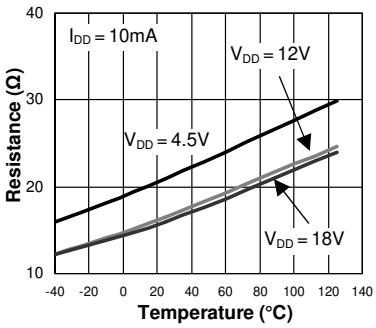
Propagation Delay (t_{D2}) vs. V_{DD}



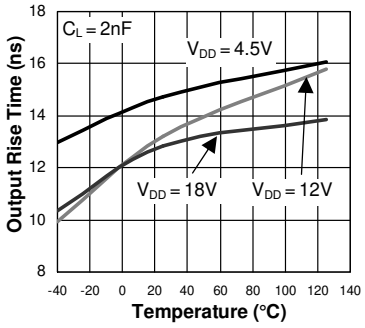
Output Source Resistance vs. Temperature



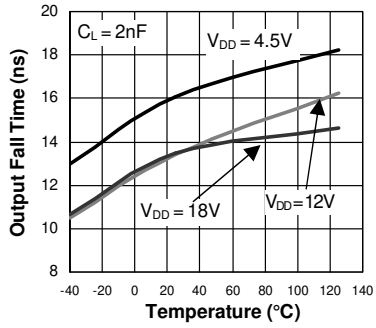
Output Sink Resistance vs. Temperature



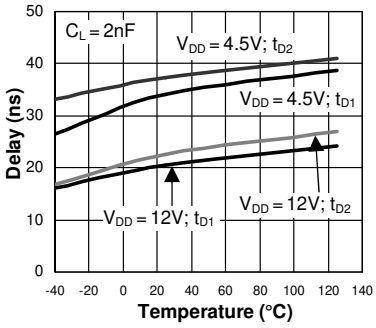
Output Rise Time vs. Temperature



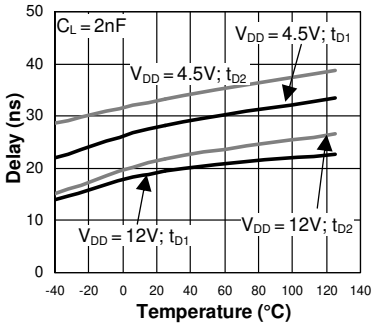
Output Fall Time vs. Temperature



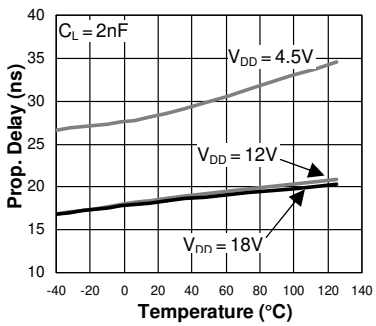
Prop. Delay (Inverting) vs. Temperature



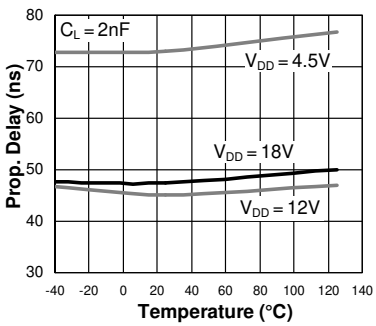
Prop. Delay (Non-Inverting) vs. Temperature



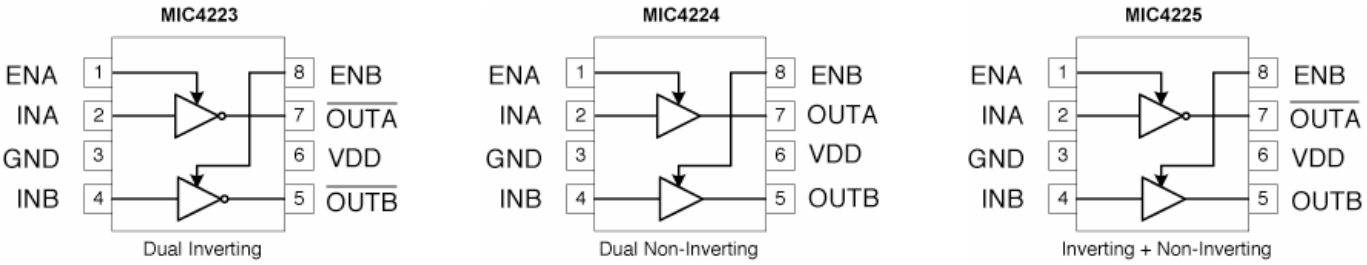
Enable to Output Delay (t_{D3}) vs. Temperature



Enable to Output Delay (t_{D4}) vs. Temperature



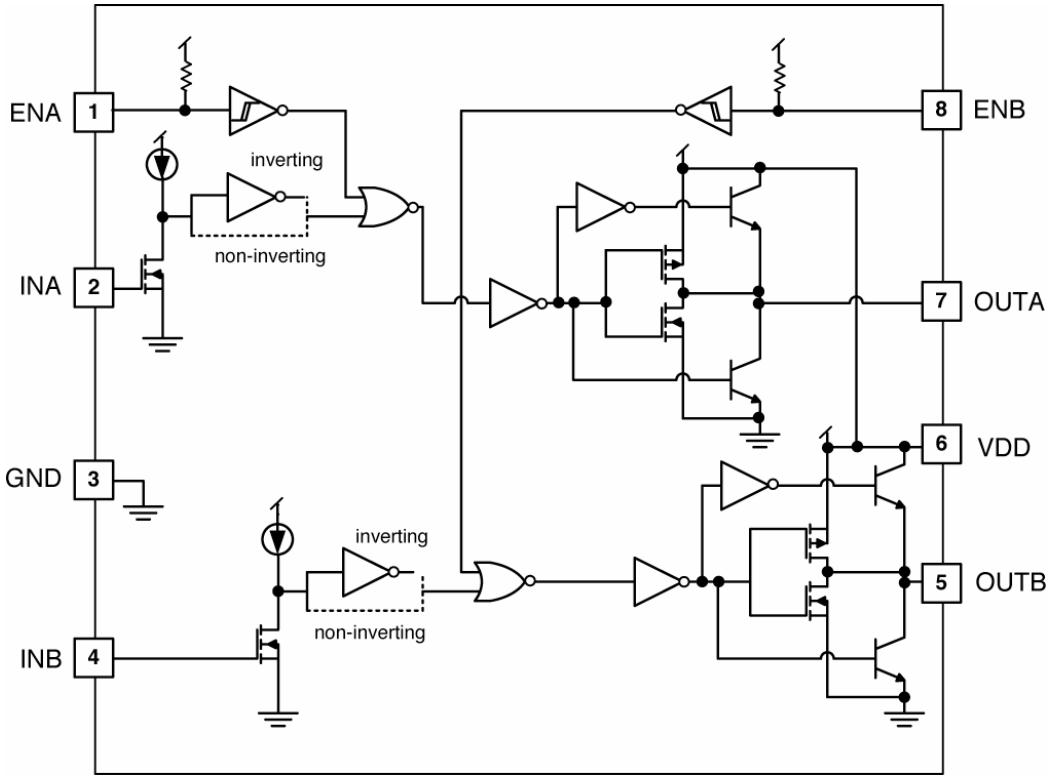
Functional Diagram



Logic Table

Enables		Inputs		MIC4223		MIC4224		MIC4225	
ENA	**ENB**	**INA**	**INB**	**OUTA**	**OUTB**	**OUTA**	**OUTB**	**OUTA**	**OUTB**
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

Block Diagram



Functional Description

The MIC4223, MIC4224 and MIC4225 are a family of dual high speed, high current drivers. The drivers come in both inverting and non-inverting versions. Each driver has an enable pin that turns the output off (low) regardless of the input.

The MIC4223 is a dual inverting driver. The MIC4224 is a dual non-inverting driver and the MIC4225 contains an inverting and non-inverting driver.

Enable

Each output has an independent enable pin that forces the output low when the enable pin is driven low. Each enable pin is internally pulled-up to V_{DD}. The outputs are enabled by default if the enable pin is left open. Pulling the enable pin low, below its threshold voltage, forces the output low. A fast propagation delay between the enable and output pins quickly disables the output, which is a requirement during a system fault condition.

Input Stage

The driver input stage is high impedance, TTL-compatible input stage. The driver's input threshold voltage makes it compatible with TTL and CMOS devices that are powered from supply voltages between 3V and V_{DD}. Hysteresis on the input pin improves noise immunity and prevents input signals with slow rise times from falsely triggering the output. The VDD pin current is slightly higher when the input voltage is above the high level threshold. See the Typical Characteristic graphs for additional information.

The input voltage signal may go up to -5V below ground without damage to the driver or cause a latch up condition. Negative input voltages that are 0.7V below ground or greater will increase propagation delay.

Output Driver Section

A functional diagram of the driver output is shown in Figure 2. The output drive is a parallel combination of MOSFET and Bipolar transistor. For a given silicon area, a bipolar device has a lower on-resistance than an equivalent MOS device. It sources and sinks current more consistently as the voltage across it changes. The low drive impedance of the bipolar allows fast turn-on and turn-off of the external MOSFET. The driver's internal MOSFET gives the output near rail-to-rail drive capability. This ensures a low R_{DSON} for the external MOSFET as well as noise immunity from dv/dt induced glitching.

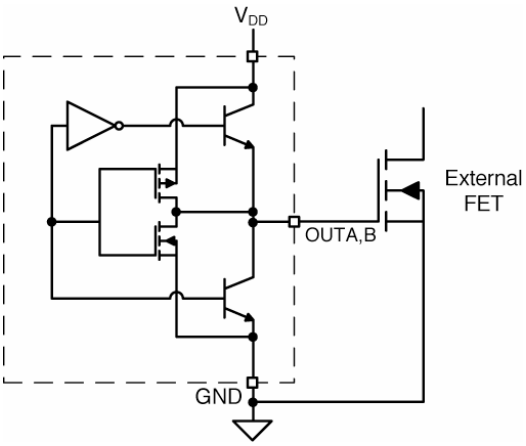


Figure 2. Output Driver

The slew rate of the output is non-adjustable and depends only on the V_{DD} voltage and how much capacitance is present at the OUTA, B pin. Changing the slew rate at the driver's input pin will not affect the output rise or fall times. The slew rate at the MOSFET gate can be adjusted by adding a resistor between the MOSFET gate and the driver output.

Application Information

Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

Output driver stage dissipation

Quiescent current dissipation used to supply the internal logic and control functions.

Output Driver Stage Power Dissipation

Power dissipation in the driver's output stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 3 shows a simplified circuit of the MIC4223 driving an external MOSFET.

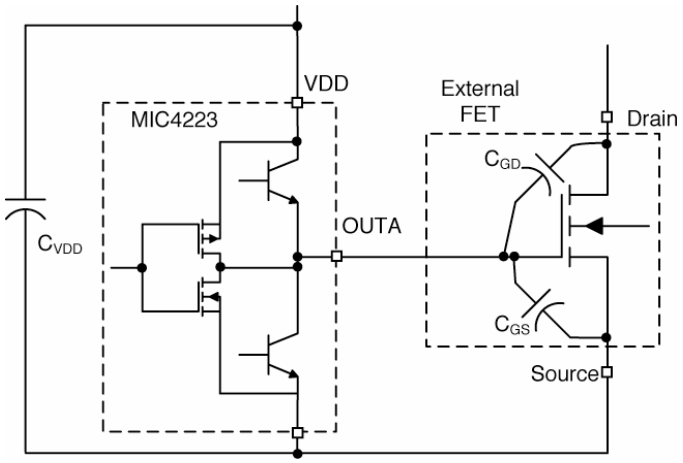


Figure 3. Functional MOSFET/Driver Diagram

Dissipation Caused by Switching the External MOSFET

Energy from capacitor C_{VDD} is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the upper driver MOSFET and Bipolar impedances. The effective capacitance of C_{GD} and C_{GS} is difficult to calculate since they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{GS}. Figure 4 shows a typical MOSFET gate charge curve. The graph illustrates that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge.

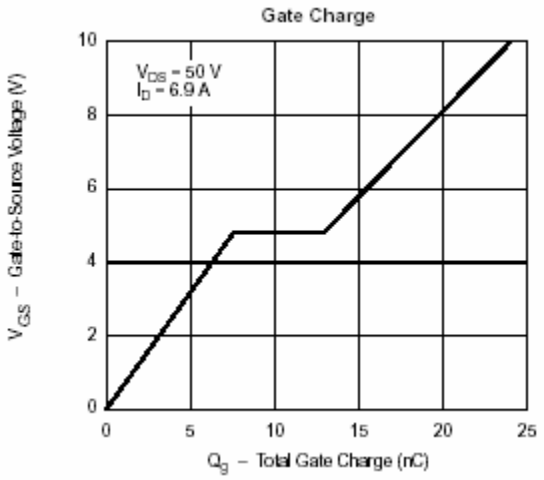


Figure 4. MOSFET Gate Charge vs. V_{GS}

The energy dissipated during turn-on is calculated as:

$$E = \tfrac{1}{2} \times C_{iss} \times V_{GS}^{\ 2}$$

where C_{iss} is the MOSFET's total gate capacitance

but :

$$Q = C \times V$$

so

$$E = 1/2 \times Q_G \times V_{GS}$$

An equivalent amount of energy is dissipated in the driver's sink circuit when the MOSFET turns off. The total energy and power dissipated by the drive components is:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

E_{DRIVER} is the energy dissipated per switching cycle

P_{DRIVER} is the power dissipated by switching the MOSFET on and off

Q_G is the total Gate charge at V_{GS}

V_{GS} is the MOSFETs Gate to Source voltage

f_S is the switching frequency of the Gate drive circuit

Quiescent Current Power Dissipation

Quiescent current powers the internal logic, level shifting circuitry and bias for the output drivers. This current is proportional to operating frequency and V_{DD} voltage. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the driver's quiescent current is:

$$Pdiss_{quiescent} = V_{DD} \times I_{DD}$$

Total Power Dissipation and Thermal Considerations

Total package power dissipation equals the power dissipation of each driver caused by driving the external MOSFETs plus the supply current.

$$Pdiss_{TOTAL} = Pdiss_{quiescent} + Pdriver_A + Pdriver_B$$

The die temperature may be calculated once the total power dissipation is known.

$$T_J = T_A + Pdiss_{TOTAL} \times \theta_{JA}$$

Where:

T_A is the Maximum ambient temperature

T_J is the junction temperature (°C)

$Pdiss_{TOTAL}$ is the power dissipation of the Driver

θ_{JA} is the thermal resistance from junction-to-ambient air (°C/W)

The following graphs help determine the maximum gate charge that can be driven with respect to switching frequency, supply voltage and ambient temperature.

Figure 5a shows the power dissipation in the driver for different values of gate charge with V_{DD} = 5V. Figure 5b shows the power dissipation at V_{DD} = 12V. Figure 5c show the maximum power dissipation for a given ambient temperature for the SOIC and ePAD MSOP packages.

The maximum operating frequency of the driver may be limited by the maximum power dissipation of the driver package.

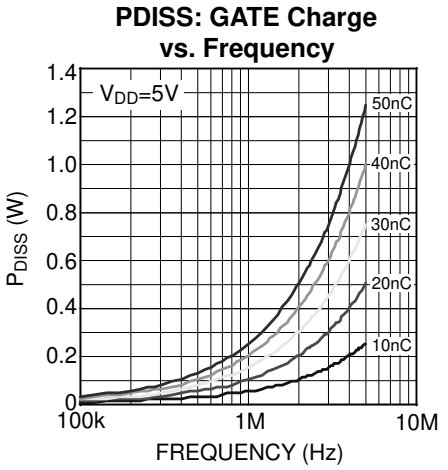


Figure 5a. P_{DISS} vs. Q_G and f_S for V_{DD} = 5V

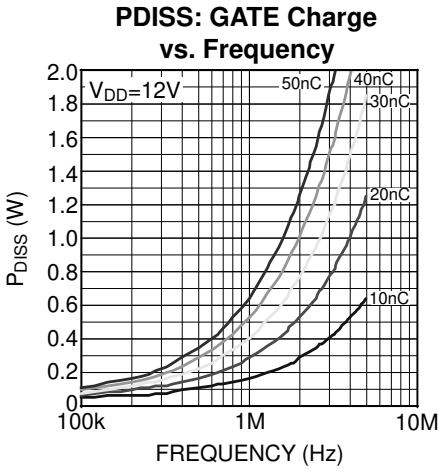


Figure 5b. P_{DISS} vs. Q_G and f_S for V_{DD} = 12V

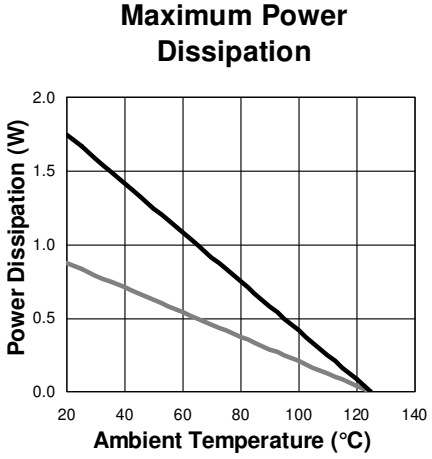


Figure 5c. Maximum P_{DISS} vs. Ambient Temperature

Bypass Capacitor Selection

Bypass capacitors are required for proper operation by supplying the charge necessary to drive the external MOSFETs as well as minimize the voltage ripple on the supply pins.

Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. Manufacturer specifications should be checked to insure voltage and temperature do not reduce the capacitance below the value needed. A minimum value of 1µF is required regardless of the MOSFETs being driven. Larger MOSFETs, with their higher input capacitance may require larger decoupling capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the VDD and GND pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Multiple vias insure a low inductance path and help with power dissipation. Refer to the section on layout and component placement for more information.

Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MOSFET driver necessitate proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching and excessive ringing.

Figure 6 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD}. Current in the gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate and out the Source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period where it should be turned on.

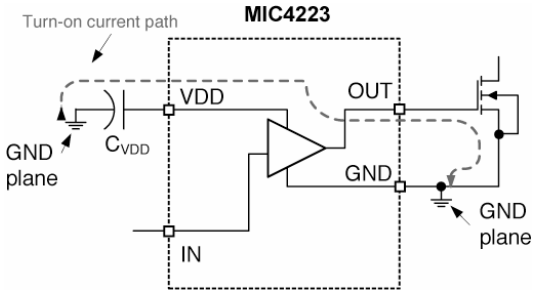


Figure 6. Driver Turn-On Current Path

Figure 7 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current from the V_{DD} supply replenishes charge in the decoupling capacitor, C_{VDD}.

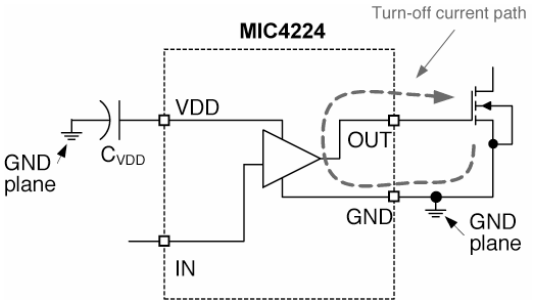


Figure 7. Driver Turn-Off Current Path

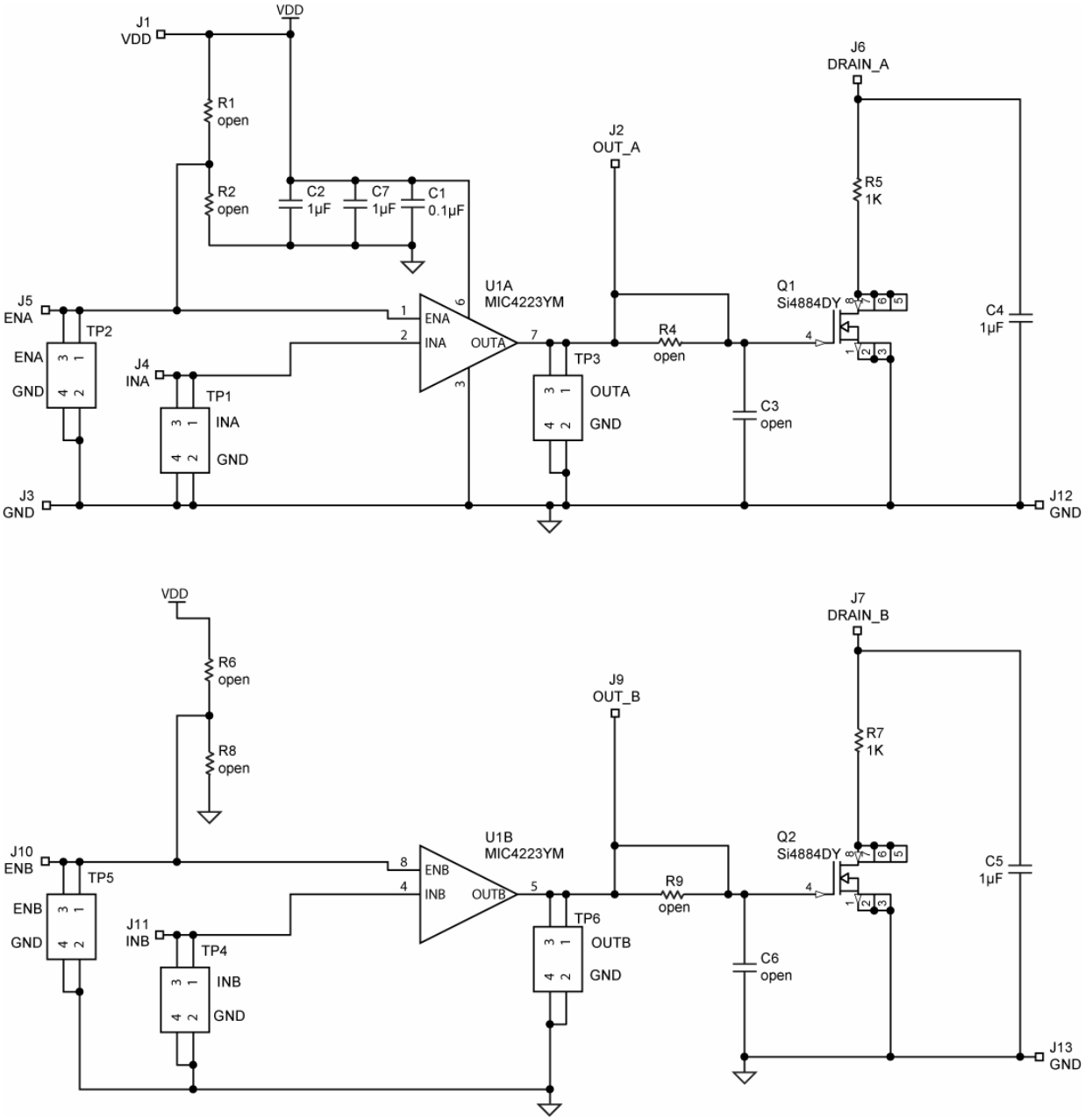
The following circuit guidelines should be adhered to for optimum circuit performance:

The V_{DD} bypass capacitor must be placed close to the VDD and ground pins. It is critical that the etch length between the decoupling capacitor and the VDD and GND pins be minimized to reduce pin inductance. Multiple vias in parallel help minimize inductance in the ground and V_{DD} paths.

A ground plane is recommended to minimize parasitic inductance and impedance of the return paths. The MIC4223 family of drivers is capable of high peak currents and very fast transition times. Any impedance between the driver, the decoupling capacitors and the external MOSFET will degrade the performance of the circuit.

Trace out the high di/dt and dv/dt paths, as shown in Figures 6 and 7 and minimize etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

Evaluation Board Schematic (SOIC)



SOIC Package

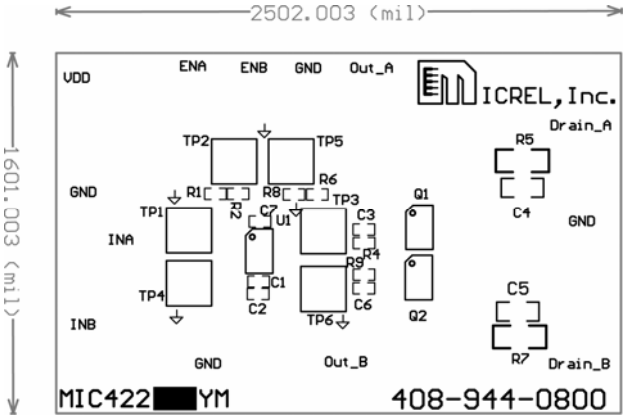
Bill of Materials (SOIC)

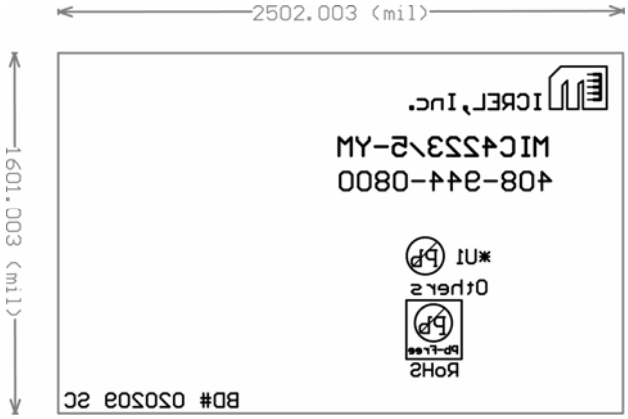
Item	Part Number	Manufacturer	Description	Qty.
C1	VJ0603Y104KXXAT	Vishay[1]	0.1µF/25V, X7R Ceramic Capacitor, Size 0603	1
C2, C7	C1608X5R1E105M	TDK[2]	1µF/25V, X5R, Ceramic Capacitor, Size 0603	2
or	06033D105MAT	AVX[3]	1µF/25V, X5R, Ceramic Capacitor, Size 0603	2
or	GRM188R61E105KA93	MuRata[4]	1µF/25V, X5R, Ceramic Capacitor, Size 0603	2
C4, C5	C3216X7R1E105K	TDK[2]	1µF/25V, X7R, Ceramic Capacitor, Size 1206	2
or	12063D105MAT	AVX[3]	1µF/25V, X7R, Ceramic Capacitor, Size 1206	2
or	GRM31MR71H105KA01	MuRata[4]	1µF/25V, X7R, Ceramic Capacitor, Size 1206	2
Q1, Q2	Si4174DY	Vishay[1]	30V N-Channel MOSFET	2
C3, R4, C6, R9, R1, R2, R6, R8			Open location – Size 0603	0
R5, R7	CRCW12061001FRT1	Vishay[1]	1kΩ Resistor, Size 1206	2
U1	**MIC4223YM**	Micrel, Inc.[5]	Dual Inverting 4A MOSFET Driver with SOIC Package	1
or	**MIC4224YM**	Micrel, Inc.[5]	Dual Non-Inverting 4A MOSFET Driver with SOIC Package	1
or	**MIC4225YM**	Micrel, Inc.[5]	Dual Inverting/Non-Inverting 4A MOSFET Driver with SOIC Package	1

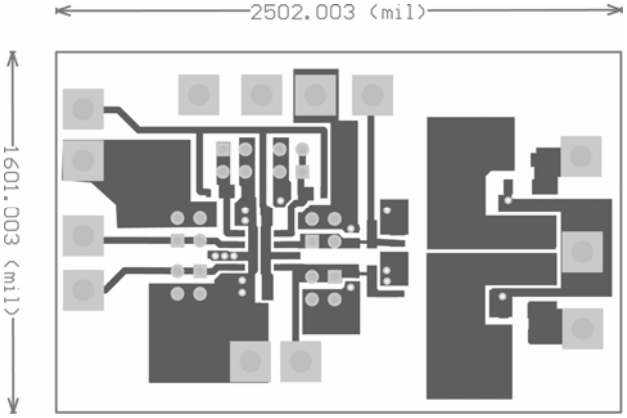
Notes:

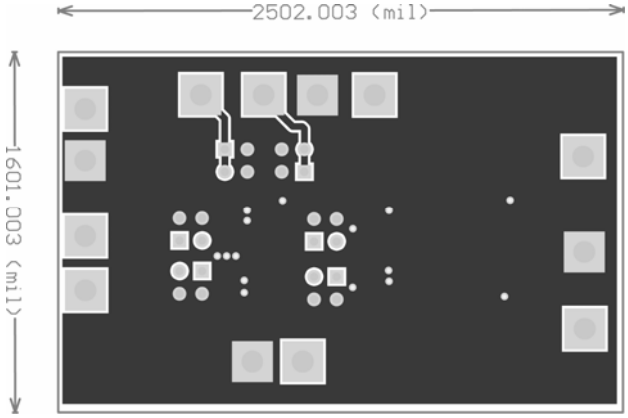
1. Vishay: www.vishay.com
2. TDK: www.tdk.com
3. AVX: www.avx.com
4. MuRata: www.murata.com
5. **Micrel, Inc:** www.micrel.com

PCB Layout (SOIC)

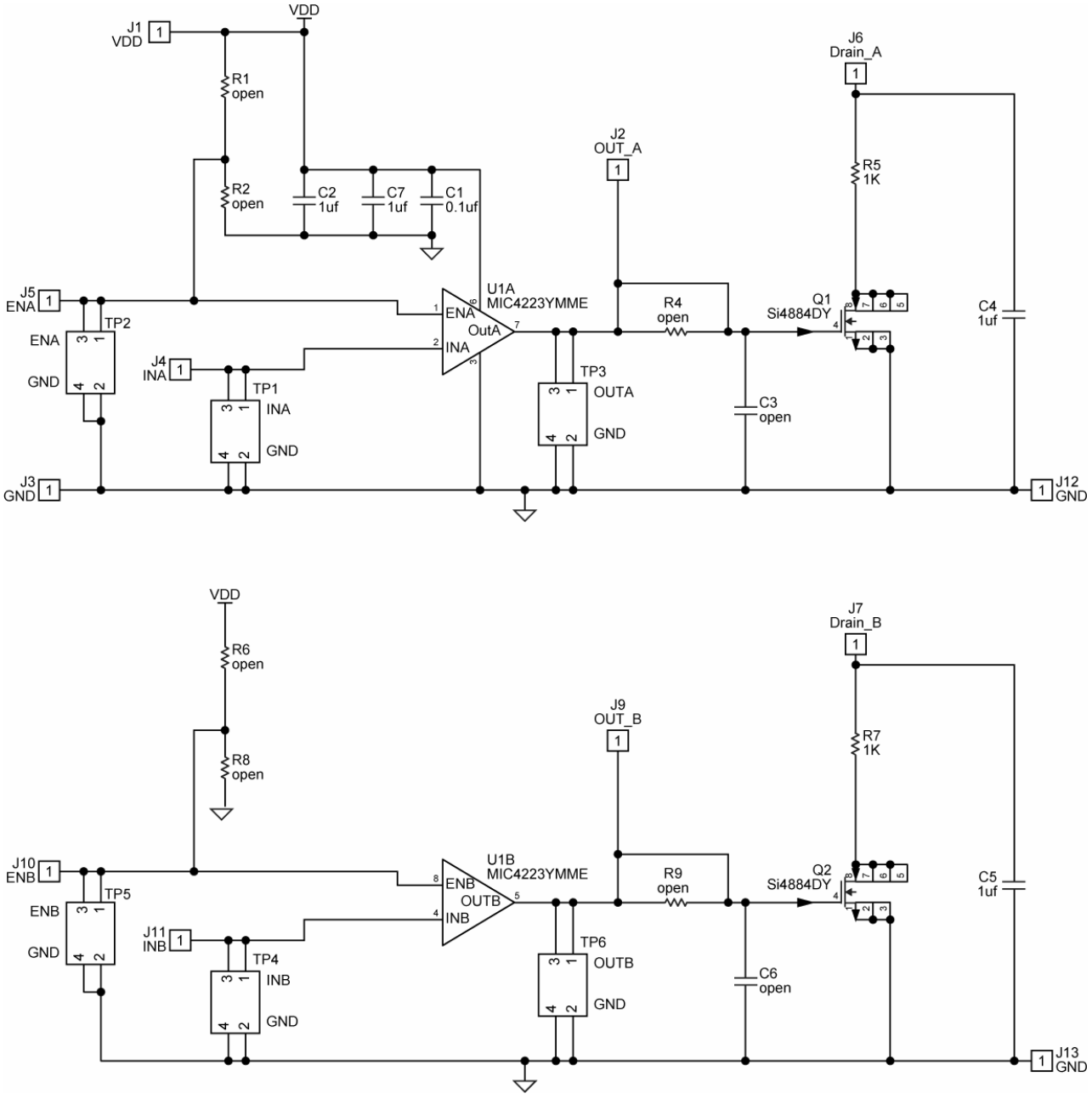






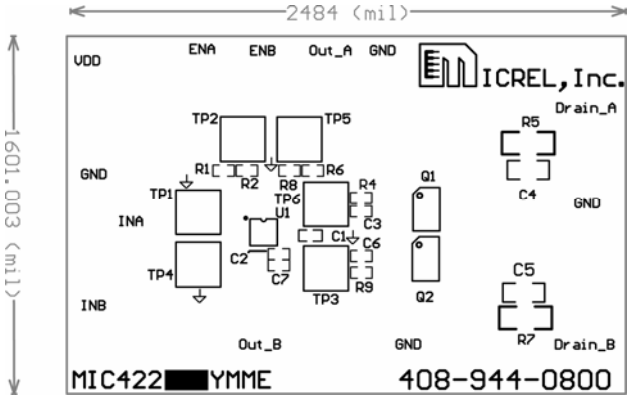


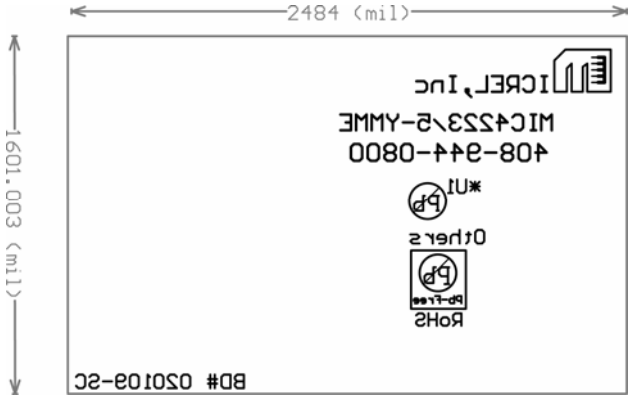
Evaluation Board Schematic (e-PAD MSOP)

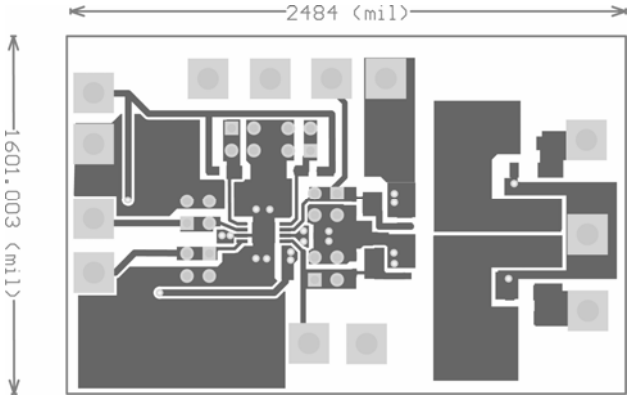


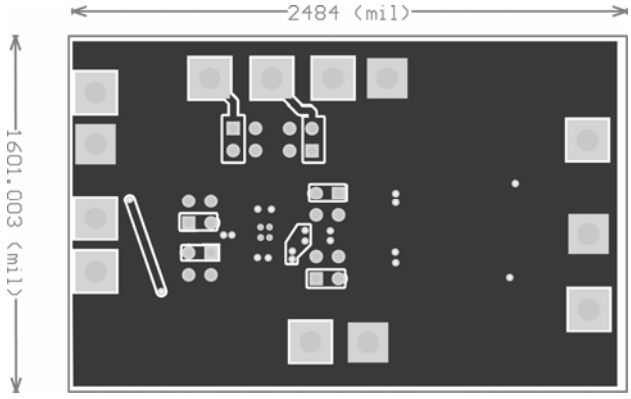
ePAD MSOP

PCB Layout (ePAD MSOP)









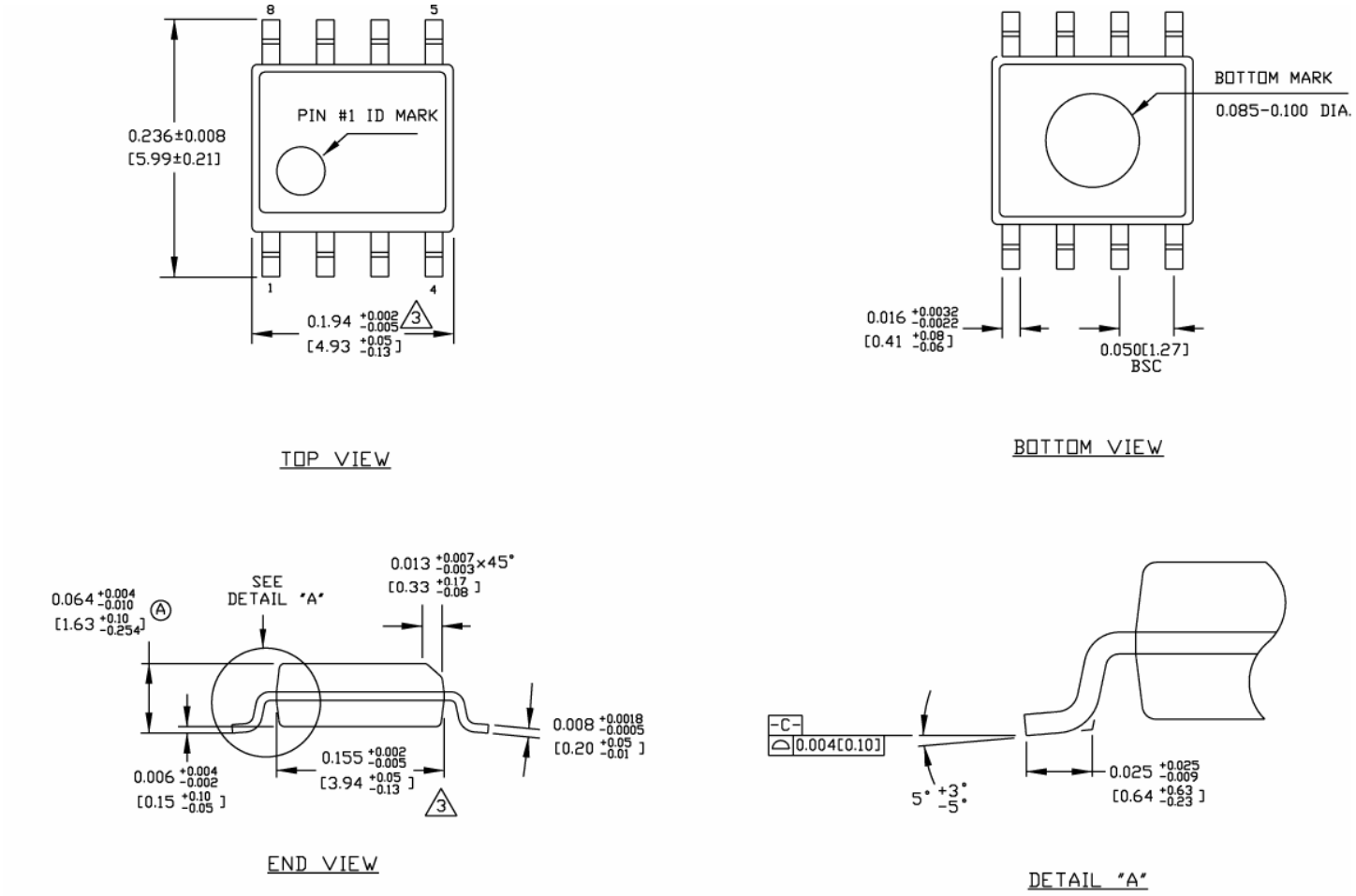
Bill of Materials (ePAD MSOP)

Item	Part Number	Manufacturer	Description	Qty.
C1	VJ0603Y104KXXAT	Vishay[1]	0.1µF/25V, X7R Ceramic Capacitor, Size 0603	1
C2, C7	C1608X5R1E105M	TDK[2]	1µF/25V, X5R, Ceramic Capacitor, Size 0603	2
or	06033D105MAT	AVX[3]	1µF/25V, X5R, Ceramic Capacitor, Size 0603	2
or	GRM188R61E105KA93	MuRata[4]	1µF/25V, X5R, Ceramic Capacitor, Size 0603	2
C4, C5	C3216X7R1E105K	TDK[2]	1µF/25V, X7R, Ceramic Capacitor, Size 1206	2
or	12063D105MAT	AVX[3]	1µF/25V, X7R, Ceramic Capacitor, Size	2
or	GRM31MR71H105KA01	MuRata[4]	1µF/25V, X7R, Ceramic Capacitor, Size	2
C3, R4, C6, R9, R1, R2, R6, R8			Open location – Size 0603	0
Q1, Q2	Si4174DY	Vishay[1]	30V N-Channel MOSFET	2
R5, R7	CRCW12061001FRT1	Vishay[1]	1kΩ Resistor, Size 1206	2
U1	**MIC4223YMME**	Micrel, Inc.[5]	Dual Inverting 4A MOSFET Driver with ePAD MSOP Package	1
or	**MIC4224YMME**	Micrel, Inc.[5]	Dual Non-Inverting 4A MOSFET Driver with ePAD MSOP Package	1
or	**MIC4225YM**	Micrel, Inc.[5]	Dual Inverting/Non-Inverting 4A MOSFET Driver with ePAD MSOP Package	1

Notes:

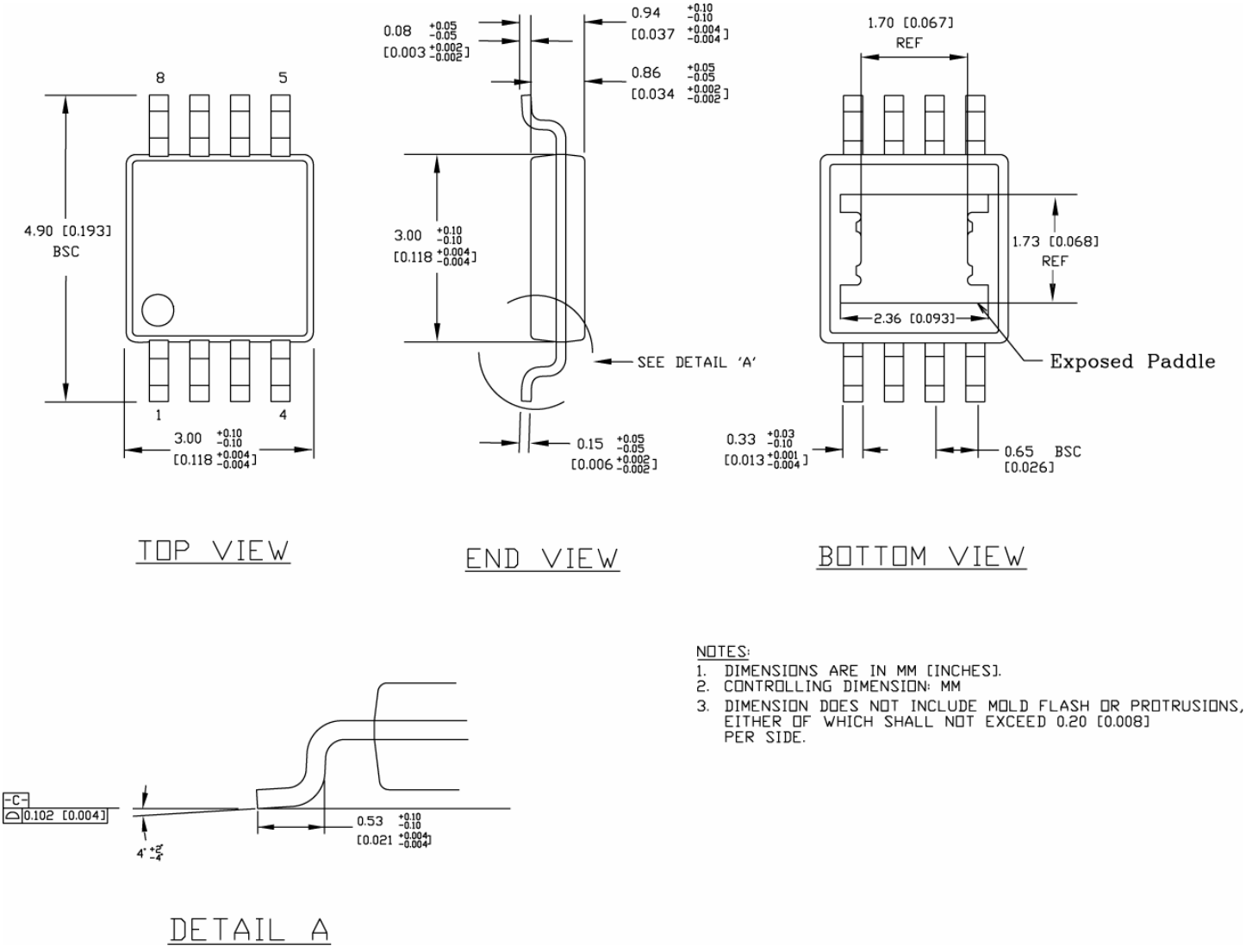
1. Vishay: www.vishay.com
2. TDK: www.tdk.com
3. AVX: www.avx.com
4. MuRata: www.murata.com
5. **Micrel, Inc:** www.micrel.com

Package Information



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

8-Pin SOIC (M)



8-Pin ePAD MSOP (MME)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com