Regulators ICs for Digital Cameras and Camcorders

System Switching Regulator IC with Built-in FET (10V)

BD8355MWV

No.11036EAT20

●Description

BD8355MWV is a system switching regulator for Li 2 cell composed of 6 step-down synchronous rectification channels and 1 step-up Di rectification channel for LED application. Using a charge-pump system for high side FET driver and including power MOSFET reduce the number of peripheral devices and realize high efficiency.

●Functions

1) Includes step-down 6 CH (CH1~6), step-up for LED 1CH (7CH) total 7CH included.
2) Includes Power MOSFET for all channels.
3) Includes Charge-pump circuit for high side driver.
4) Operating frequency of 750 kHz.
5) CH1 and 4 are common, 3 and 5 are also common, and others are possible to turn ON/OFF independently.
6) Includes Short Circuit Protection (SCP), Under Voltage Lock Out (UVLO) and Thermal Shut Down (TSD).
7) Includes Short Circuit Protection for CH6 (SCP6).
8) Includes Over Voltage Protection for CH7.
9) Thermally enhanced UQFN056V7070 package (7mm×7mm, 0.4mm pitch)

●Applications

For digital single-lens reflex camera, digital video camera

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	VCC, VBAT, VHx1~6	-0.3~11.0	V
	VLx1~6	-0.3~VHx	V
	VLx7	-0.3~28.0	V
	HVREG	-0.3~15.0	V
	CTL14, CTL2, CTL35, CTL6	-0.3~11.0	V
	CTL7	-0.3~7.0	V
Maximum Current	IomaxLx1, Lx4, Lx5	±1.5	A
	IomaxLx2, Lx3	±0.8	A
	IomaxLx6	±2.0	A
	IomaxLx7	+1.0	A
Power Dissipation	Pd	420 (*1)	mW
		930 (*2)	mW
Operating Temperature	Topr	-25~+85	℃
Storage Temperature	Tstg	-55~+125	℃
Junction Temperature	Tjmax	125	℃

*1 Without external heat sink, power dissipation degrades by 4.2mW/℃ above 25℃.
*2 Power dissipation degrades by 9.3mW/℃ above 25℃, when mounted on a 74.2mm×74.2mm×1.6mmt grass epoxy PCB.

●Recommended Operating Conditions(Ta=-25~+85℃)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	VCC, VBAT, VHx1~6	4.0	7.2	10.0	V
VREGA Output Capacitor	CVREGA	0.47	1.0	2.2	μF
VREGD Output Capacitor	CVREGD	0.47	1.0	2.2	μF
HVREG Output Capacitor	CHVREG	0.47	1.0	2.2	μF
Flying Capacitor	CFLY	0.047	0.1	0.22	μF
Oscillator Frequency	Fosc	500	750	1800	kHz
Timing Resistor	RRT	15	47	82	kΩ

●Electrical Characteristics(Ta=25℃,Vcc=VBAT=7.2V, fosc=750kHz with no designation)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
【Reference Voltage】						
VREGA Output Voltage	VREGA	3.54	3.60	3.66	V	VREGA=-1mA
Line Regulation	DVli	-	-	10	mV	VCC=4V~10V, VREGA=-1mA
Load Regulation	DVlo	-	-	10	mV	VREGA=-1mA~-5mA
【Bias Voltage】						
VREGD Output Voltage	VREGD	3.50	3.60	3.70	V	VREGD=-10mA
【Charge Pump】						
HVREG Output Voltage	HVREG	VBAT +3.50	VBAT +3.60	-	V	Iout=0mA, FB=2.5V
Output Impedance	RHVREG	-	24	40	Ω	Iout=-30mA, CFLY=0.1μF
【Oscillator】						
Oscillator Frequency	fosc	650	750	850	kHz	RT=47kΩ
Oscillator Frequency cofficient	Df	-	0	2	%	VCC=4V~10V
【PWM Comparator】						
CH7 0% Duty Threshold Voltage	Vth0	0.2	0.3	-	V	
CH7 Max Duty	Dmax	86	92	96	%	
【Error Amplifier 1】(CH1)						
Threshold Voltage	Veth1	0.790	0.800	0.810	V	
Output Voltage L	VFBL1	-	0.03	0.2	V	INV1=0.9V
Output Voltage H	VFBH1	3.3	3.5	-	V	INV1=0.7V
Output Sink Current	Isink1	4.0	17.0	-	mA	INV1=0.9V, FB1=1.75V
Output Source Current	Isource1	-	-140	-70	μA	INV1=0.7V, FB1=1.75V
Input Bias Current	Ibias1	-100	0	100	nA	INV1=0V
【Error Amplifier 2】(CH2~6)						
Threshold Voltage	Veth	0.990	1.000	1.010	V	
Output Voltage L	VFBL	-	0.03	0.2	V	INV=1.1V
Output Voltage H	VFBH	3.3	3.5	-	V	INV=0.9V
Output Sink Current	Isink	4.0	17.0	-	mA	INV=1.1V, FB=1.75V
Output Source Current	Isource	-	-140	-70	μA	INV=0.9V, FB=1.75V
Input Bias Current	Ibias	-100	0	100	nA	INV=0V
【Error Amplifier 3】(CH7)						
Threshold Voltage	Veth7	0.285	0.300	0.315	V	
Output Voltage L	VFBL7	-	0.03	0.2	V	INV=0.4V
Output Voltage H	VFBH7	3.3	3.5	-	V	INV=0.2V
Output Sink Current	Isink7	4.0	17.0	-	mA	INV=0.4V, FB=1.75V
Output Source Current	Isource7	-	-140	-70	μA	INV=0.2V, FB=1.75V
Input Bias Current	Ibias7	-50	0	50	nA	INV7=0V

Parameter		Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
【Soft Start】							
CH1 Soft Start Time		Tss1	1.3	2.5	3.7	msec	CH1
CH2-6 Soft Start Time		Tss2-6	1.5	3.1	4.6	msec	CH2~6
CH7 Duty Restriction Time		TDTC7	12.0	15.0	18.0	msec	CH7
【 Driver】							
CH1~6 Lx Pull-down Resistor		RLx	300	500	700	Ω	CTL=0V
CH1 High Side Nch FET On Resistor		RonH1	-	0.27	0.44	Ω	Lx1=-50mA
CH1 Low Side Nch FET On Resistor		RonL1	-	0.15	0.24	Ω	Lx1=50mA
CH2 High Side Nch FET On Resistor		RonH2	-	0.42	0.68	Ω	Lx2=-50mA
CH2 Low Side Nch FET On Resistor		RonL2	-	0.30	0.48	Ω	Lx2=50mA
CH3 High Side Nch FET On Resistor		RonH3	-	0.52	0.84	Ω	Lx3=-50mA
CH3 Low Side Nch FET On Resistor		RonL3	-	0.20	0.32	Ω	Lx3=50mA
CH4 High Side Nch FET On Resistor		RonH4	-	0.20	0.32	Ω	Lx4=-50mA
CH4 Low Side Nch FET On Resistor		RonL4	-	0.30	0.48	Ω	Lx4=50mA
CH5 High Side Nch FET On Resistor		RonH5	-	0.23	0.37	Ω	Lx5=-50mA
CH5 Low Side Nch FET On Resistor		RonL5	-	0.22	0.36	Ω	Lx5=50mA
CH6 High Side Nch FET On Resistor		RonH6	-	0.22	0.36	Ω	Lx6=-50mA
CH6 Low Side Nch FET On Resistor		RonL6	-	0.30	0.48	Ω	Lx6=50mA
CH7 Nch FET On Resistor		Ron7	-	0.50	0.80	Ω	Lx7=50mA
【Under Voltage Lock Out(UVLO)】							
Threshold Voltage1		Vthuvlo1	3.3	3.4	3.5	V	VCC pin voltage
Hysteresis Voltage		DVuv	25	100	200	mV	VCC pin voltage
Threshold Voltage2		Vthuvlo2	-	2.5	2.7	V	VREGA pin voltage
Threshold Voltage3		Vthuvlo3	-	3.15	3.35	V	VREGD pin voltage
【Short Circuit Protection(SCP)】							
Timer Start Voltage		Vstart	2.65	2.8	2.95	V	FB1~5, 7 pin v oltage
CH6 Timer Start Voltage		Vstart6	0.45	0.50	0.55	V	INV6 pin voltage
SCP pin Threshold Voltage		Vscpth	0.9	1.0	1.1	V	
SCP6 pin Threshold Voltage		Vscp6th	0.9	1.0	1.1	V	
SCP pin Source Current		Iscp	-1.4	-1.0	-0.6	μA	SCP=0.1V
SCP6 pin Source Current		Iscp6	-1.4	-1.0	-0.6	μA	SCP6=0.1V
SCP pin Stand-by Voltage		Vstscp	-	10	100	mV	CTL=3V, FB=0V
SCP6 pin Stand-by Voltage		Vstscp6	-	10	100	mV	CTL6=3V, INV6=1.0V
【Over Voltage Protection(OVP)】							
CH7 OVP Threshold Voltage		VOVP7	26.5	28.0	29.5	V	Vo7 pin voltage
【Control】							
CTL1-6 Control Voltage	Active	VCTLH	2	-	VCC	V	
	Non-Active	VCTLL	-0.3	-	0.4	V	
CTL7 Control Voltage	Active	VCTLH	2	-	5.5	V	
	Non-Active	VCTLL	-0.3	-	0.4	V	
CTL pin Pull-Down Resistor		RCTL	0.6	1.0	1.4	MΩ	
【Whole device】							
Stand-by Current	VCC pin	Istb1	-	0	5	μA	CTL=0V
	Hx pin	Istb2	-	0	5	μA	Hx1~6=10V, sum of Hx1~6
	Lx7 pin	Istb3	-	0	5	μA	Lx7=28V
Circuit Current		Icc	-	6.0	9.0	mA	CTL=3V, FB=2.5V

◎This product is not designed for normal operation within a radioactive environment.

●Package dimensions

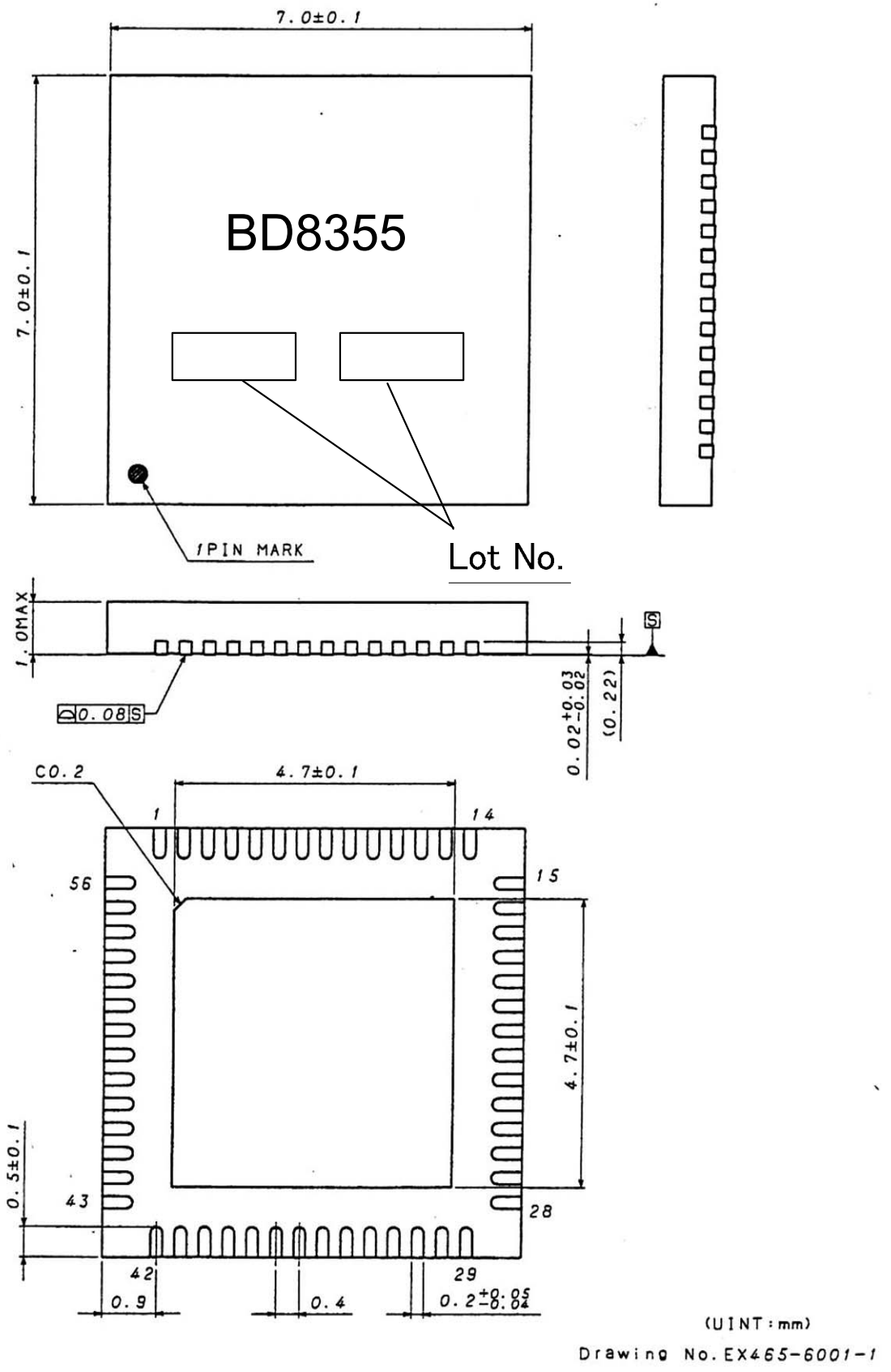


Fig. 1 Package dimension

●PIN Assignments

Pin No.	Pin Name	Pin Descriptions	Pin No.	Pin Name	Pin Descriptions
1	INV7	CH7 Error Amplifier Negative Input Pin	29	CTL35	CH3, 5 ON/OFF Control Pin
2	FB6	CH6 Error Amplifier Output Pin	30	CTL14	CH1, 4 ON/OFF Control Pin
3	INV6	CH6 Error Amplifier Negative Input Pin	31	PGND12	Ground Pin for CH1, 2 Output
4	FB5	CH5 Error Amplifier Output Pin	32	PGND12	Ground Pin for CH1, 2 Output
5	INV5	CH5 Error Amplifier Negative Input Pin	33	Lx2	Pin for Connecting to Inductor of CH2
6	GND	Ground Pin	34	Hx2	CH2 Highside Transistor and Driver Supply Voltage
7	FB4	CH4 Error Amplifier Output Pin	35	Hx3	CH3 Highside Transistor and Driver Supply Voltage
8	INV4	CH4 Error Amplifier Negative Input Pin	36	Lx3	Pin for Connecting to Inductor of CH3
9	INV3	CH3 Error Amplifier Negative Input Pin	37	PGND34	Ground Pin for CH3, 4 Output
10	FB3	CH3 Error Amplifier Output Pin	38	PGND34	Ground Pin for CH3, 4 Output
11	INV2	CH2 Error Amplifier Negative Input Pin	39	Lx4	Pin for Connecting to Inductor of CH4
12	FB2	CH2 Error Amplifier Output Pin	40	Lx4	Pin for Connecting to Inductor of CH4
13	SCP6	CH6 Short Circuit Protection Delay Time Setting Pin with External Capacitor	41	CTL6	CH6 ON/OFF Control Pin
14	CTL7	CH7 ON/OFF Control Pin	42	CTL2	CH2 ON/OFF Control Pin
15	INV1	CH1 Error Amplifier Negative Input Pin	43	Hx4	CH4 Highside Transistor and Driver Supply Voltage
16	FB1	CH1 Error Amplifier Output Pin	44	Hx4	CH4 Highside Transistor and Driver Supply Voltage
17	SCP	CH1-5 and CH7 Short Circuit Protection Delay Time Setting	45	Hx5	CH5 Highside Transistor and Driver Supply Voltage Pin
18	RT	Oscillator Frequency Adjustment Pin with External	46	Lx5	Pin for Connecting to Inductor of CH5
19	VREGA	3.6V Reference Output Voltage Pin	47	PGND56	Ground Pin for CH5, 6 Output
20	VCC	Input Supply Voltage Pin	48	PGND56	Ground Pin for CH5, 6 Output
21	VREGD	3.6V Lowside Transistor Bias Voltage Output Pin	49	Lx6	Pin for Connecting to Inductor of CH6
22	CMINUS	Pin for Connecting Chargepump Flying Capacitor	50	Lx6	Pin for Connecting to Inductor of CH6
23	HVREG	Chargepump Voltage Output Pin	51	Hx6	CH6 Highside Transistor and Driver Supply Voltage
24	CPLUS	Pin for Connecting Chargepump Flying Capacitor	52	Hx6	CH6 Highside Transistor and Driver Supply Voltage
25	VBAT	Chargepump Input Supply Voltage Pin	53	Lx7	Pin for Connecting to Inductor of CH7
26	Hx1	CH1 Highside Transistor and Driver Supply Voltage	54	PGND7	Ground Pin for CH7 Output
27	Lx1	Pin for Connecting to Inductor of CH1	55	Vo7	Voltage Monitor Pin for CH7 Over Voltage Protection
28	Lx1	Pin for Connecting to Inductor of CH1	56	FB7	CH7 Error Amplifier Output Pin

●PIN Assignments

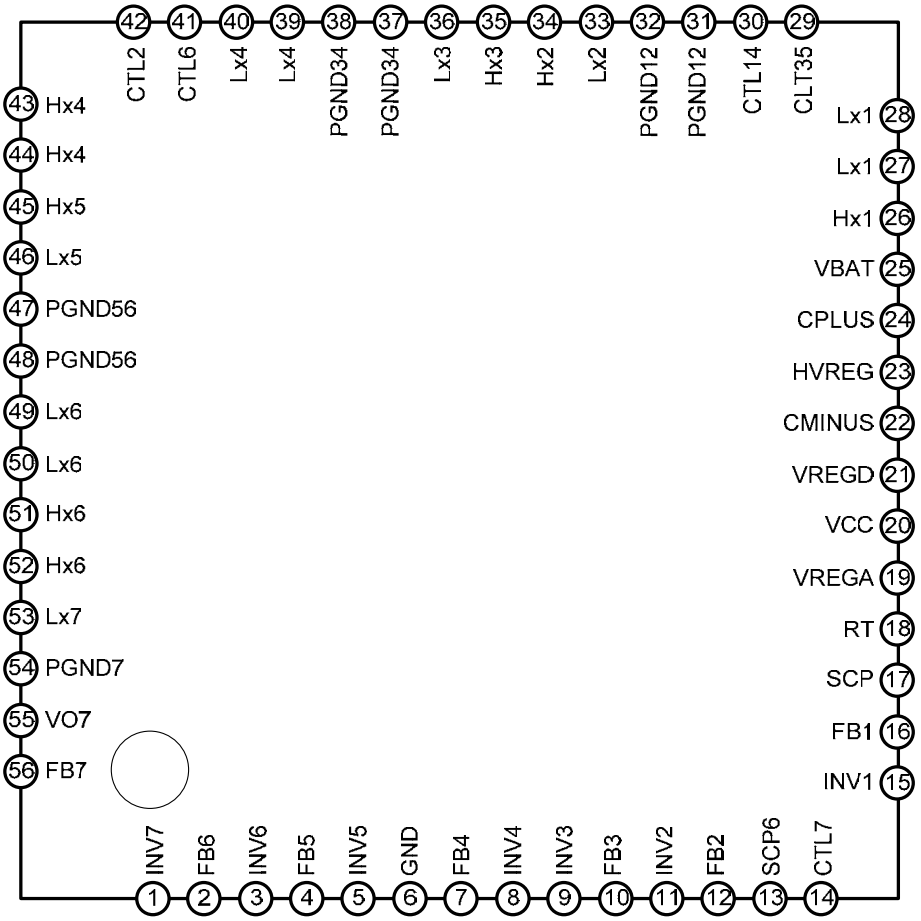


Fig. 2 Pin Assignments

●Block diagram and application circuit

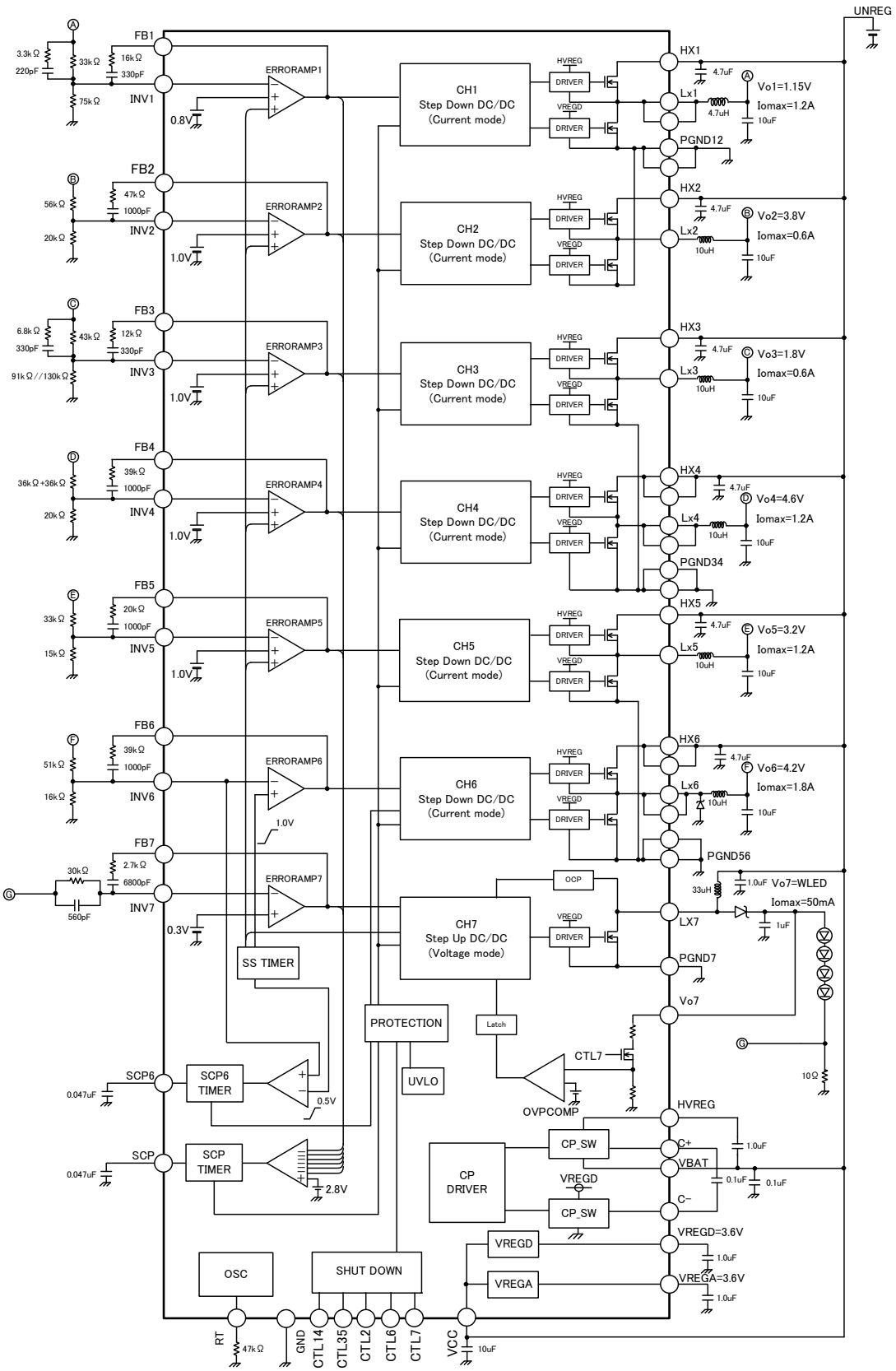
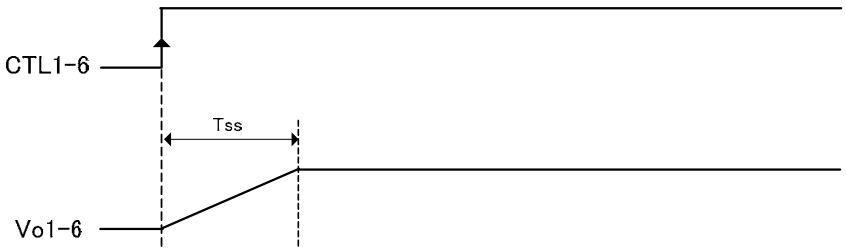


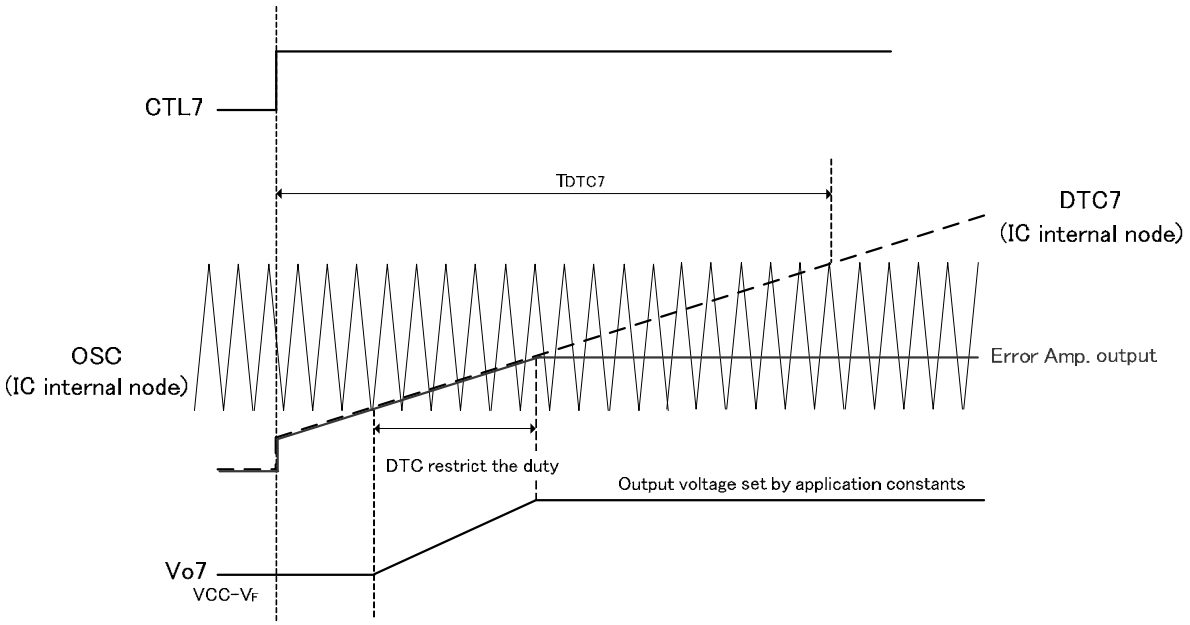
Fig. 3 Application circuit

* We are confident that the above applied circuit diagram should be recommended, but please thoroughly confirm its characteristics when using it. In addition, when using it with the external circuit's constant changed, please make a decision that allows a sufficient margin in light of the fluctuations of external components and ROHM's IC in terms of not only static characteristic but also transient characteristic.

●Timing chart



Tss1: 2.5 msec (fosc=750 kHz)
Tss2-6: 3.1 msec (fosc=750 kHz)
Fig. 4 CH1-6 startup sequence



TDTC7 (CH7 duty restriction time): 15 msec (fosc=750 kHz)
※Turn on any CTL1-6 and wait more than 500 usec before turn on CTL7.
Fig. 5 CH7 startup sequence

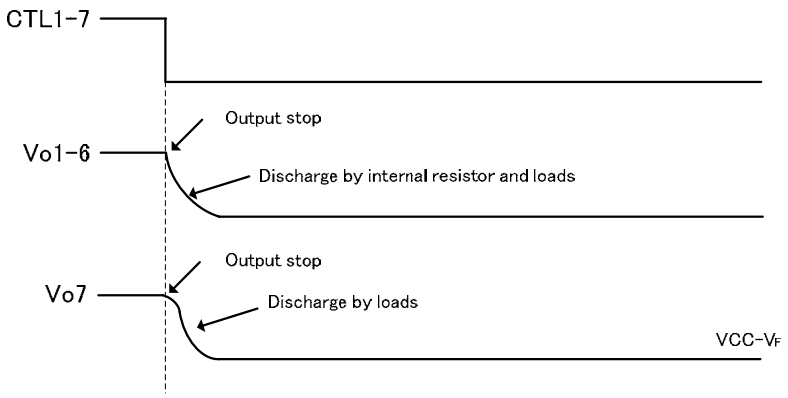


Fig. 6 stop sequence

●Functional Description / peripheral devices setting

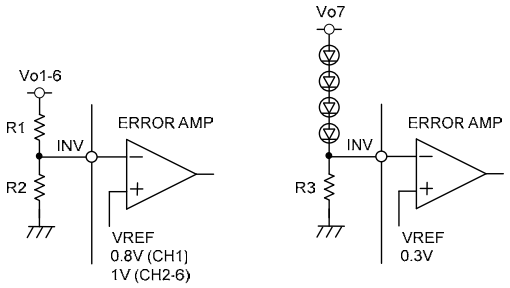
1. Internal Regulator (VREGA, VREGD)
   Both VREGA and VREGD are internal regulator of 3.6 V output. Bypass VREGA/VREGD to GND with a capacitor between 0.47 µF and 2.2 µF. In addition, it needs care for the voltage between VREGA and VREGD not to excess 0.3 V to avoid IC malfunctions.

2. Control block (SHUT DOWN)
   Inputting voltages to CTL14, 2, 35, 6, and 7 control ON/OFF of respective channels. Note that it is impossible to independently control CH1 and 4, and to independently control CH3 and 5. In addition, turn on any CTL1-6 and wait 500 usec before turning on CTL7. Input higher voltage than 2 V to CTL14, 2, 35, or 6 to turn on each channel. Open or input voltage -0.3 ~ 0.4 V to those to turn off. Input 2 ~ 5.5 V to CTL7 to turn on CH7. Open or input voltage -0.3 ~ 0.4 V to CTL7 to turn off. The states of output terminals (Lx1-7), FB terminals, SCP/SCP6 terminals, and internal regulator (VREGA and VREGD) are written below.
   Each CTL terminal contains pull down resistor of 1MΩ (typ.)

CTL					Lx							FB							VREGA	VREGD	SCP	SCP6
14	2	35	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7				
L	L	L	L	L	L	L	L	L	L	L	H-Z	L	L	L	L	L	L	L	L	L	L	L
H	L	L	L	L	A	L	L	A	L	L	H-Z	A	L	L	A	L	L	L	A	A	A	L
L	H	L	L	L	L	A	L	L	L	L	H-Z	L	A	L	L	L	L	L	A	A	A	L
L	L	H	L	L	L	L	A	L	A	L	H-Z	L	L	A	L	A	L	L	A	A	A	L
L	L	L	H	L	L	L	L	L	L	A	H-Z	L	L	L	L	L	A	L	A	A	L	A
L*	L*	L*	L*	H	L*	L*	L*	L*	L*	L*	A	L*	L*	L*	L*	L*	L*	A	A	A	A	L*
H	H	H	H	H	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A

* Turn on any CTL1-6 before turn on CTL7. Conditions of Lx1～6, FB1～6, SCP6 are changed with active channel. A: active

3. Output voltage/current setting



$$Vo = \frac{(R1+R2)}{R2} \times 0.8[V] \cdots (1)$$

$$Vo = \frac{(R1+R2)}{R2} \times 1.0[V] \cdots (2)$$

$$Io = \frac{0.3}{R3} [A] \cdots (3)$$

Fig. 7 Setting of feedback resistance

(a) Setting output voltage of CH1-6
The reference voltages of ERROR AMP. are 0.8 V (CH1) and 1 V (CH2-6). The output voltages are determined as equation (1) and (2). Set the value of feedback resistance R1 and R2 which are connected to INV1-6 pin.

(b) Setting output current of CH7
The reference voltage of CH7 ERROR AMP. is 0.3 V. The current flowing LED is determined as equation (3). Set the value of feedback resistance R3, considering the tolerance current of LED.

4. Startup/Stop sequence
   To avoid rush current on startup, each channel has soft start function. The output voltage of CH1 reaches to the target in Tss1=2.5msec (typ.) and the output voltage of CH2 ~ 6 reaches to the target in Tss2-6=3.1msec (typ.). In case of CH7, the output of error amplifier is restricted in TDTC7=15msec (typ.).
   Note that Tss1-6, TDTC7 vary from typical value Ttyp as following with setting of switching frequency.

$$T_{ss1\text{-}6},\ T_{DTC7},\ T_{stop1} = T_{typ} \times \frac{750}{fosc[kHz]}\ [msec]$$

5. Protection matrix
   The following table displays state of outputs when protection is operating.

	Lx1-5	Lx6	Lx7	FB1-6	FB7	VREGA	VREGD	HVREG	SCP	SCP6
Short Circuit Protection (CH1-5,7)	H-Z	A	H-Z	A	A	A	A	A	-	A
Short Circuit Protection (CH6)	A	H-Z	A	A	A	A	A	A	A	-
Under Voltage Lockout (VCC)	H-Z	H-Z	H-Z	NA	NA	A	A	NA	NA	NA
Under Voltage Lockout (VREGA)	H-Z	H-Z	H-Z	NA	NA	-	A	NA	NA	NA
Under Voltage Lockout (VREGD)	H-Z	H-Z	H-Z	NA	NA	A	-	NA	NA	NA
Under Voltage Lockout (HVREG)	H-Z	H-Z	A	NA	A	A	A	-	NA	NA
Thermal Shutdown（TSD）	H-Z	H-Z	H-Z	NA	NA	NA	NA	NA	NA	NA

A: active
NA: non-active

6. Short circuit protection (SCP, SCP6)
For CH1 ~ 5 and 7, monitoring the output voltages of error amplifier (FB voltage), if the voltages become more than 2.8 V, the output of SCPCOMP will become “L” level, and transistor “M1” will turn off. Thus the current “1μA” be supplied to CSCP the capacitor connected to SCP terminal. The outputs stop when SCP terminal voltage reaches 1 V. The time from short circuit detect to outputs stop (tscp) is set as shown below.

$$tSCP[s] = 1.0 \times CSCP[\mu F]$$

On the other hand, short circuit of CH6 is detected when the error amplifier input of CH6 (INV6) becomes less than 0.5 V. The time from short circuit detect to output stop (tscp6) is set with CSCP6 as tscp.
To release from short circuit protection latch state, turn CTL terminal to “L” level. Connect SCP/SCP6 terminal to GND when the function of short circuit protection is not used.

7. Over voltage protection(OVP)
In CH7, when LED is open, INV7 become L and output voltage increase suddenly. If that condition continues Lx7 voltage increase and exceed break down voltage.CH7 has over voltage protection circuit (OVP) not to exceed break down voltage. When the voltage of VO7 terminal becomes more than 28V (typ.), OVP function works and CH7 stops operating. Once OVP is detected, CH7 becomes latch state. To release from latch state, turn off CTL7.

8. Thermal shutdown circuit (TSD)
The TSD circuit protects the IC against thermal runaway and heat damage. The TSD thermal sensor detects junction temperature. When the temperature reaches the TSD threshold (typ: 175), the circuit switches the outputs of all channels, VREGA, and VREGD OFF. At the same time, it sets the FB1-7 terminals “L” level. The hysteresis width (typ: 15) provided between the TSD function start temperature (threshold) and the stop temperature serves to prevent malfunctions from temperature fluctuations.

9. Under Voltage Lockout (UVLO)
Under voltage lockout prevents IC malfunctions that could otherwise occur due to power supply fluctuation at power ON or abrupt power OFF. This system turns OFF each channel output when the VCC voltage becomes lower than 3.4 V. The UVLO detect voltage has 0.1 V hysteresis to prevent malfunctions from power supply fluctuation.
In addition, UVLO works when an internal regulator voltage drops down. The outputs of all channels are turned OFF when VREGD becomes lower than 3.15 V or VREGA becomes lower than 2.4 V. Moreover, the outputs of CH1-6 are turned OFF when HVREG becomes lower than VCC+2.5 V.
The switching frequency
The switching frequency is set by the resistor connected to the RT terminal. Set the frequency with referring fig. 19.

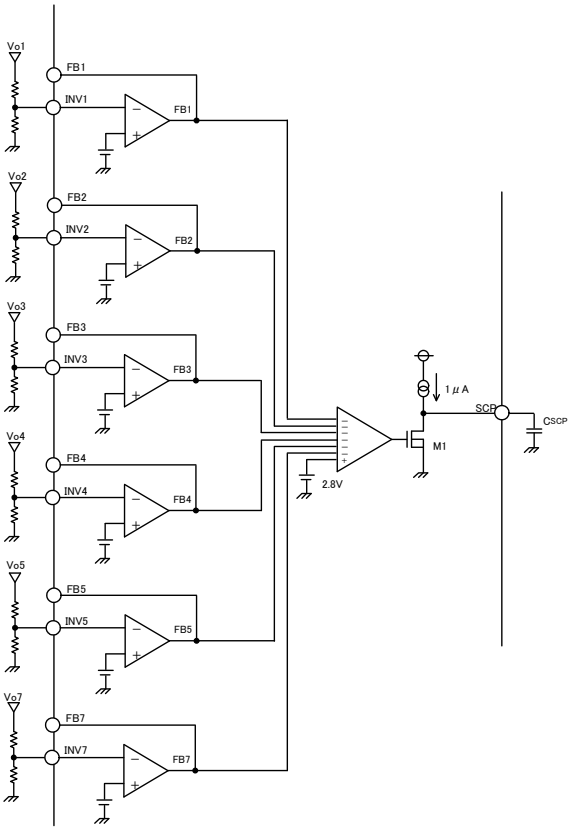


Fig. 8 Block diagram of short circuit protection circuit.

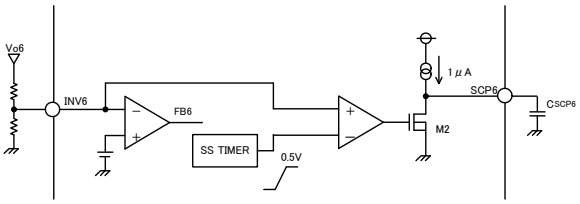


Fig. 9 Block diagram of short circuit protection6 circuit.

10. Selection of output inductor

A combination of the output inductor and the output capacitor form a second-order smoothing filter for switch waveform and provide DC output voltage. If the inductance is low, its package size is minimized, but the penalty is higher ripple current, with lower efficiency and an increase of output noise. Conversely, higher inductance increases the package size, but lowers ripple current, consequently, and suppress the output ripple voltage. Generally, set inductance as that the ripple current is about 20-50 % of their output current. Below equations are the relations of between inductance and ripple current.

(step down) $$L[H]=\frac{(V_{IN}[V]-V_{OUT}[V])}{\Delta I_L[A]}\times\frac{V_{OUT}[V]}{V_{IN}[V]}\times\frac{1}{f_{osc}\,[Hz]}$$

(step up) $$L[H]=\frac{(V_{OUT}[V]-V_{IN}[V])}{\Delta I_L[A]}\times\frac{V_{IN}[V]}{V_{OUT}[V]}\times\frac{1}{f_{osc}\,[Hz]}$$

L: inductance V_{IN}: input voltage
V_{OUT}: output voltage ΔI_L: ripple current
fosc: switching frequency I_{OUT}: output load current

In addition, set larger values than I_{peak} that is calculated from below equation.

(step down) $I_{peak}=I_{OUT}+\Delta I_L/2$

(step up) $I_{peak}=\{I_{OUT}\times(V_{OUT}/V_{IN})/(\eta/100)\}+\Delta I_L/2$ （η: efficiency[%]）

11. Phase Compensation

The components shown will add poles and zeros to the loop gain as given by the following expression:

・CFB adds a pole whose frequency is given by:

$$fp\,(CFB)=\frac{1}{2\pi\times A\times CFB\times(R1//R2)}$$

(A: error amplifier open loop gain)

・RFB adds a zero whose frequency is given by:

$$fz\,(RFB)=\frac{1}{2\pi\times CFB\times RFB}$$

・The output capacitor adds both a pole and a zero to the loop:

$$fz\,(COUT)=\frac{1}{2\pi\times ESR\times COUT}$$

$$fp\,(COUT)=\frac{1}{2\pi\times RL\times COUT}$$

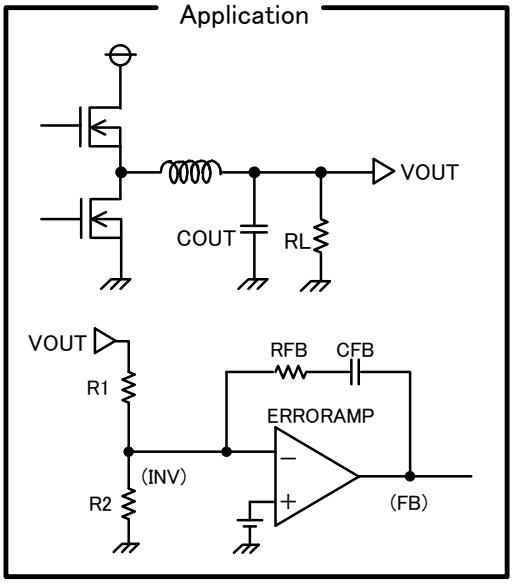


Fig. 10 Phase compensation setting

Where, RL is output load resistance, and ESR is the equivalent series resistance of the output capacitor. CFB forms a pole and a zero. Changing the value of CFB moves the frequency of both the pole and the zero. The CFB pole is typically referred to as the dominant pole, and its primary function is to roll off loop gain and reduce the bandwidth.
The RFB zero is required to add some positive phase shift to offset some of the negative phase shift from the two low-frequency poles. Without this zero, these two poles would cause -180° of phase shift at the unity-gain crossover, which is clearly unstable.

12. Precaution in the layout of Printed Circuit Board

- When switching regulator is operating, large current flow through the path of Power Supply – Inductor – Output Capacitor. In laying a pattern of the board, make this line as short and wide as possible to decrease impedance.
- The switching noise on INV1-7 terminals may cause the output oscillation. To avoid interference of the noise, make the line between voltage divider resistor and INV terminals as shortened as possible and not crossed at switching line.

●Reference data

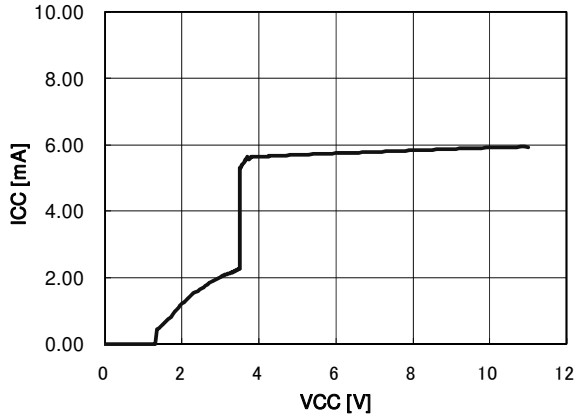


Fig. 11 Circuit current vs supply voltage (all cannels ON)

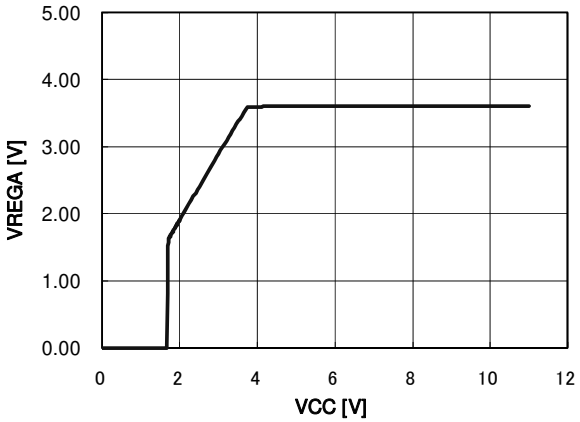


Fig. 12 VREGA vs supply voltage

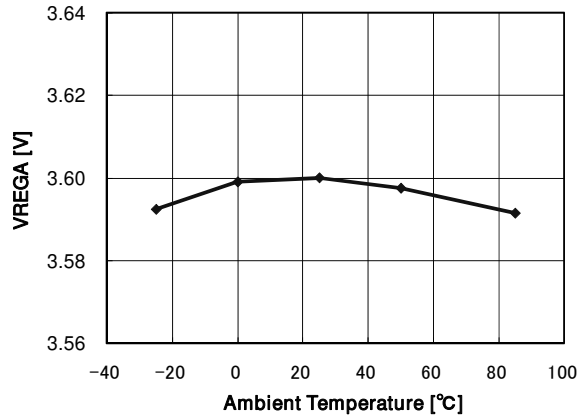


Fig. 13 VREGA vs ambient temperature

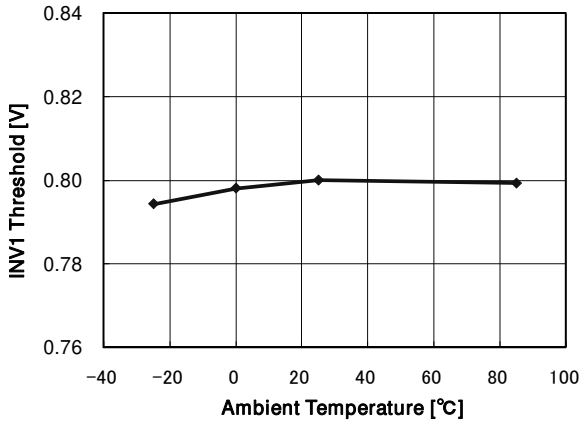


Fig. 14 CH1 ErrorAmp. INV threshold vs ambient temperature

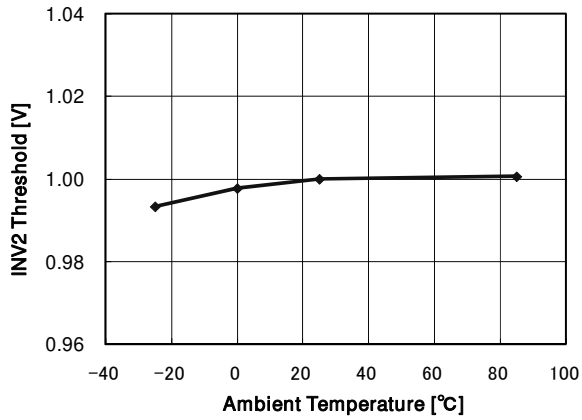


Fig. 15 CH2 ErrorAmp. INV threshold vs ambient temperature

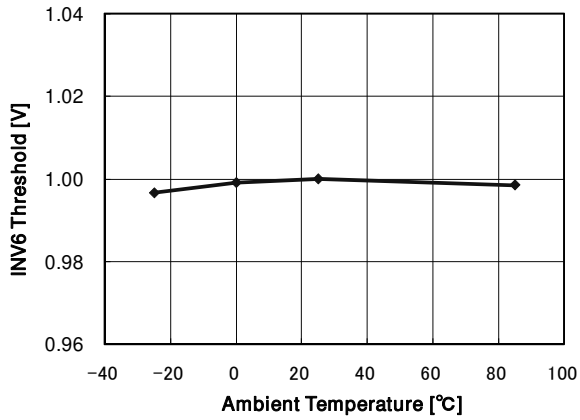


Fig. 16 CH6 ErrorAmp. INV threshold vs ambient temperature

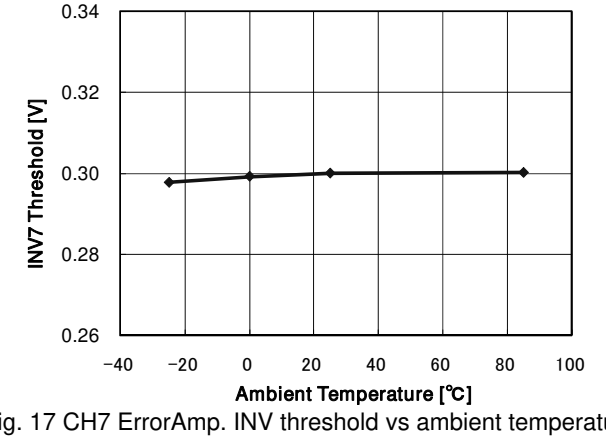


Fig. 17 CH7 ErrorAmp. INV threshold vs ambient temperature

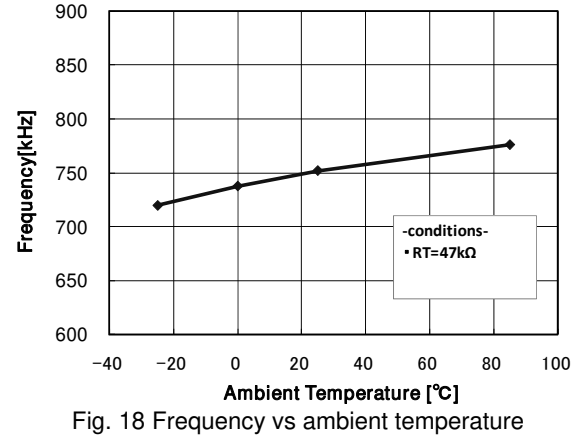


Fig. 18 Frequency vs ambient temperature

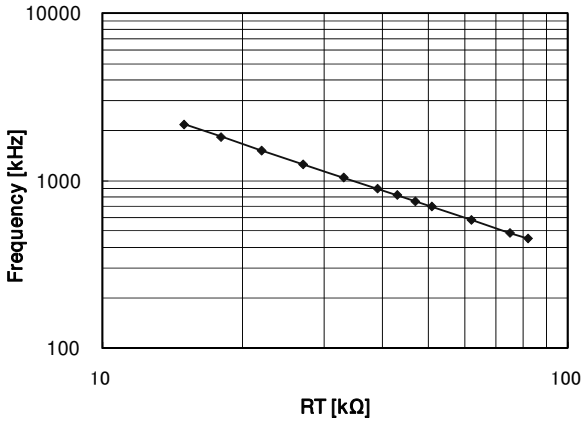


Fig. 19 Switching frequency vs timing resistance

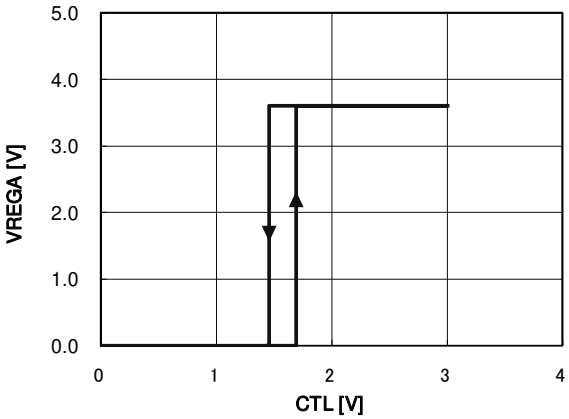


Fig. 20 CTL terminal characteristic

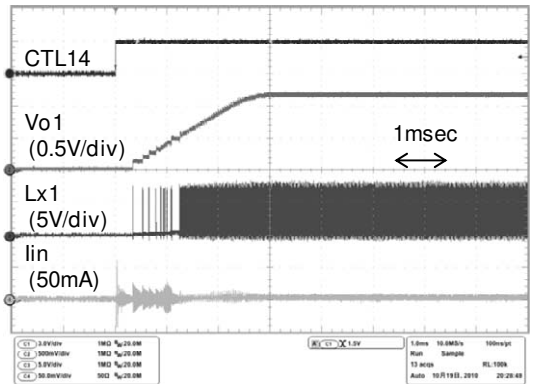


Fig. 21 CH1 startup waveform

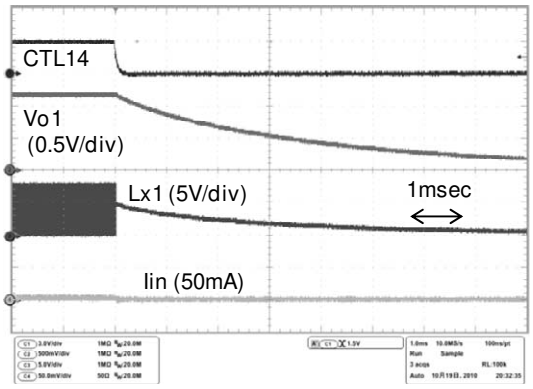


Fig. 22 CH1 stop waveform

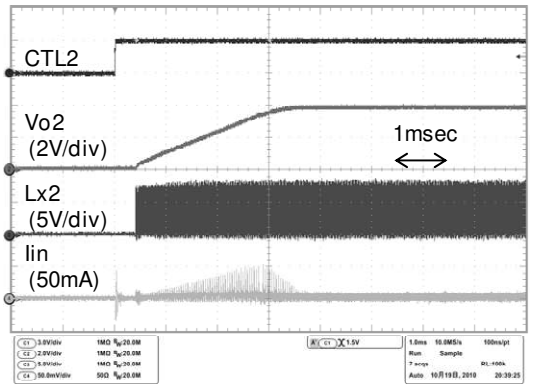


Fig. 23 CH2 startup waveform

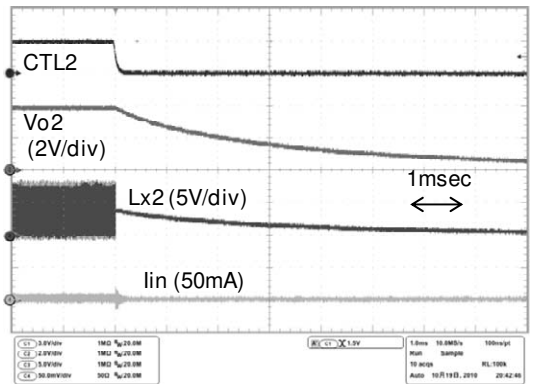


Fig. 24 CH2 stop waveform

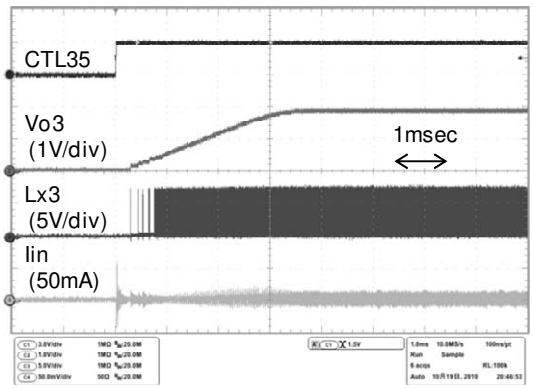


Fig. 25 CH3 startup waveform

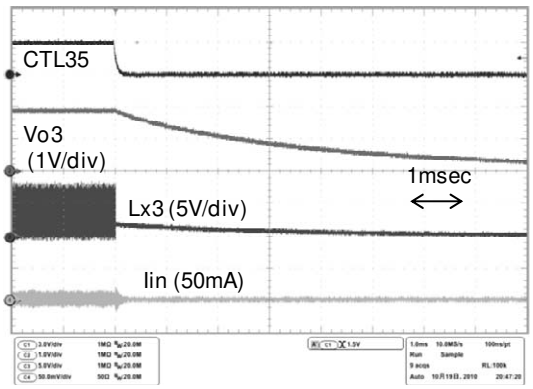


Fig. 26 CH3 stop waveform

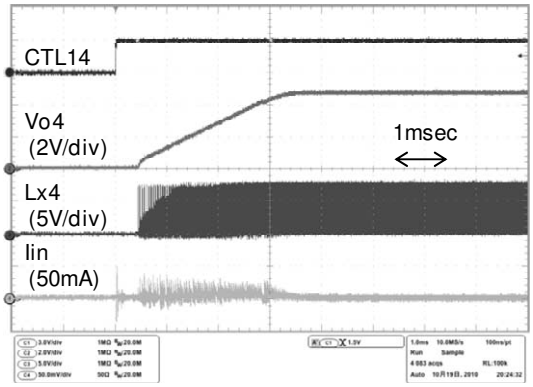


Fig. 27 CH4 startup waveform

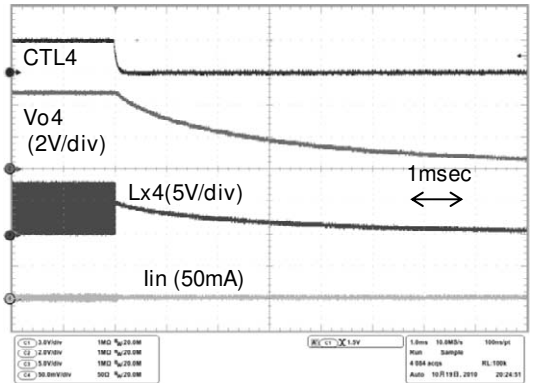


Fig. 28 CH4 stop waveform

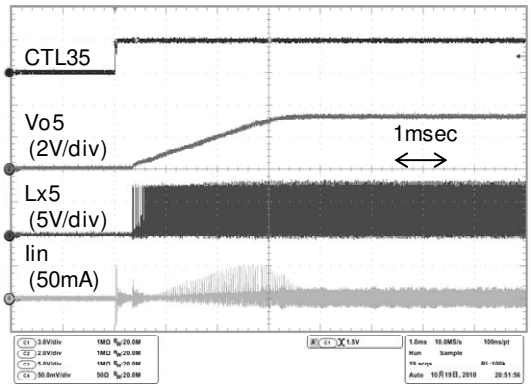


Fig. 29 CH5 startup waveform

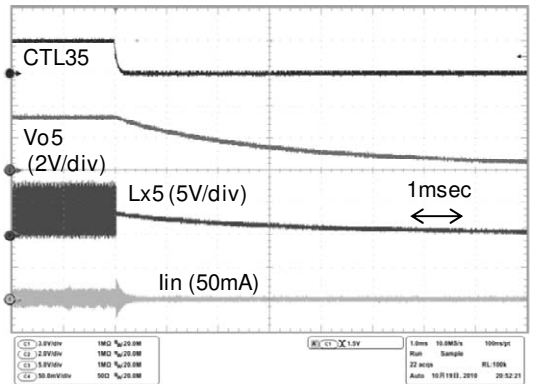


Fig. 30 CH5 stop waveform

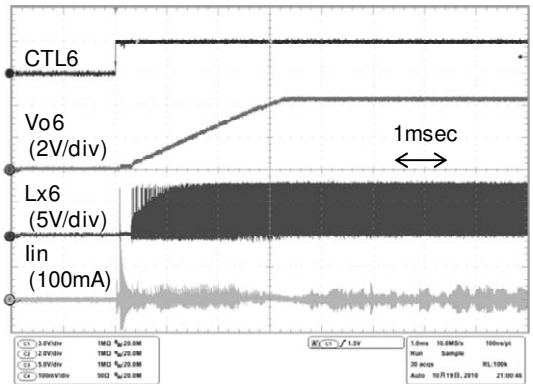


Fig. 31 CH6 startup waveform

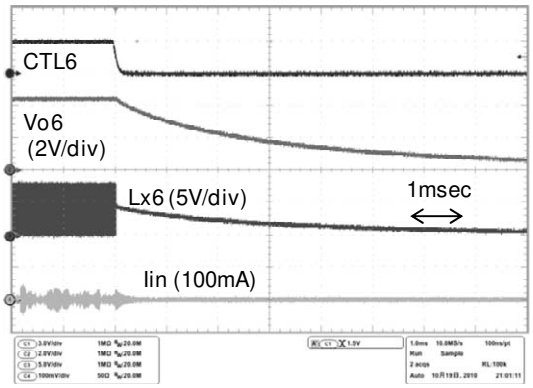


Fig. 32 CH6 stop waveform

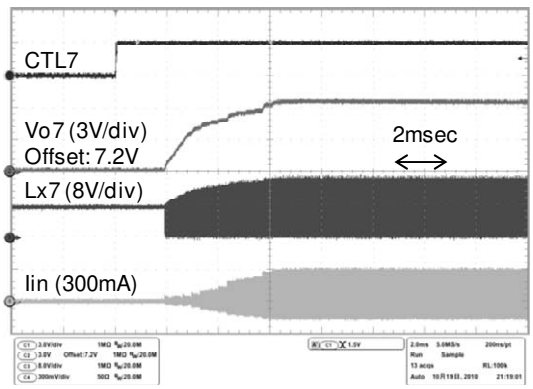


Fig. 33 CH7 startup waveform

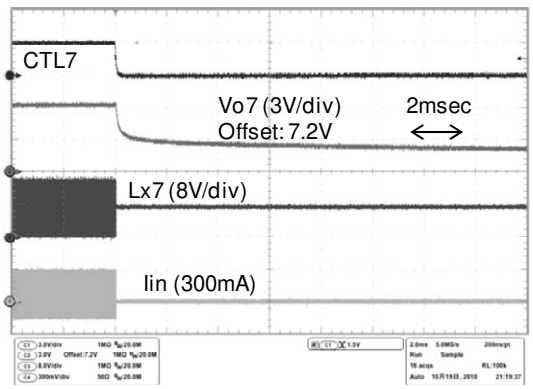


Fig. 34 CH7 stop waveform

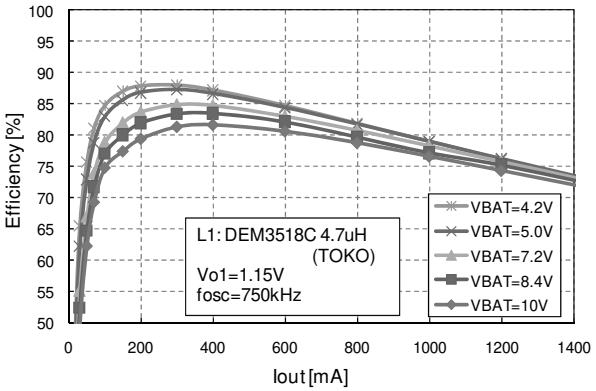


Fig. 35 Efficiency vs load current (CH1)

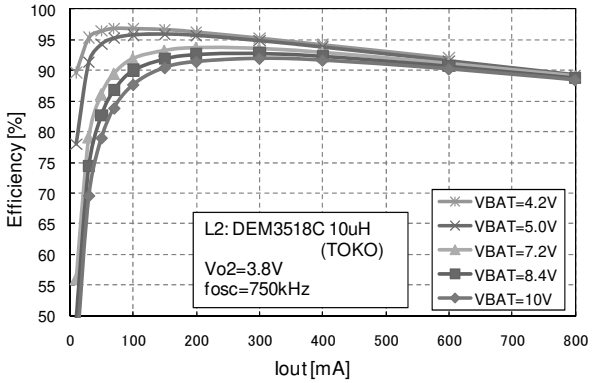


Fig. 36 Efficiency vs load current (CH2)

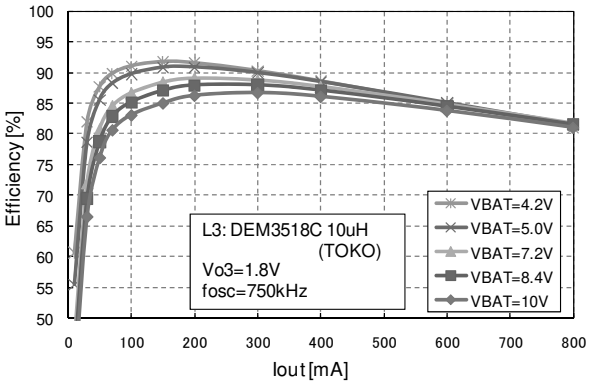


Fig. 37 Efficiency vs load current (CH3)

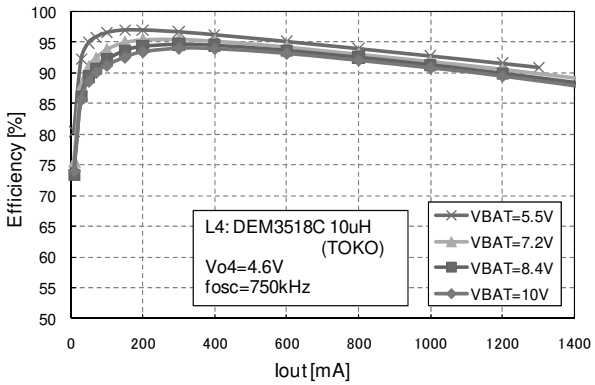


Fig. 38 Efficiency vs load current (CH4)

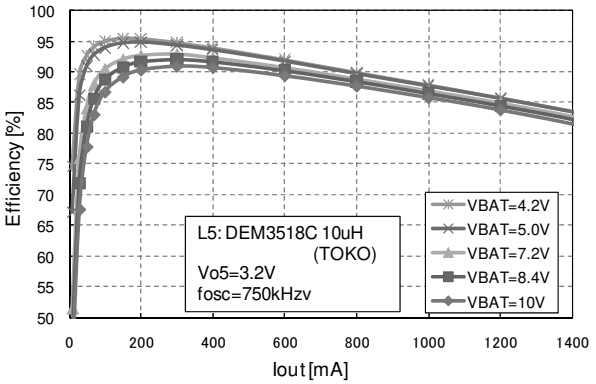


Fig. 39 Efficiency vs load current (CH5)

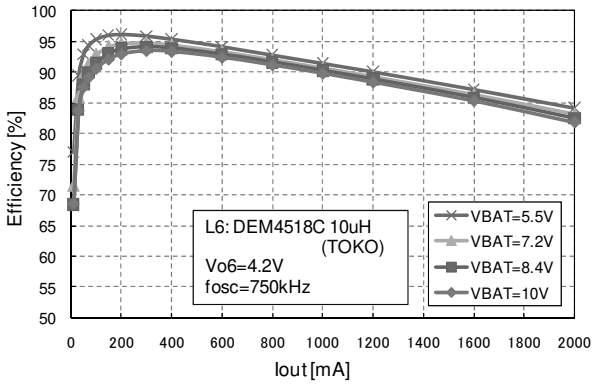


Fig. 40 Efficiency vs load current (CH6)

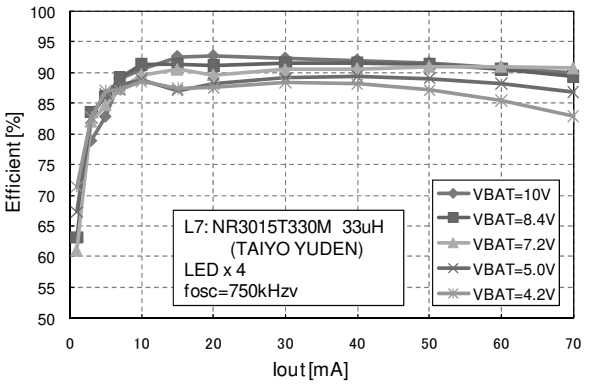


Fig. 41 Efficiency vs load current (CH7)

●Power Dissipation Reduction

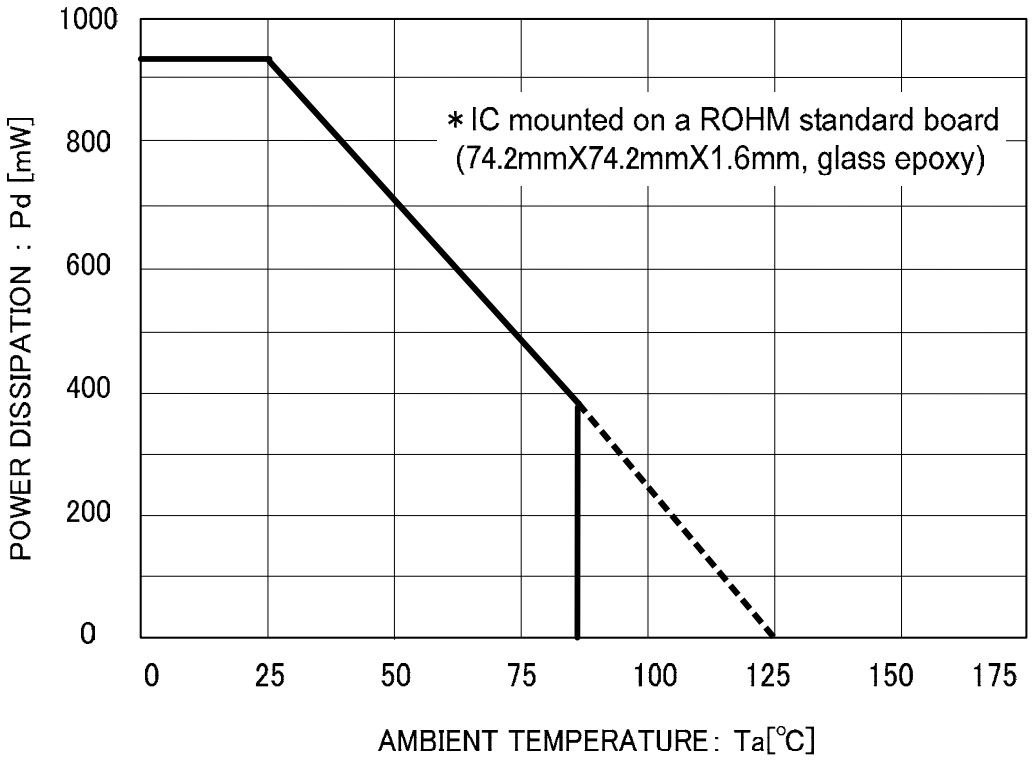
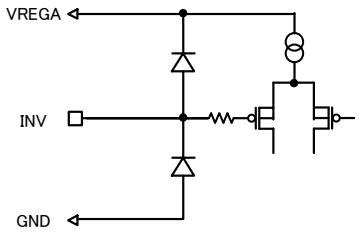
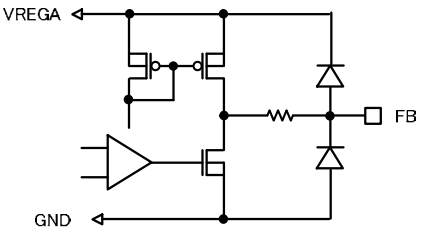
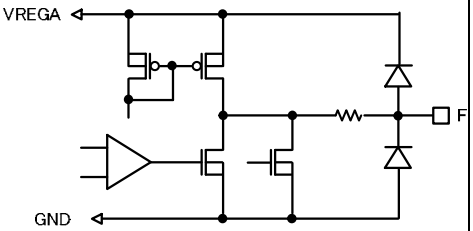
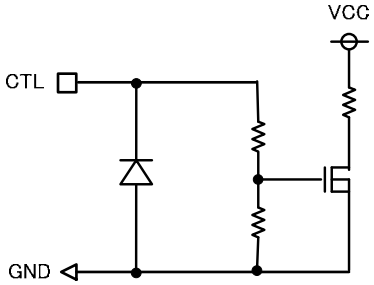
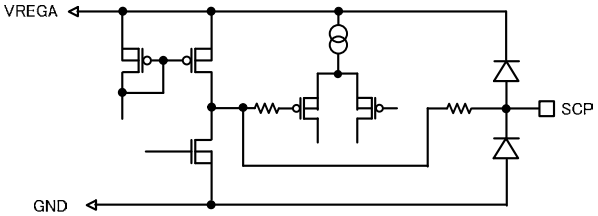
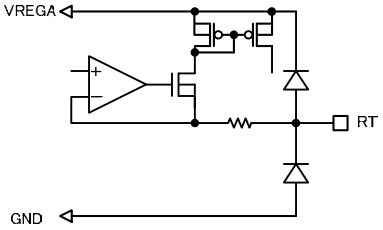
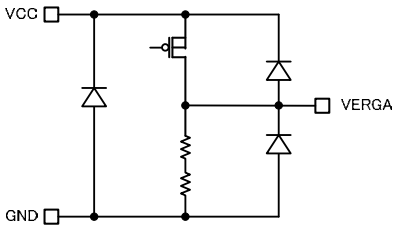
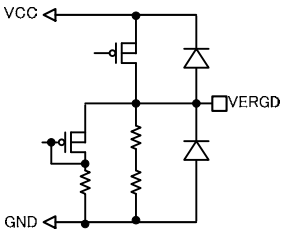
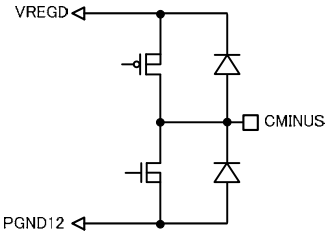
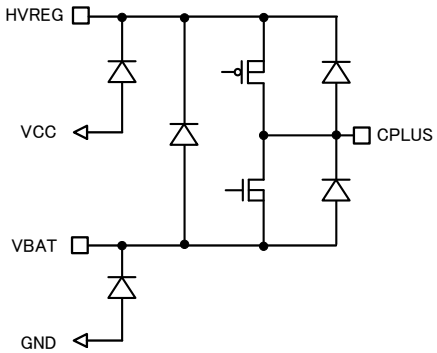
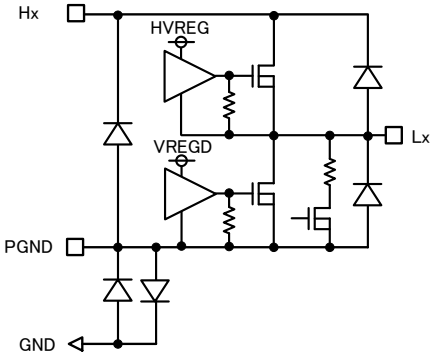
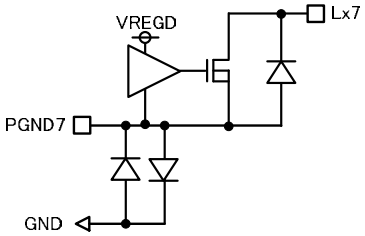
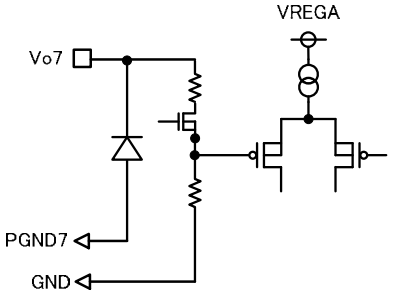


Fig. 42 Power dissipation vs ambient temperature

●PIN equivalent circuit

Pin name	Equivalent circuit	Pin name	Equivalent circuit
INV1 INV2 INV3 INV4 INV5 INV6 INV7		FB1 FB2 FB3 FB4 FB5 FB6	
FB7		CTL14 CTL2 CTL35 CTL6 CTL7	
SCP SCP6			
RT		VCC VREGA GND	
VREGD		CMINUS	

Pin name	Equivalent circuit	Pin name	Equivalent circuit
HVREG CPLUS VBAT		HX1 LX1 HX2 LX2 PGND12 HX3 LX3 HX4 LX4 PGND34 HX5 LX5 HX6 LX6 PGND56	
Lx7 PGND7		Vo7	

●Notes for use

1.) Absolute maximum ratings
This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine (e.g. short mode, open mode). Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential
Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3.) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4.) Inter-pin shorts and mounting errors
Use caution direction and position the IC for mounting on printed circuit boards. Improper mounting may result in damage the IC. In addition, Output-output short and output-power supply/ground short condition may destroy the IC

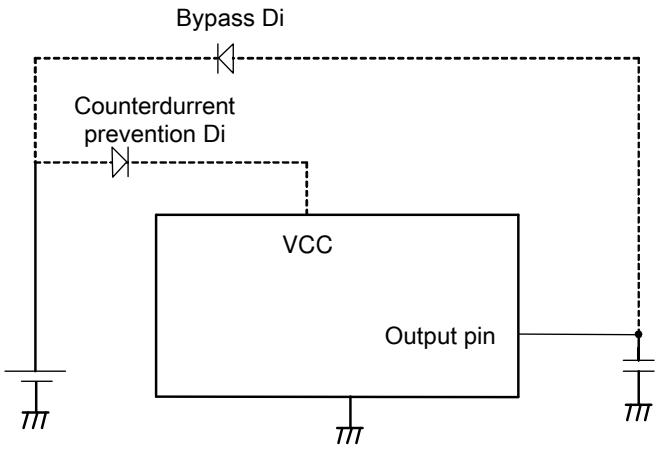
5.) Operation in a strong electromagnetic field
Exposing the IC within a strong electric/magnetic field may cause malfunction.

6.) Common impedance
Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

7.) Voltage of CTL pins
The threshold voltage of CTL pins are 0.4 V and 2.0 V. Standby state is set below 0.4 V while running state is set beyond 2.0 V. The region between 0.4 V and 2.0 V is not recommended and may cause improper operation.
The rise and fall time must be under 10 msec. In case to put capacitors to CTL pins, it is recommended using under 0.01μF.
The maximum permissible voltage of CTL7 is 5.5 V. CTL7 pin should not be connected to VCC voltage.
Turn on any CTL1-6 and wait more than 500 usec before turn on CTL7.

8.) Thermal shutdown circuit (TSD circuit)
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

9.) Applications with modes that VCC/GND and other pins except Lx and HVREG potential are reversed may cause damage internal IC circuits. In addition, modes that each pins sink current may also cause damage the circuits. Therefore, It is recommended to insert a diode to prevent back current flow or bypass diodes.



10.) Rush current at the time of power supply injection.
An IC which has plural power supplies could have momentary rush current at the time of power supply injection. Please take care about power supply coupling capacity and width of power Supply and GND pattern wiring

11.) Please use it so that VCC and PVCC terminal should not exceed the absolute maximum ratings. Ringing might be caused by L element of the pattern according to the position of the input capacitor, and ratings be exceeded. Please will assume the example of the reference ,the distance of IC and capacitor, use it by 5.0mm or less when thickness of print pattern are 35um, pattern width are 1.0mm.

12.) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

13.) Thermal fin.
There is no problem in the operating of IC even if the thermal fin on the back of package doesn't connect anywhere.
But it is recommended to connect GND on the PCB board for radiation.

14.) IC Terminal Input
This IC is a monolithic IC that has a P- board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed. For example, an application where a resistor and transistor are connected to a terminal (shown in Fig.43)

- ○When GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode
- ○When GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the N layers of other elements in the proximity of the aforementioned parasitic diode.

Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.

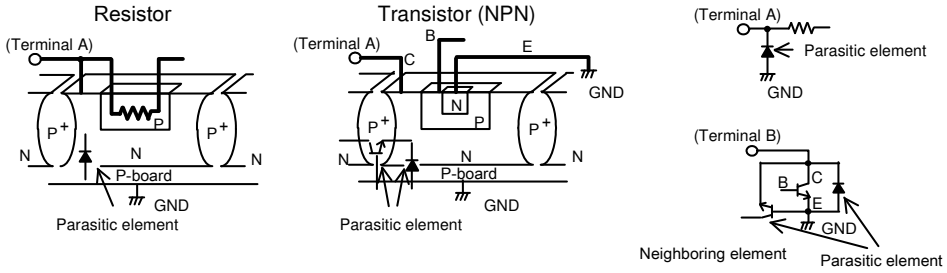


Fig. 43 Simple Structure of Bipolar IC (Sample)

●Ordering part number

B	D	8	3	5	5	M	W	V	-	E	2

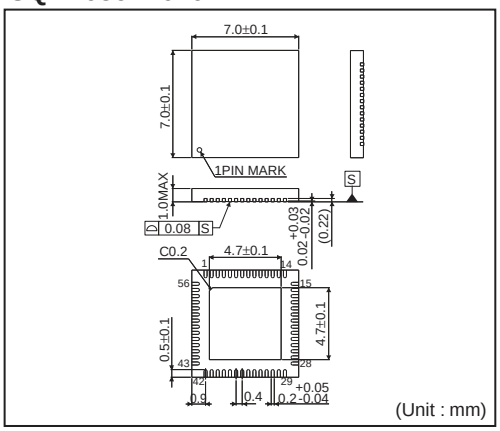
Part No.

Part No.

Package
MWV: UQFN056V7070

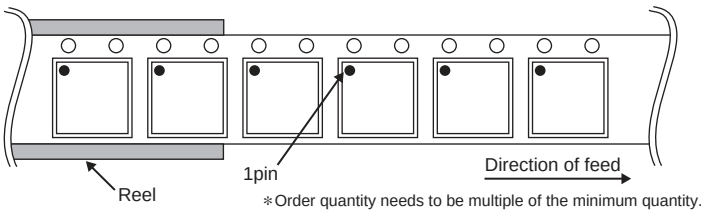
Packaging and forming specification
E2: Embossed tape and reel

UQFN056V7070



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:

2. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the information contained in this document.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.