



256K x 16 Static RAM

Features

- **High speed**
— 55 ns and 70 ns availability
- **Low voltage range:**
— 1.65V–1.95V
- **Pin-compatible w/ CY62147BV18**
- **Ultra-low active power**
— Typical Active Current: 0.5 mA @ f = 1 MHz
— Typical Active Current: 2 mA @ f = f_{max} (70 ns speed)
- **Low standby power**
- **Easy memory expansion with \overline{CE} and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

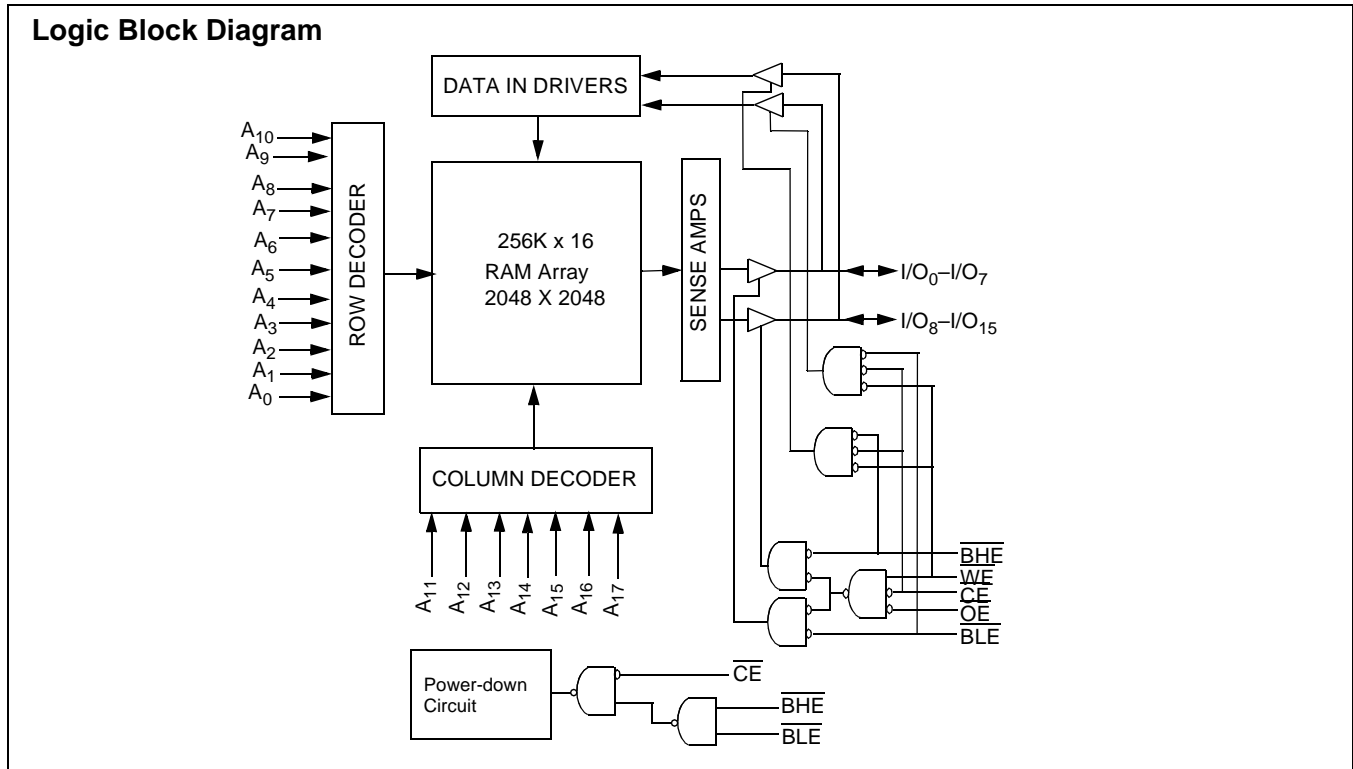
The CY62147CV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly

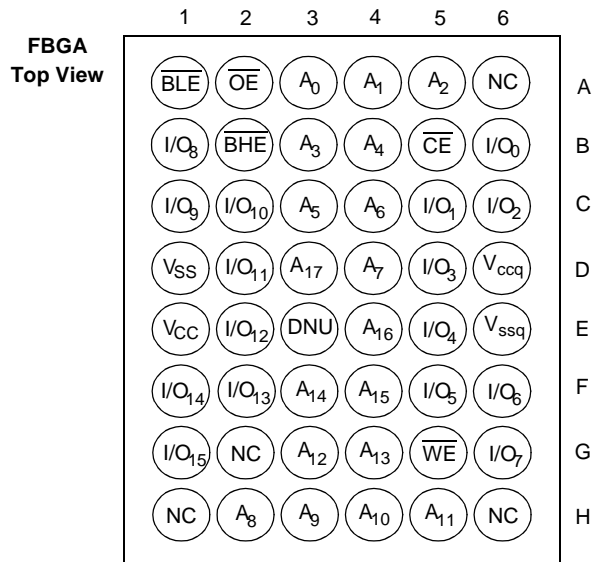
reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE} HIGH or both \overline{BLE} and \overline{BHE} are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62147CV18 is available in a 48-ball FBGA package.



Pin Configuration^[1, 2]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.2V to +2.4V
DC Voltage Applied to Outputs in High-Z State ^[3]	-0.2V to V _{CC} + 0.2V

DC Input Voltage ^[3]	-0.2V to V _{CC} + 0.2V
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	> 2001V (per MIL-STD-883, Method 3015)
Latch-up Current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62147CV18	Industrial	-40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
	V _{CC} (min.)	V _{CC} (typ.) ^[4]	V _{CC} (max.)		Operating (I _{CC})				Standby (I _{SB2})	
					f = 1 MHz		f = f _{max}		Typ. ^[4]	Max.
					Typ. ^[4]	Max.	Typ. ^[4]	Max.		
CY62147CV18	1.65V	1.80V	1.95V	55 ns	0.5 mA	3 mA	2.5 mA	7 mA	1 μA	10 μA
				70 ns	0.5 mA	3 mA	2 mA	6 mA		

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62147CV18-55			CY62147CV18-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA, V _{CC} = 1.65V	1.4			1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA, V _{CC} = 1.65V			0.2			0.2	V
V _{IH}	Input HIGH Voltage		1.4		V _{CC} + 0.2V	1.4		V _{CC} + 0.2V	V
V _{IL}	Input LOW Voltage		-0.2		0.4	-0.2		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA

Notes:

- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
- V_{IL}(min) = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ) Typ, T_A = 25°C.

Electrical Characteristics Over the Operating Range (continued)

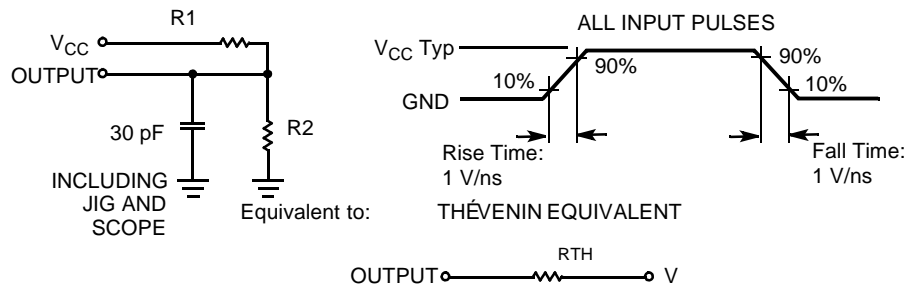
Parameter	Description	Test Conditions	CY62147CV18-55			CY62147CV18-70			Unit
			Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		+1	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$		2.5	7		2	6	mA
		$f = 1 \text{ MHz}$	$V_{CC} = 1.95V$ $I_{OUT} = 0 \text{ mA}$ CMOS levels		0.5	3		0.5	3
I_{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE, and BLE)		1	10		1	10	μA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 1.95V$							

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = V_{CC}(typ)$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	55	$^\circ C/W$
Θ_{JC}	Thermal Resistance (Junction to Case) ^[5]		16	$^\circ C/W$

AC Test Loads and Waveforms


Parameters	1.8V	Unit
R1	13500	Ohms
R2	10800	Ohms
R_{TH}	6000	Ohms
V_{TH}	0.80	Volts

Data Retention Characteristics (Over the Operating Range)

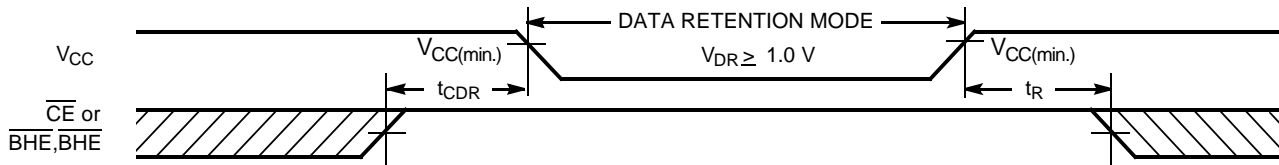
Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		1.95	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	8	μA

Note:

- Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics (Over the Operating Range) (continued)

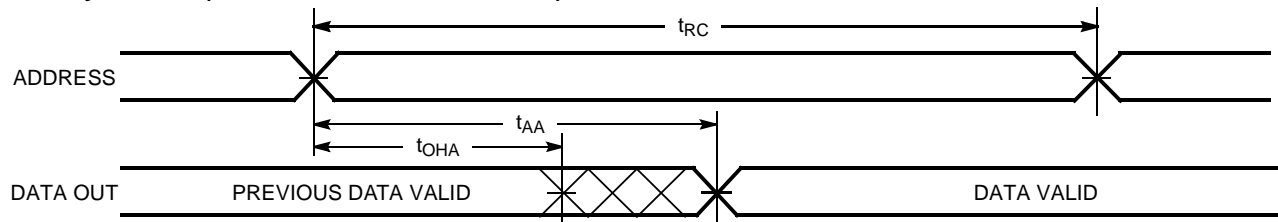
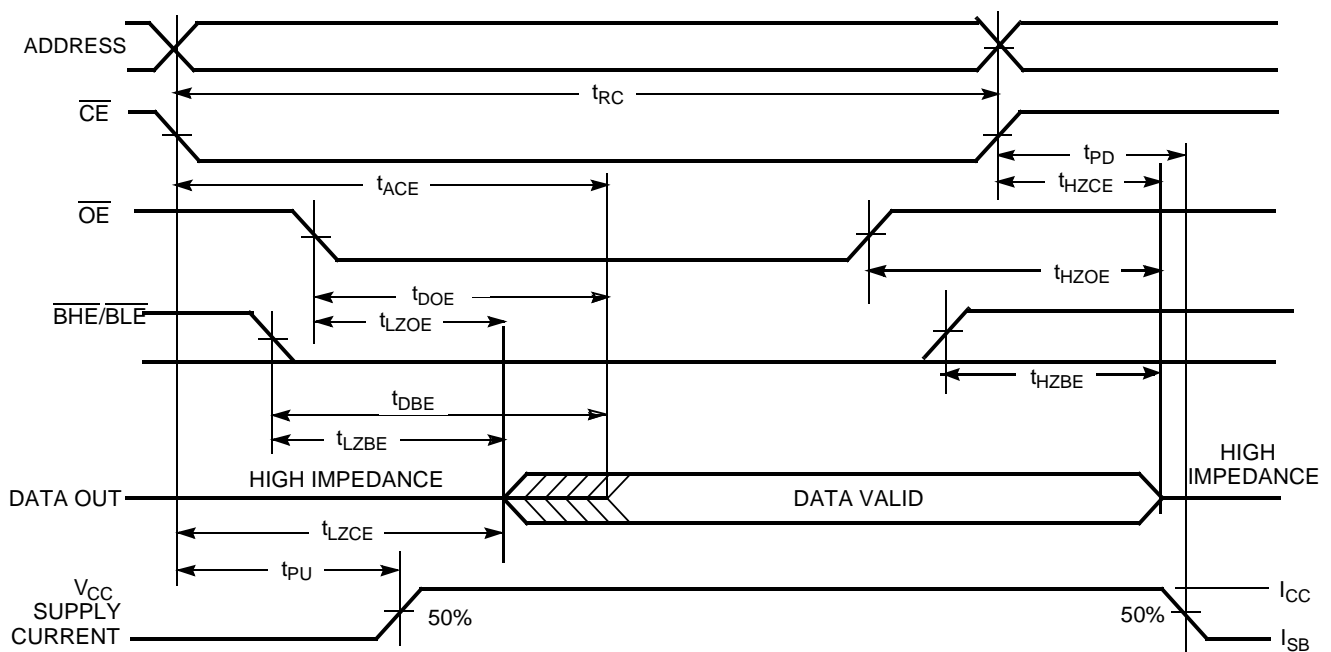
Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[6]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[7]

Switching Characteristics Over the Operating Range ^[8]

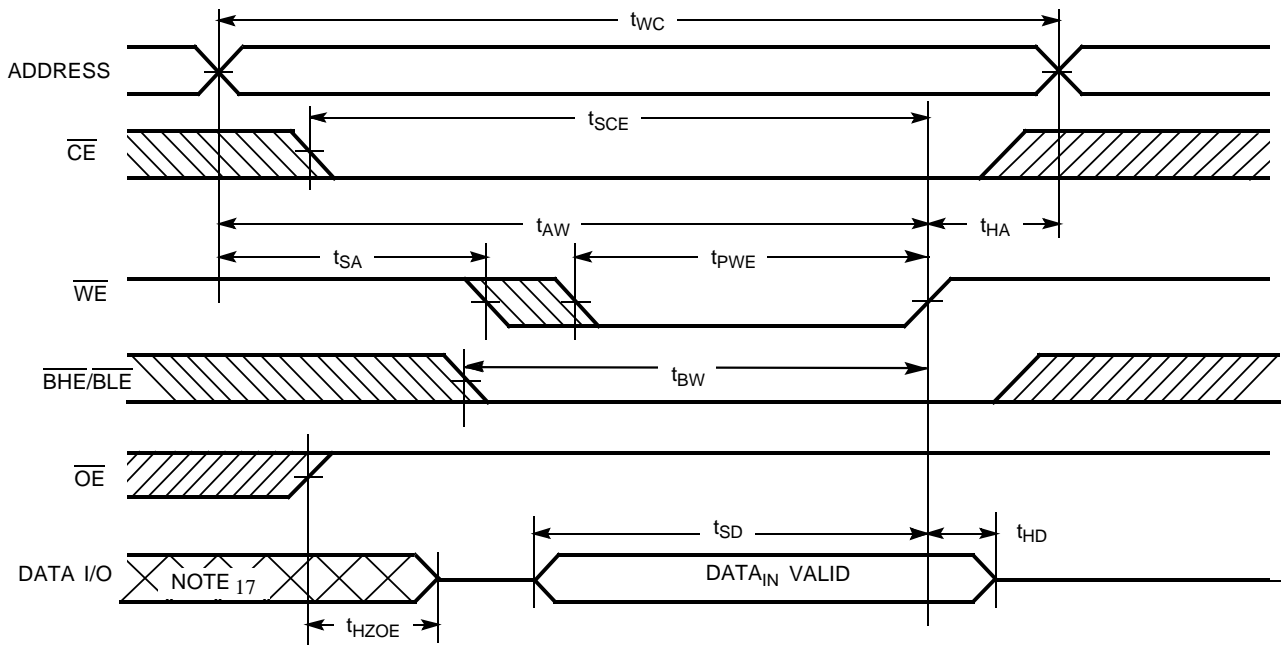
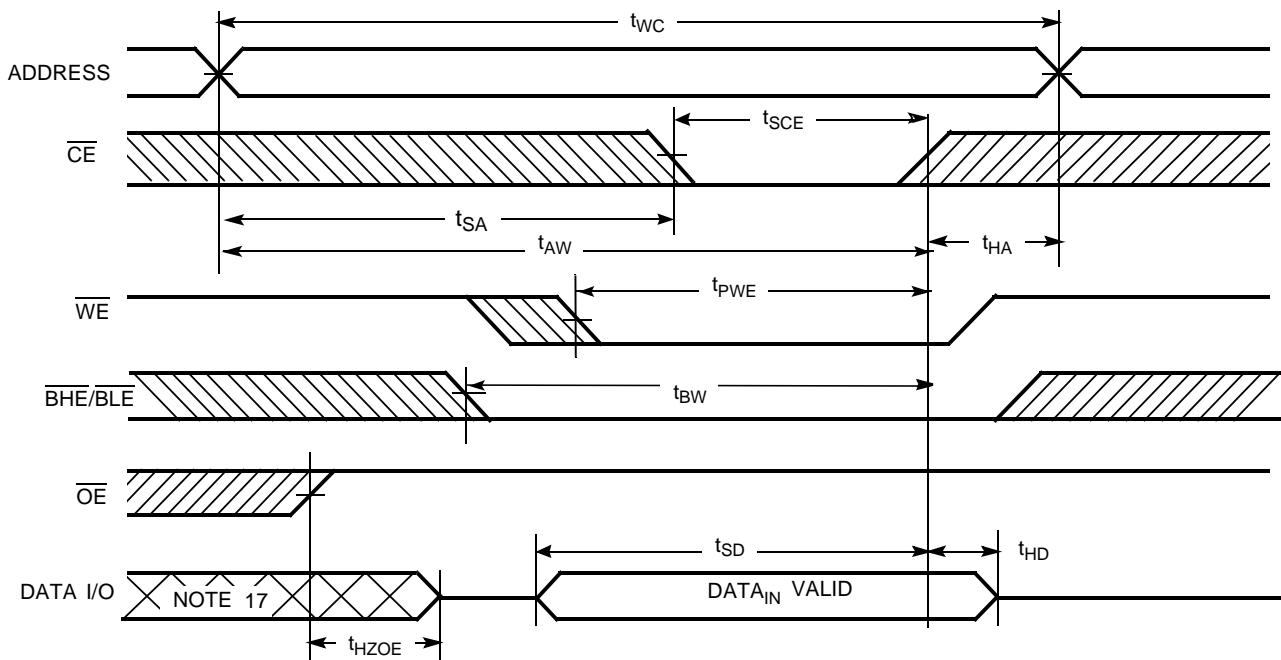
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	CE LOW to Data Valid		55		70	ns
t_{DOE}	OE LOW to Data Valid		25		35	ns
t_{LZOE}	OE LOW to Low-Z ^[9]	5		5		ns
t_{HZOE}	OE HIGH to High-Z ^[9, 10]		20		25	ns
t_{LZCE}	CE LOW to Low-Z ^[9]	5		10		ns
t_{HZCE}	CE HIGH to High-Z ^[9, 10]		20		25	ns
t_{PU}	CE LOW to Power-up	0		0		ns
t_{PD}	CE HIGH to Power-down		55		70	ns
t_{DBE}	BLE/BHE LOW to Data Valid		55		70	ns
t_{LZBE}	BLE/BHE LOW to Low-Z ^[9]	5		5		ns
t_{HZBE}	BLE/BHE HIGH to High-Z ^[9, 10]		20		25	ns
Write Cycle^[11]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	CE LOW to Write End	40		60		ns
t_{AW}	Address Set-up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	40		50		ns
t_{BW}	BLE/BHE LOW to Write End	40		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	WE LOW to High-Z ^[9, 10]		15		25	ns
t_{LZWE}	WE HIGH to Low-Z ^[9]	5		10		ns

Notes:

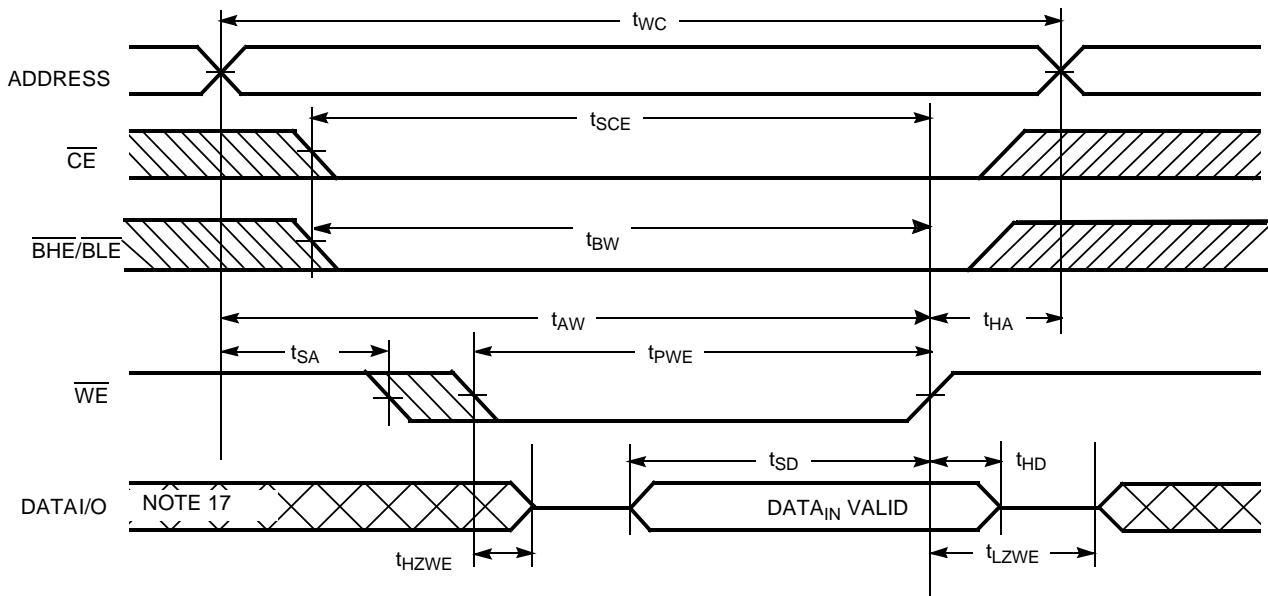
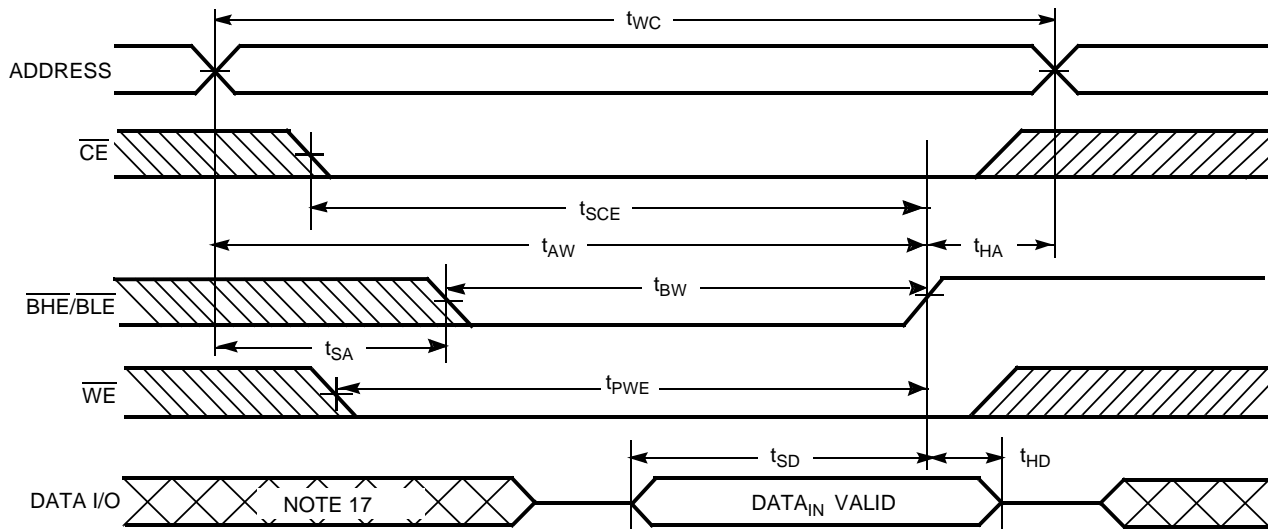
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.
- \overline{BHE} , \overline{BLE} is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .
- Test conditions assume signal transition time of 3ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of \overline{WE} , $CE = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled) ^[12, 13]

Read Cycle No. 2 (\overline{OE} Controlled) ^[13, 14]

Notes:

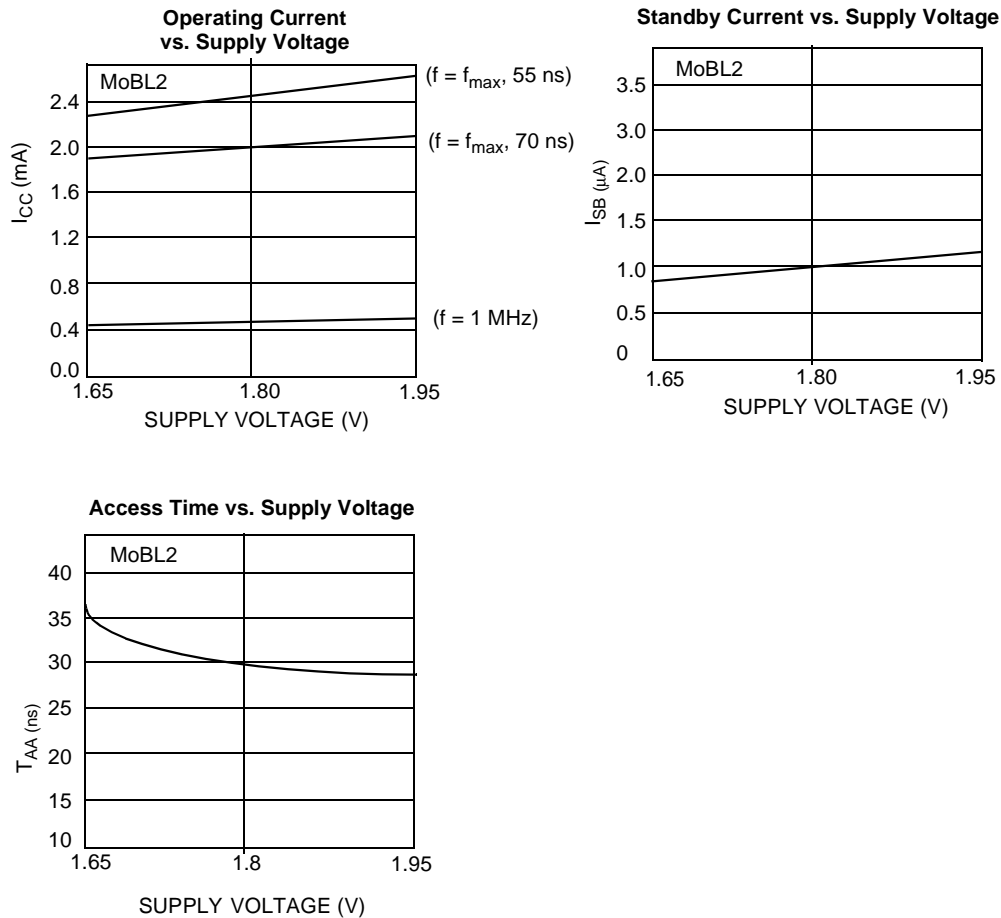
12. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE} , \overline{BHE} , \overline{BLE} , transition LOW.

Switching Waveforms
Write Cycle No. 1 (\overline{WE} Controlled) [11, 15, 16]

Write Cycle No. 2 (\overline{CE} Controlled) [11, 15, 16]

Notes:

15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms
Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[16]

Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[16]


Typical DC and AC Characteristics (Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC\ Typ}$, $T_A = 25^\circ C$.)



Truth Table

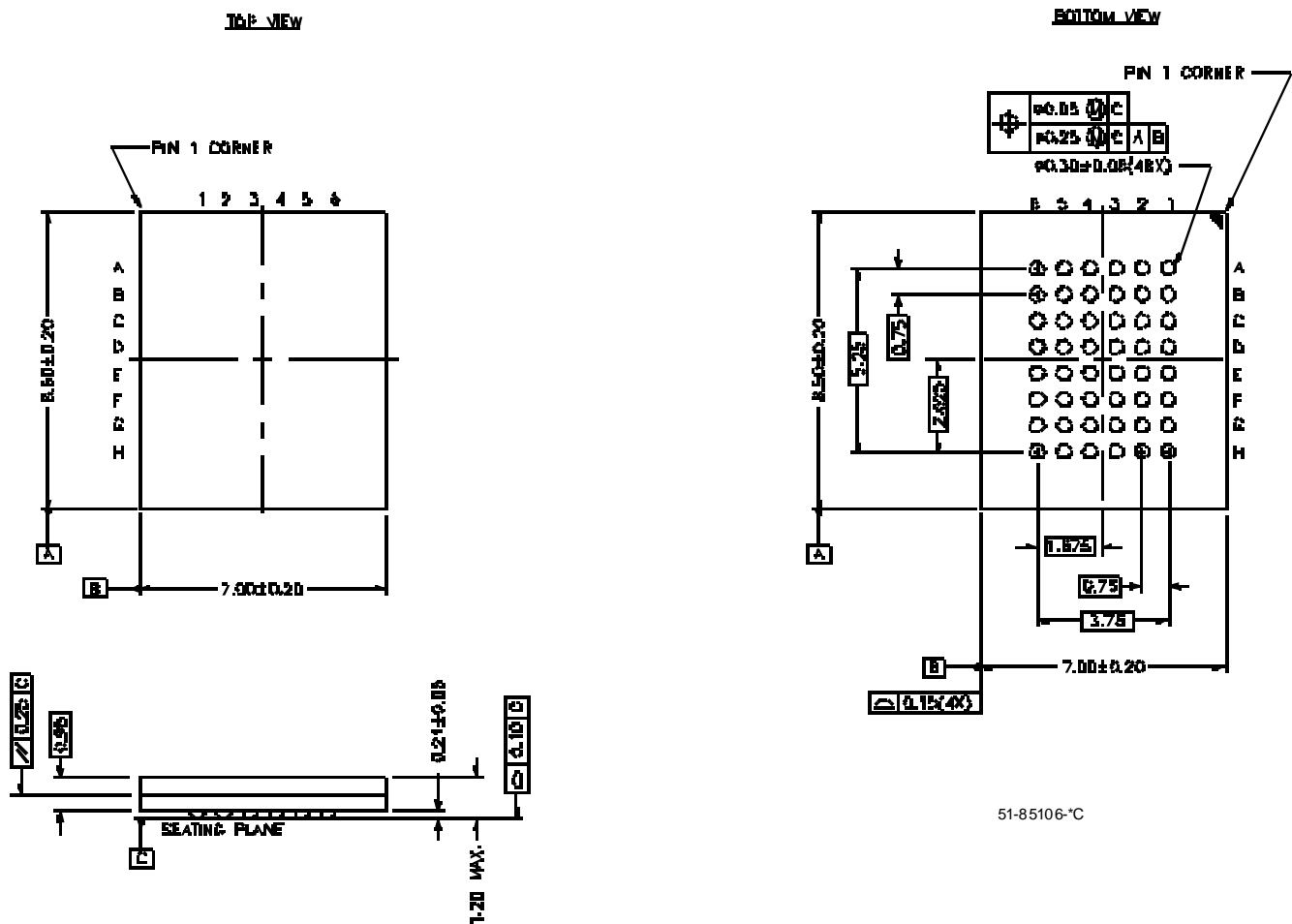
\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	H	H	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 - I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 - I/O_7); I/O_8 - I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 - I/O_{15}); I/O_0 - I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 - I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 - I/O_7); I/O_8 - I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 - I/O_{15}); I/O_0 - I/O_7 in High-Z	Write	Active (I_{CC})

Ordering Information

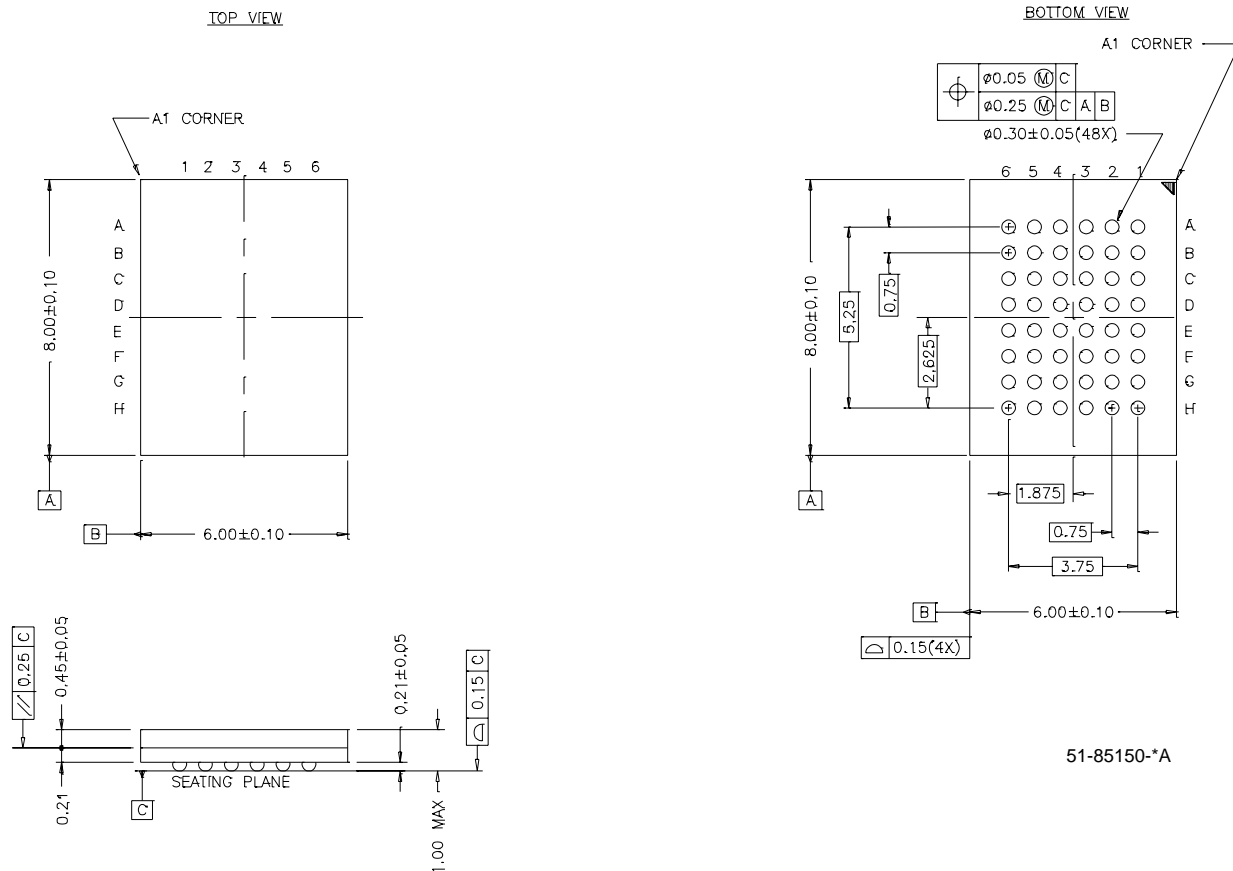
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62147CV18LL-70BAI	BA48B	48-ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62147CV18LL-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62147CV18LL-55BAI	BA48B	48-ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62147CV18LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams

48-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA48B



51-85106-C

Package Diagrams (continued)
48-Lead VFBGA (6 x 8 x 1 mm) BV48A


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Document Title: CY62147CV18 MoBL2™ 256K x 16 Static RAM				
Document Number: 38-05011				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106265	5/7/01	HRT/MGN	New Data Sheet
*A	108941	08/24/01	MGN	From Preliminary to Final
*B	110573	11/02/01	MGN	Improved I _{SB} Typ. from 1.5 μA to 1 μA. Improved Typical DC and AC Characteristics graphs. Improved Switching Characteristics: t _{OHA} , t _{LZCE} . Added preliminary package diagram of BV48A. Format standardization
*C	115864	09/04/02	MGN	Removed Preliminary status for BV package