TPS61175EVM-588

This user's guide describes the characteristics, operation, and use of the TPS61175EVM-588 evaluation module (EVM). This EVM contains the Texas Instruments TPS61175 high-efficiency boost converter that is configured in a split-rail, single-ended primary inductance converter (SEPIC) to provide a regulated 12-V output voltage from an input voltage ranging from 9-V to 24-V. This user's guide includes a schematic diagram, board layout, bill of materials, and test data.

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1 Introduction

This section contains background information for the TPS61175EVM-588 evaluation module.

1.1 Background

This TPS61175EVM-588 SEPIC is designed to boost and buck input voltages ranging from 9-V to 24-V to a 12-V output. The goal of the EVM is to facilitate evaluation of the split-rail TPS61175 SEPIC power supply solution. The EVM uses the TPS61175 adjustable output boost converter, external schottky diode, input, output, and flying capacitors, a coupled inductor, split-rail circuitry, and the appropriate feedback and compensation components to provide a regulated 12-V.

1.2 Performance Specification Summary

Table 1 provides a summary of the TPS61775EVM-588 performance specification. All specifications are given for ambient temperature of 25°C.

Table 1. Performance Specification Summary for V_{IN} = 9.0 V

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		5	9	18	V
$I_{IN(AVG)}$	Average input current	I_O = 750 mA, V_{IN} = 9V			1.3	A
f_{SW}	Switching frequency			750		kHz
OUTPUT CHARACTERISTICS						
V_O	Output voltage		11 (1)	12	13 (1)	V
	Line regulation	8.5 V < V_{IN} < 9.5 V at I_O = 400 mA			1%	$\Delta V_O/\Delta V_{IN}$
	Load regulation	V_{IN} = 9 V, 50 mA < I_O < 375 mA			1.5%	$\Delta V_O/\Delta I_O$
$\Delta V_{O(PP)}$	Output voltage ripple	I_O = 750 mA, V_{IN} = 9V			150	mV_{PP}
I_O	Output current	V_{IN} = 9V	1		750	mA
TRANSIENT RESPONSE						
ΔI_O	Load step	V_{IN} = 9V		0.325		A
ΔV_O	V_O undershoot	V_{IN} = 9V		0.4		V

(1) Minimum and maximum values include 1% resistor tolerance as well as IC feedback reference voltage tolerance.

Table 2. Performance Specification Summary for V_{IN} = 24.0 V with Split Rail Circuitry Installed

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		9	18	24	V
$I_{IN(AVG)}$	Average input current	$_O$ = 750 mA, V_{IN} = 24V			0.5	A
f_{SW}	Switching frequency			750		kHz
OUTPUT CHARACTERISTICS						
V_O	Output voltage		23 (1)	24	25 (1)	V
	Line regulation	23 V < V_{IN} < 24 V at I_O = 750 mA			1%	$\Delta V_O/\Delta V_{IN}$
	Load regulation	V_{IN} = 12 V, 50 mA < I_O < 375 mA			1%	$\Delta V_O/\Delta I_O$
$\Delta V_{O(PP)}$	Output voltage ripple	I_O = 750 mA, V_{IN} = 24V			150	mV_{PP}
I_O	Output current	V_{IN} = 24V	1		0.750	A
TRANSIENT RESPONSE						
ΔI_{TRAN}	Load step	V_{IN} = 24V		0.325		A
ΔV_{TRAN}	V_O undershoot	V_{IN} = 24V		250		mV

(1) Minimum and maximum values include 1% resistor tolerance as well as IC feedback reference voltage tolerance

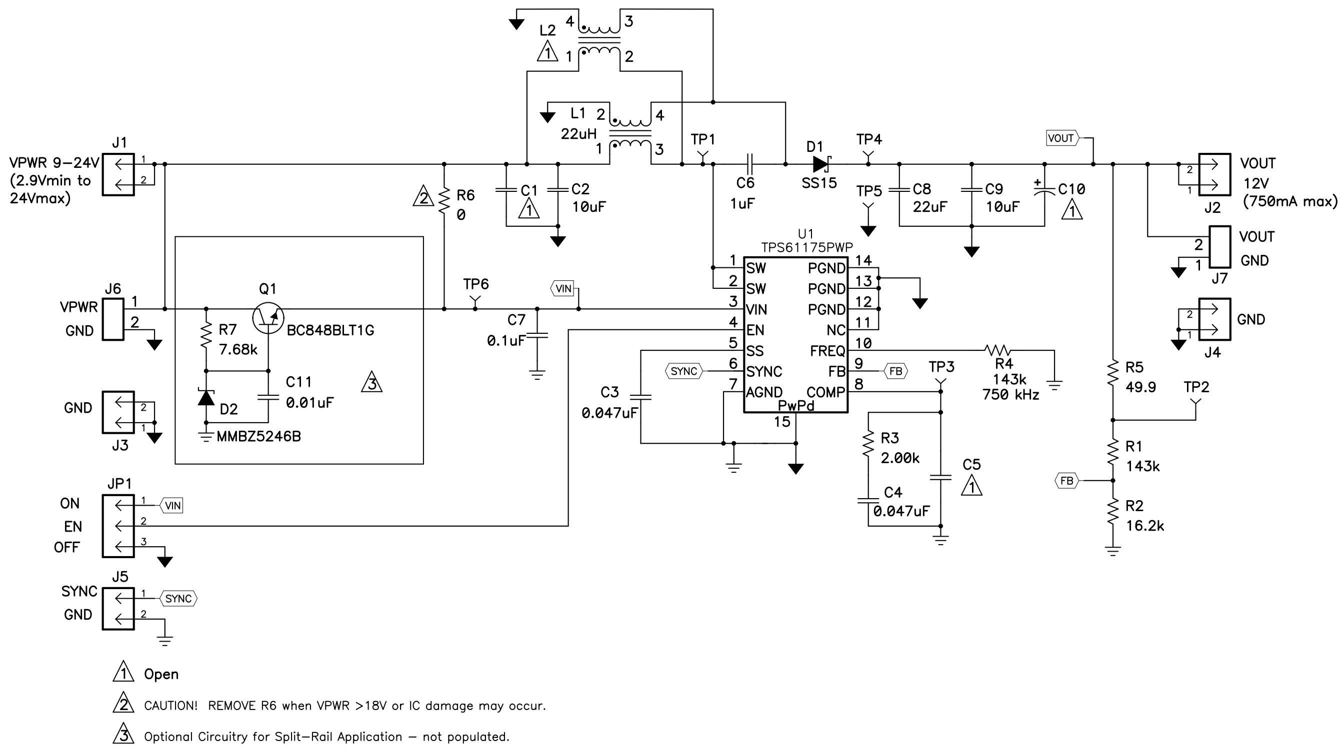
1.3 Modifications

The absolute maximum input voltage for the TPS61175 IC and this EVM is 18V. Do not apply more 18V to this EVM unless R6 is removed or IC damage may occur. However, split-rail circuitry can be added to allow the power stage voltage to reach higher levels. The TPS61175EVM-588 contains unpopulated pads for a discrete linear regulator to be included, which can extend the input voltage up to 24V. Table 3 documents the necessary components.

1.4 Design Example

For a guide to designing a split-rail SEPIC converter, refer to application note (SLVA384).

2 Schematic



3 Setup and Test Results

This section describes how to properly connect, set up, and use the TPS61175EVM-588.

3.1 Input/Output Connections

The connection points are described in the following paragraphs.

3.1.1 J1 – V_{IN}

This header is the positive connection to the input power supply used for lower (< 1A) input currents. Twist the leads to the input supply, and keep them as short as possible.

3.1.2 J2 – V_{OUT}

This header is the positive output for the device used for lower (< 1A) output currents. Connect the positive lead of the load and/or output multimeter to this point

3.1.3 J3 – GND

This header is the return connection for the input power supply used for lower (< 1A) input currents.

3.1.4 J4 – GND

This header is the return connection for the load and/or output multimeter used for lower (< 1A) output currents.

3.1.5 J5 pin 1 – SYNC

This pin is available for the application of an external clock synchronization signal. Make sure that the frequency of the clock signal is within the range in Table 1. This pin cannot be left floating, so use a shorting jumper to short the SYNC pin to GND if not used.

3.1.6 J5 pin 2 – GND

This pin is the return connection for the external synchronization signal

3.1.7 J6 pin 1 – V_{IN}

This is the positive connection for the input power supply used for higher (> 1A) input currents.

3.1.8 J6 pin 2 – GND

This is the return connection to the input power supply used for higher (> 1A) input currents. Twist the leads to the input supple, and keep them as short as possible.

3.1.9 J7 pin 1 – GND

This is the return connection for the load used for higher (> 1A) output currents.

3.1.10 J7 pin 2 – V_{OUT}

This is the positive connection for the load used for higher (> 1A) output currents.

3.1.11 JP1 – ENABLE

Installing this jumper ties the enable pin to either the input voltage (on) or ground (off). If left unconnected, the enable pin's internal pull down resistor disables the IC.

3.1.12 TP1 – SW Node

Test point for the switch node of the boost converter.

3.1.13 TP2 – Loop Response

Test point for control loop response measurements.

3.1.14 TP3 – Comp Pin

Test point for the compensation network.

3.1.15 TP4 and TP5 – Output Ripple

Test points for measuring the output ripple voltage.

3.1.16 TP6 – V_{IN}

Test point for measuring the input voltage.

3.2 Test Results

The following section shows the test results of the TPS61775EVM-588.

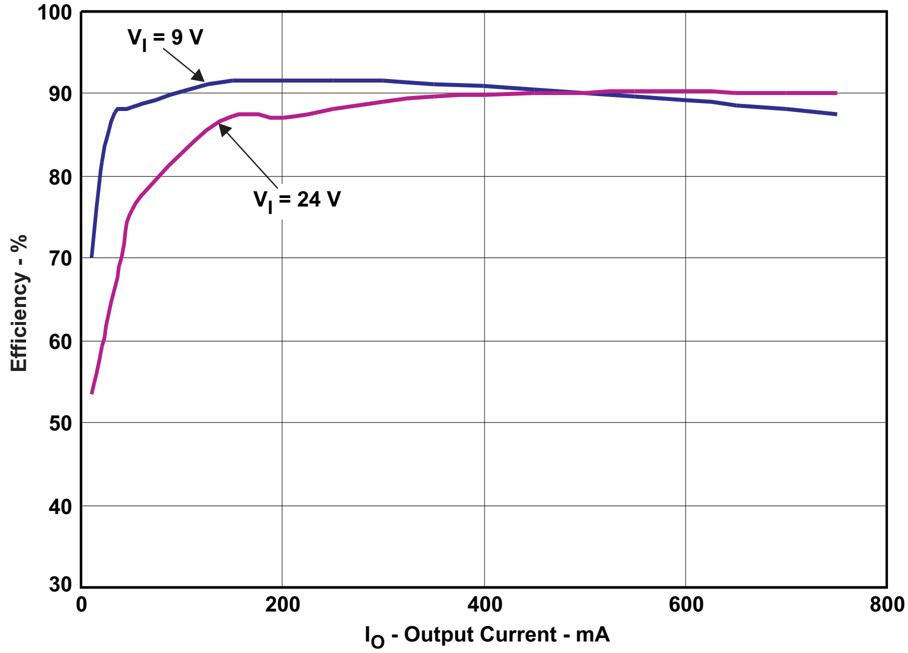


Figure 1. TPS61175EVM-588 Efficiency

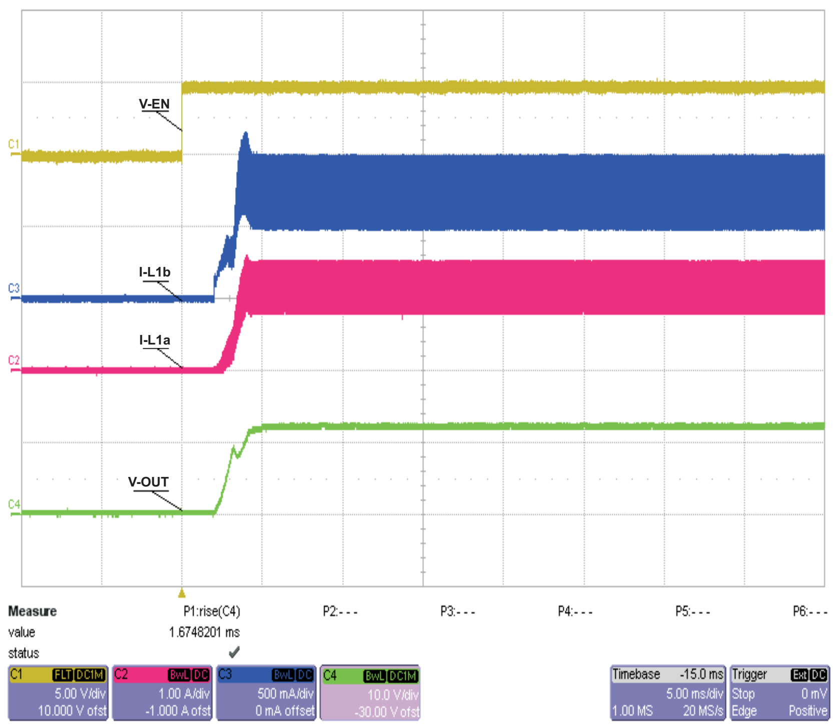


Figure 2. Start-Up With V_{IN} = 9V and I_{OUT} = 750 mA

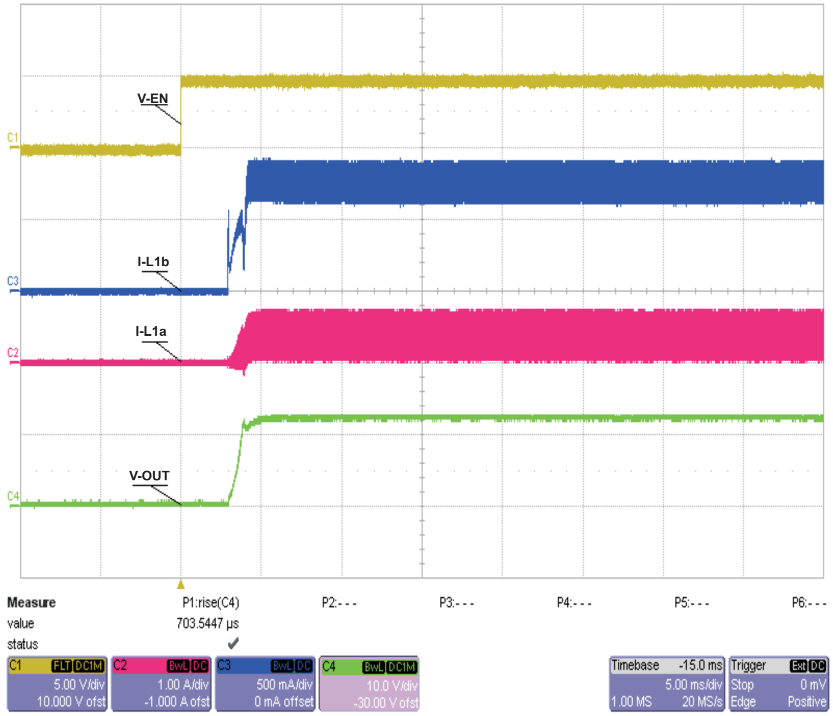


Figure 3. Start-Up With V_{IN} = 24V and I_{OUT} = 750 mA

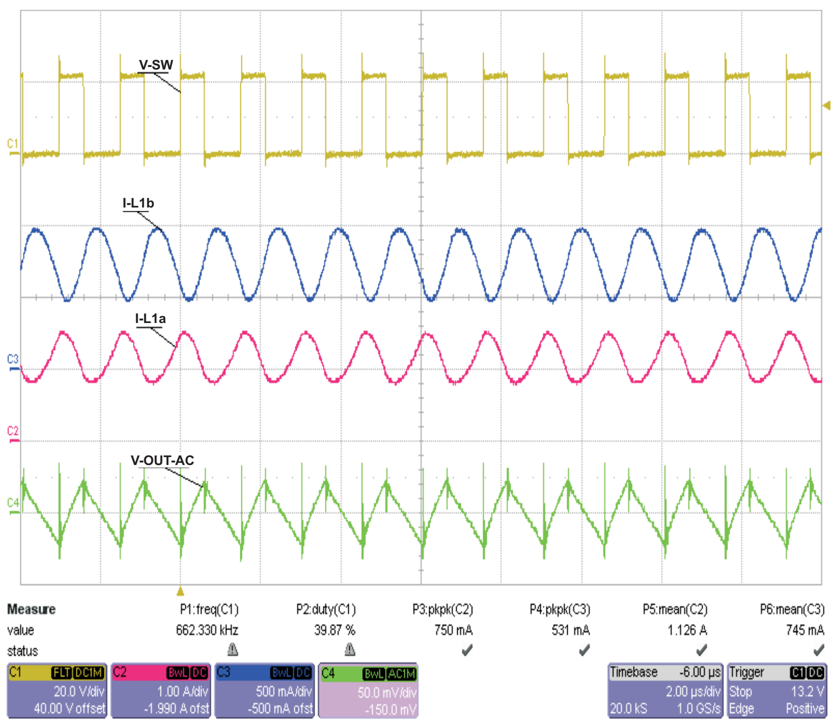


Figure 4. PWM Operation at 750 mA with V_{IN} = 9V

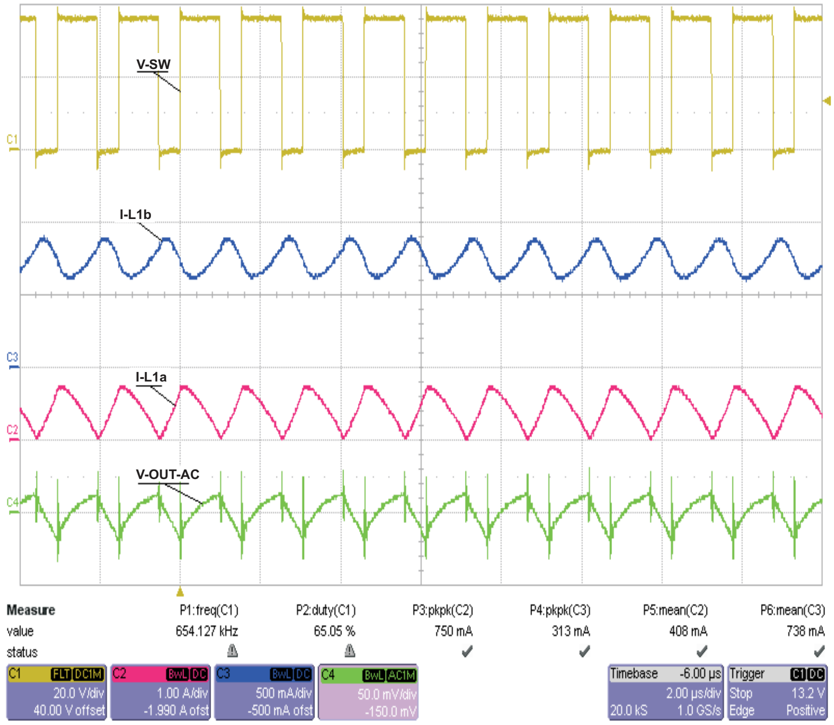


Figure 5. PWM Operation at 750 mA with V_{IN} = 24V

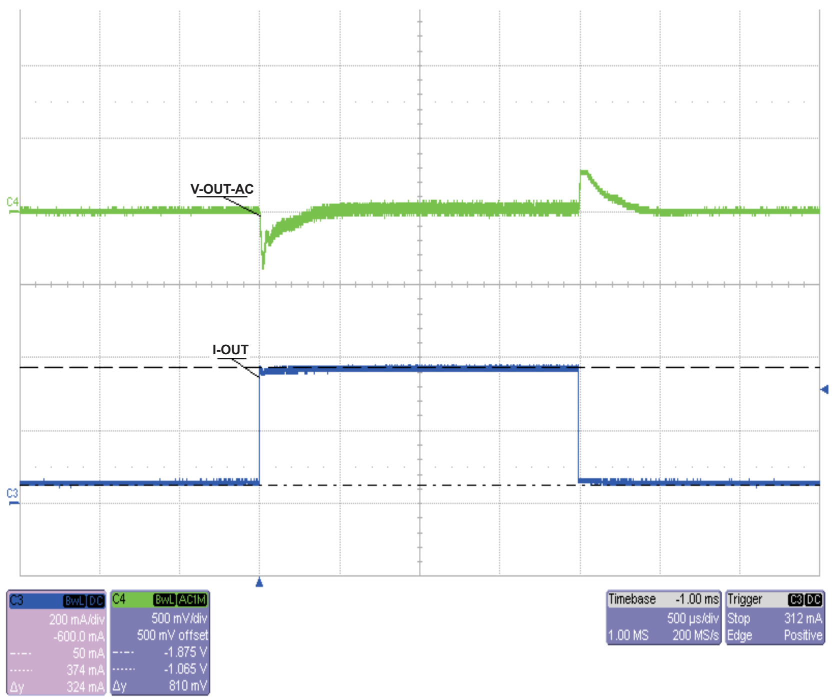


Figure 6. Load Transient Response From 50 mA to 375 mA With V_{IN} = 9V

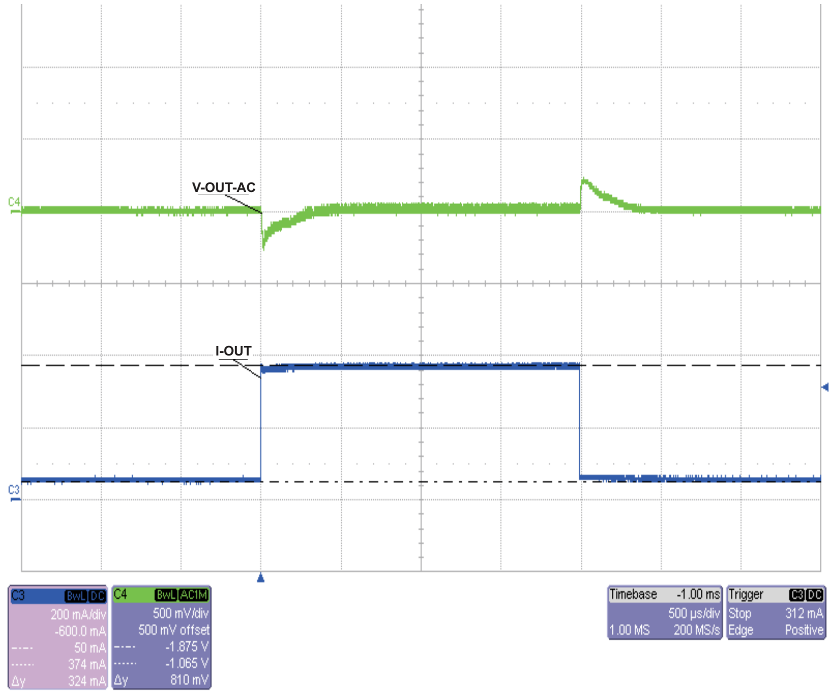


Figure 7. Load Transient Response From 50 mA to 375 mA With V_{IN} = 24V

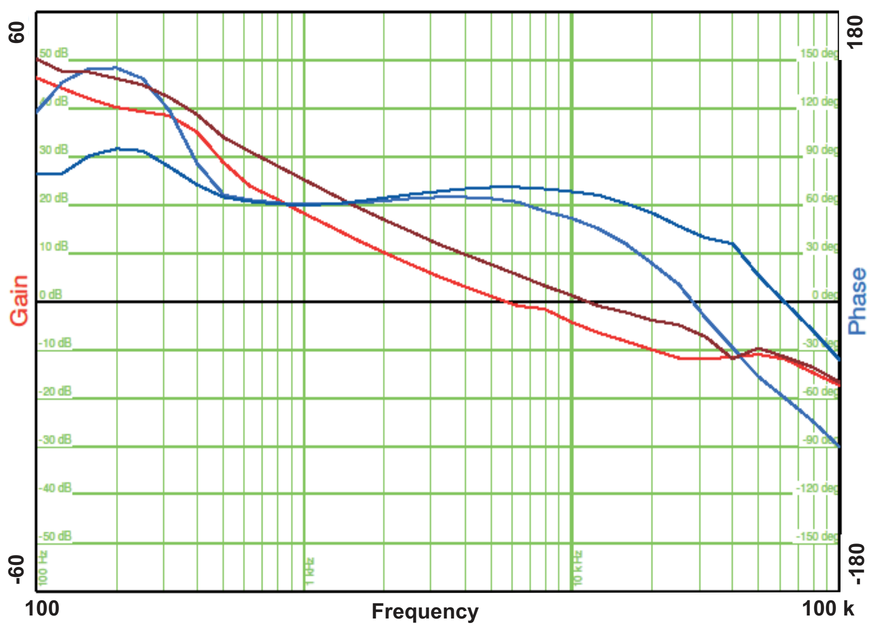


Figure 8. Loop Gain and Phase

4 Board Layout

This section provides the TPS61175EVM-588 board layout and illustrations.

4.1 Layout

Board layout is critical for all switch-mode power supplies. Figure 9 through Figure 13 show the board layout for the HPA326 printed-circuit board. The switching nodes with high frequency noise are isolated from the noise-sensitive feedback circuitry. Careful attention has been given to the routing of high-frequency current loops. See the data sheet (SLVS892) for further layout recommendations.

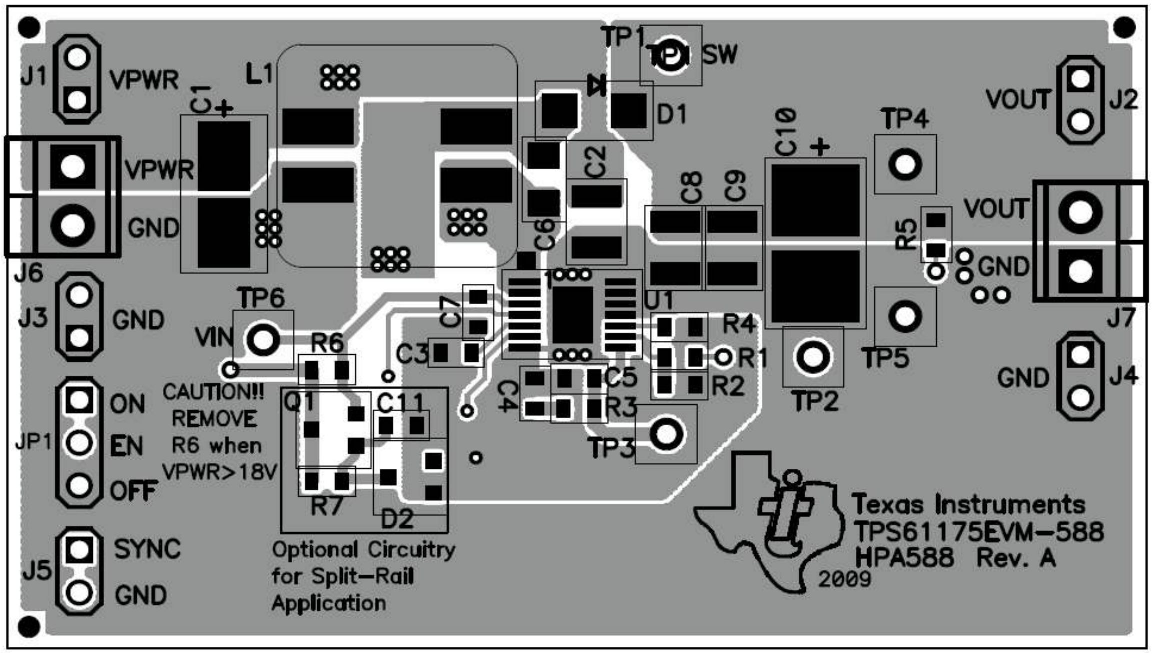


Figure 9. Top Layer Assembly

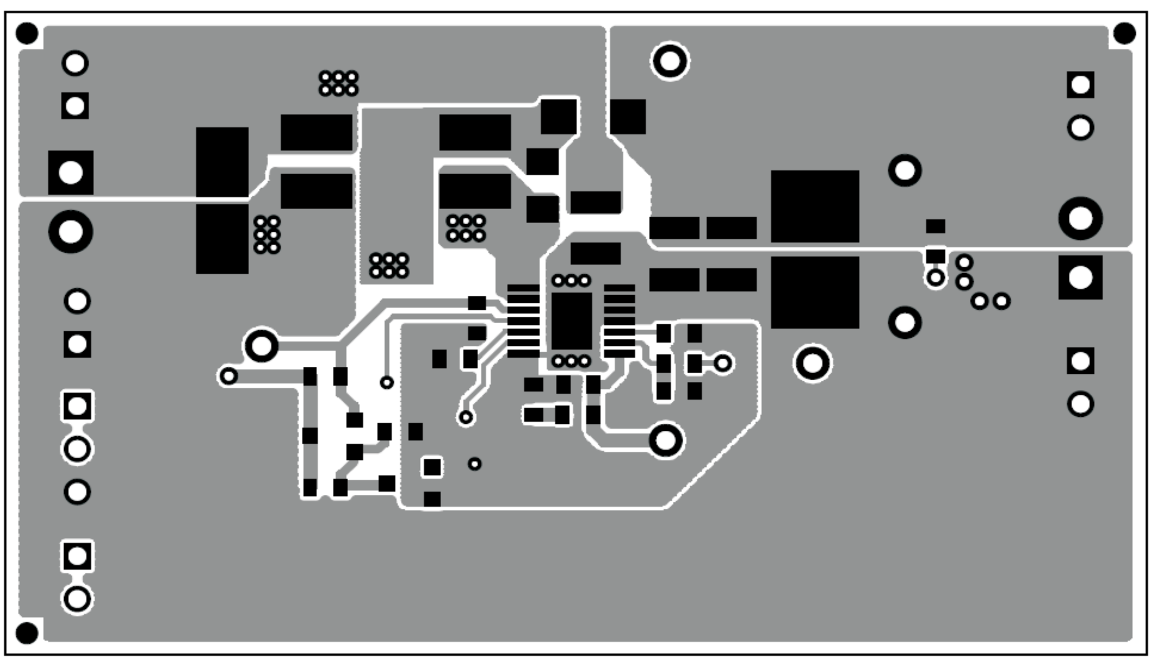


Figure 10. Top Layer Routing

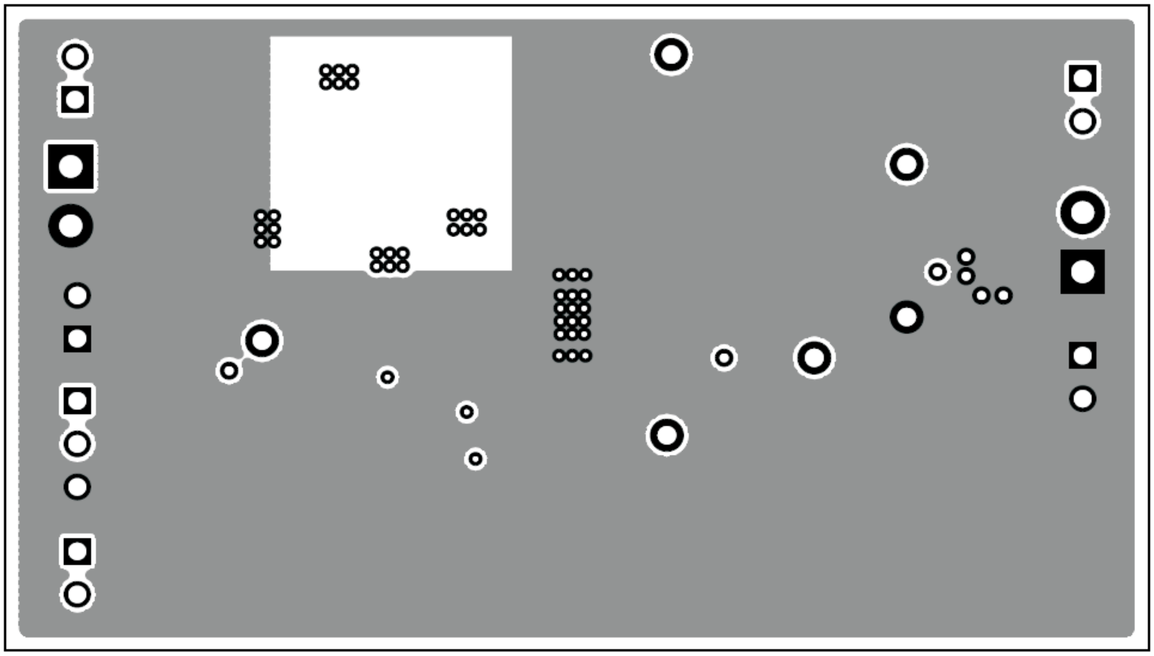


Figure 11. Internal Layer 1

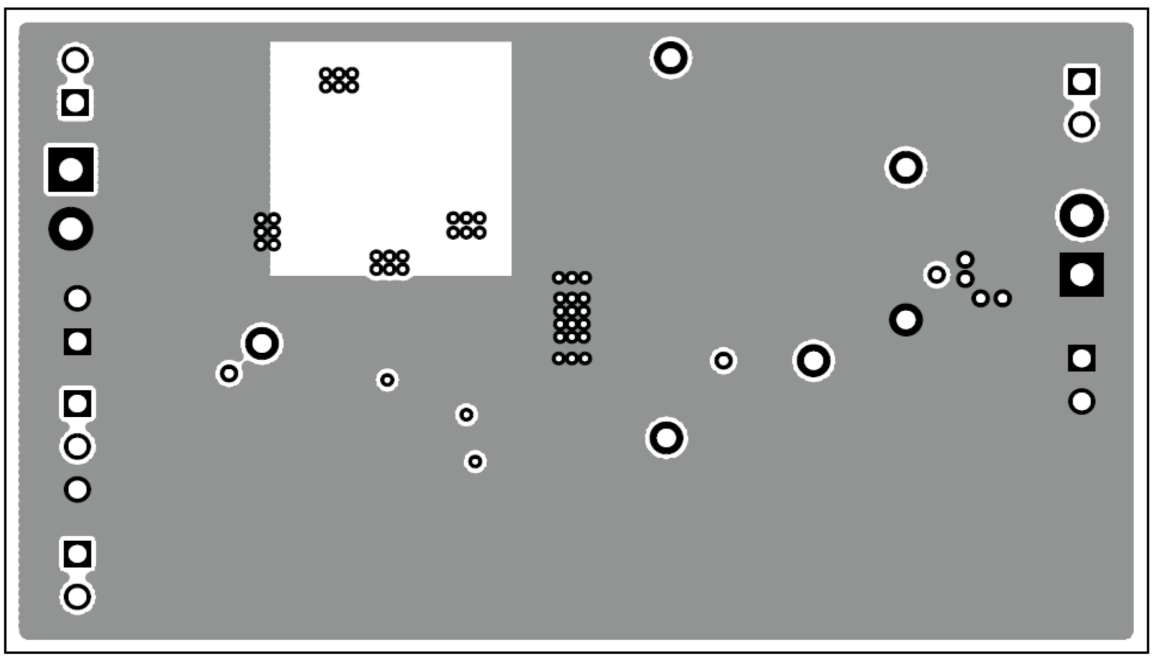


Figure 12. Internal Layer 2

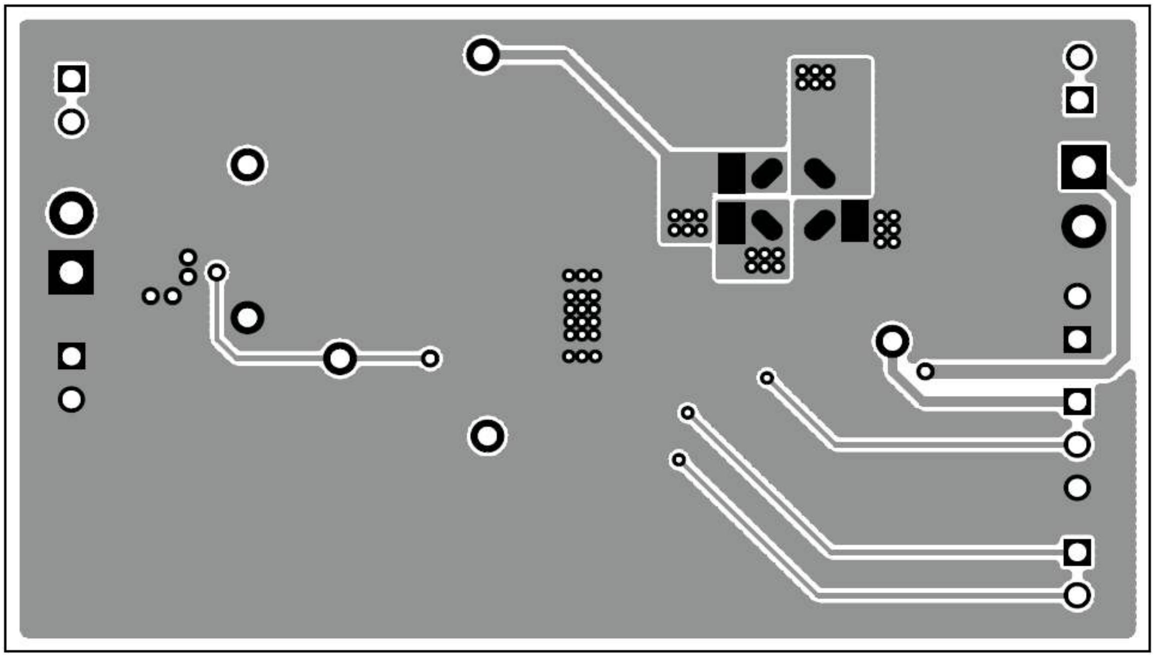


Figure 13. Bottom-Side Layer

5 5 Bill of Materials

Table 3 shows the TPS61175EVM-588 bill of materials.

Table 3. Bill of Materials

RefDes	Value	Description	Size	Part Number	MFR
C2	10 µF	Capacitor, Ceramic, 50V, X5R, 20%	1210	STD	STD
C3, C4	0.047 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
C5	Open	Capacitor, Ceramic, 10V, X5R, 10%	0603	STD	STD
C6	1 µF	Capacitor, Ceramic, 25V, X7R, 10%	1206	STD	STD
C7	0.1 µF	Capacitor, Ceramic, 25V, X5R, 20%	0603	STD	STD
C8	22 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	STD	STD
C9	10 µF	Capacitor, Ceramic, 25V, X5R, 10%	1210	STD	STD
C10	Open	Capacitor, Electrolytic, Snap Mt., 25V	Multi sizes	Engineering Only	STD
C11	0.01 µF (UNPOPULATED)	Capacitor, Ceramic, 25V, X5R, 20%	0603	STD	STD
D1	SS15	Diode, Schottky, 3A, 40V	SMA	SS15-TP	Micro Commercial
D2	MMBZ5246BLT1G (UNPOPULATED)	Diode, Zener, 16V, 225mW	SOT23	MMBZ5246BLT1G	ON Semi
J1–J5	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
J6, J7	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
L1	22uH	Inductor, SMT, 5.01A, 116mΩ, + 20%	0.484 x 0.484 inch	MSD1260-223MLB	Coilcraft
L2	Open	Inductor, SMT, yy-A, zz-mΩ	0.150 x 0.150 inch	LPD4012-xxxML	Coilcraft
Q1	BC848BLT1G (UNPOPULATED)	Transistor, NPN, VCEO 30V, VCBO 30V, VCES 30V, VEBO 5V, IC 100mA	SOT23	BC848BLT1G	ON Semi
R1, R4	143k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2	16.2k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3	2.00k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std

Table 3. Bill of Materials (continued)

RefDes	Value	Description	Size	Part Number	MFR
R7	7.68k (UNPOPULATED)	Resistor, Chip, 1/16W, 1%	0603	Std	Std
TP1–TP4, TP6	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
TP5	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
U1	TPS61175PWP	IC, High Voltage/Current Boost Converter	HTSSOP-14	TPS61175PWP	TI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 9 V to 24 V and the output voltage range of 0 V to 12 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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