TEXAS INSTRUMENTS

SN74AHCT174
SCLS419G – JUNE 1998 – REVISED MAY 2023

SN74AHCT174 Hex D-Type Flip-Flops with Clear

1 Features

- Inputs are TTL-voltage compatible
- Contain six flip-flops with single-rail outputs
- Latch-Up performance exceeds 250 mA per JESD 17

2 Applications

- Buffer/Storage Registers
- Shift Registers
- Pattern Generators

3 Description

These positive-edge-triggered D-type flip-flops have a direct clear ($\overline{CLR}$) input.

Package Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
SN74AHCT174	D (SOIC, 16)	9.00 mm × 3.90 mm
	DB (SSOP, 16)	6.2 mm × 5.3 mm
	N (PDIP , 16)	19.3 mm × 6.35 mm
	NS (SOP, 16)	10.3 mm × 5.3 mm
	PW (TSSOP, 16)	5.00 mm × 4.40 mm

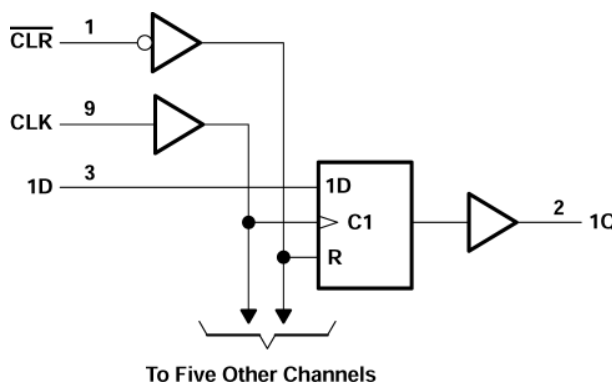1. For all available packages, see the orderable addendum at the end of the data sheet.

Figure 3-1. Logic Diagram (Positive Logic)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

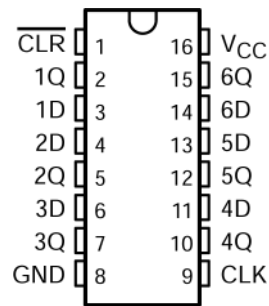| **Changes from Revision F (April 2002) to Revision G (May 2023)**	**Page**
• Added *Applications*, *Package Information* table, *Pin Functions* table, and *Thermal Information* table.............. 1	

5 Pin Configuration and Functions

```
              ┌───┐ ┌───┐
    CLR  [  1      16  ] VCC
     1Q  [  2      15  ] 6Q
     1D  [  3      14  ] 6D
     2D  [  4      13  ] 5D
     2Q  [  5      12  ] 5Q
     3D  [  6      11  ] 4D
     3Q  [  7      10  ] 4Q
    GND  [  8       9  ] CLK
              └──────────┘
```

Figure 5-1. Package SN74AHCT174 D, DB, DGV, N, NS, or PW Package (Top View)

Table 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CLR}}$	I	Clear all channels, active low
2	1Q	O	Channel 1, Q output
3	1D	I	Channel 1, D input
4	2D	I	Channel 2, D input
5	2Q	O	Channel 2, Q output
6	3D	I	Channel 3, D input
7	3Q	O	Channel 3, Q output
8	GND	—	Ground
9	CLK	I	Clock all channels, rising edge triggered
10	4Q	O	Channel 4, Q output
11	4D	I	Channel 4, D input
12	5Q	O	Channel 5, Q output
13	5D	I	Channel 5, D input
14	6D	I	Channel 6, D input
15	6Q	O	Channel 6, Q output
16	V_{CC}	—	Positive supply

Product Folder Links: *SN74AHCT174*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I [1]	Input voltage range		−0.5	7	V
V_O [1]	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$(V_I < 0)$		−20	mA
I_{OK}	Output clamp current	$(V_O < 0$ or $V_O > V_{CC})$		±20	mA
I_O	Continuous output current	$(V_O = 0$ to $V_{CC})$		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Machine Model (MM), per JEDEC specification	±200	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see Note 1)

		SN74AHCT174		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall time		20	ns/V
T_A	Operating free-air temperature	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25 °C			SN74AHCT174		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = -50 µA	4.5 V	4.4	4.5		4.4		V
	I_{OH} = -8 mA		3.94			3.8		

Product Folder Links: *SN74AHCT174*

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25 °C			SN74AHCT174		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC} [1]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	μA
C_i	V_I = V_{CC} or GND	5 V		2	10		10	pF

(1)   This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

6.5 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T_A = 25°C		SN74AHCT174		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	5		5		
t_{su}	Setup time before CLK↑	Data	5		5		ns
		$\overline{CLR}$ inactive	3.5		3.5		
t_h	Hold time, data after CLK↑		0		0		ns

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74AHCT174		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	100[1]	135[1]		80		MHz
			C_L = 50 pF	80	115		65		
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 15 pF		7.6[1]	10.4[1]	1	13	ns
t_{PLH}	CLK	Any Q	C_L = 15 pF		5.8[1]	7.8[1]	1	9	ns
t_{PHL}					5.8[1]	7.8[1]	1	9	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		8.1	11.4	1	13	ns
t_{PLH}	CLK	Any Q	C_L = 50 pF		6.3	8.8	1	10	ns
t_{PHL}					6.3	8.8	1	10	
$t_{sk(o)}$			C_L = 50 pF		1 [2]			1	ns

(1)   On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2)   On products compliant to MIL-PRF-38535, this parameter does not apply.

6.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT174			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see ^{Note 4})

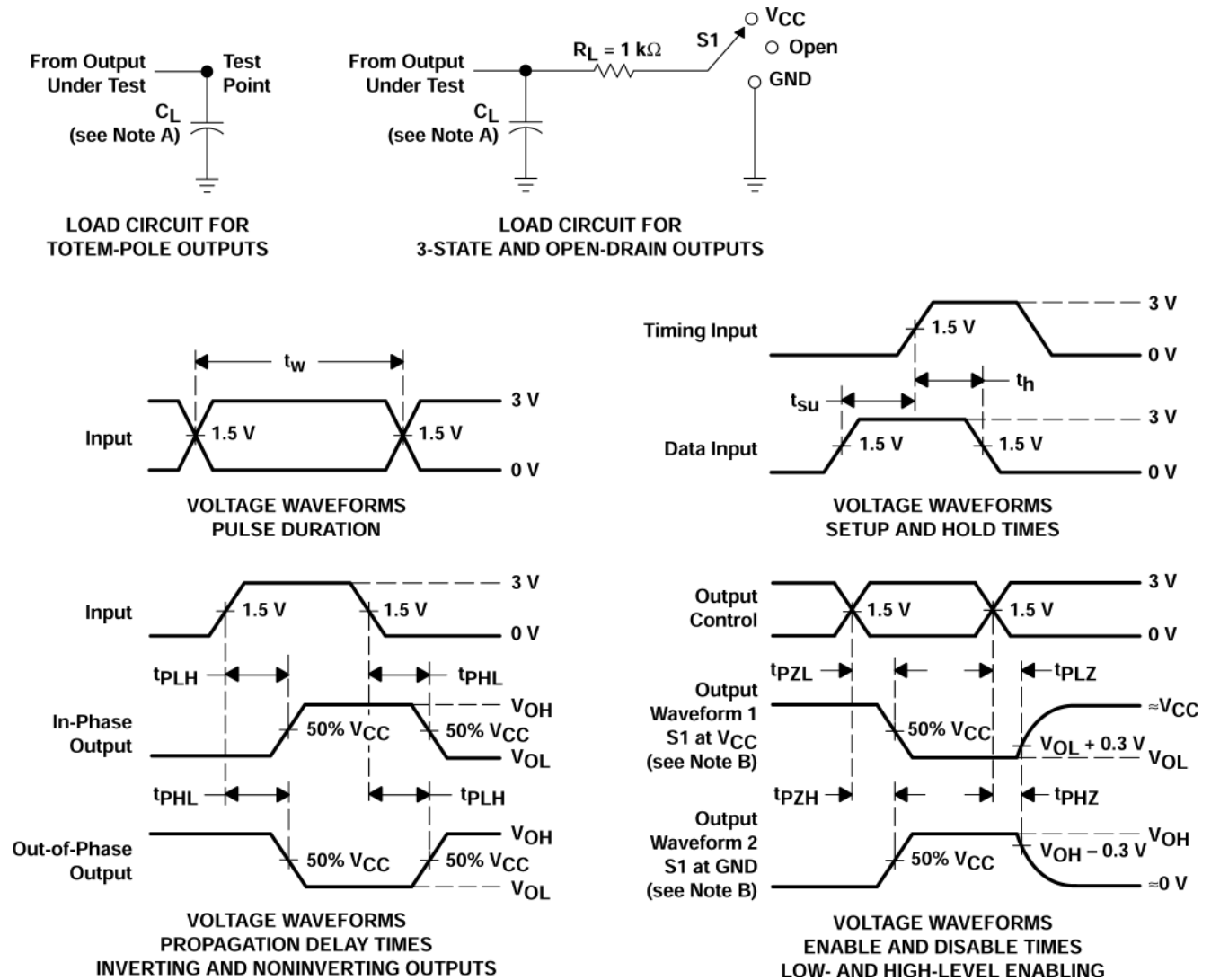| PARAMETER		SN74AHCT174			UNIT
		MIN	**TYP**	**MAX**	
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1)   Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	28	pF

Product Folder Links: *SN74AHCT174*

7 Parameter Measurement Information

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

Product Folder Links: SN74AHCT174

8 Detailed Description

8.1 Overview

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.
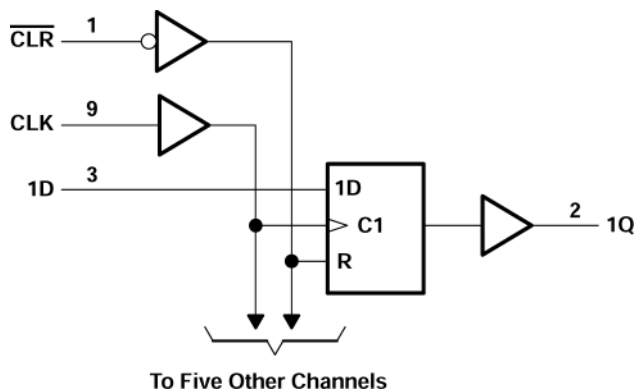
8.2 Functional Block Diagram

Figure 8-1. Logic Diagram (Positive Logic)

Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

8.3 Device Functional Modes

Table 8-1. Function Table

INPUTS[1]			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Qo

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT174D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT174	
SN74AHCT174DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB174	Samples
SN74AHCT174DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT174	Samples
SN74AHCT174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT174N	Samples
SN74AHCT174NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT174	Samples
SN74AHCT174PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB174	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT174DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT174DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT174NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT174PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT174DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHCT174DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT174NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74AHCT174PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHCT174D	D	SOIC	16	40	507	8	3940	4.32
SN74AHCT174N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT174N	N	PDIP	16	25	506	13.97	11230	4.32

8.2 / 7.4 TYP

A

PIN 1 ID AREA

14X 1.27

1

16

10.4 / 10.0 NOTE 3

2X 8.89

8

9

B

5.4 / 5.2 NOTE 4

16X 0.51 / 0.35

⌖ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0.3 / 0.1

0° - 10°

1.05 / 0.55

(1.25)

DETAIL A
TYPICAL
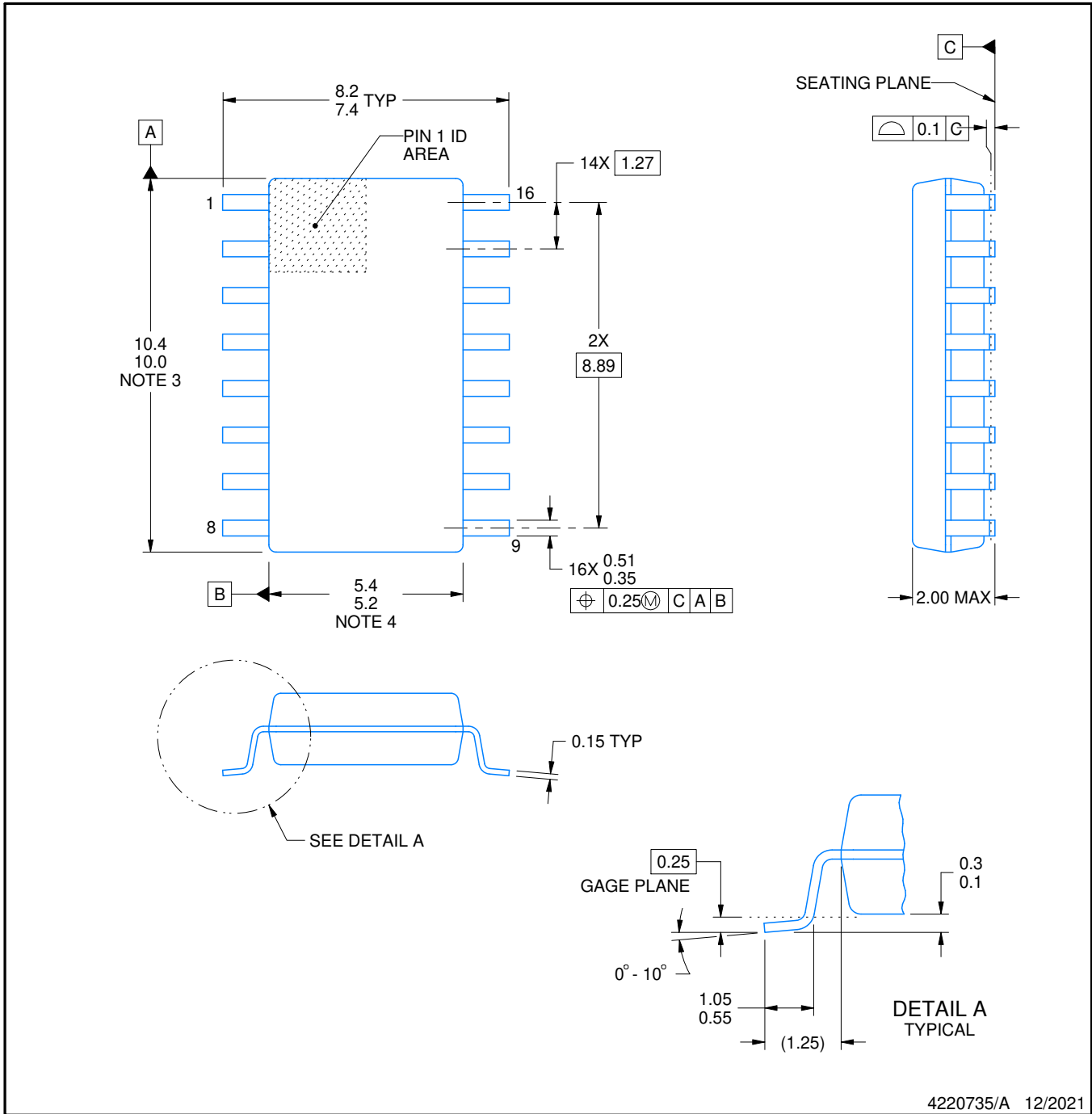
4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

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16X (1.85)

SYMM

SEE
DETAILS

1

16X (0.6)

16

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
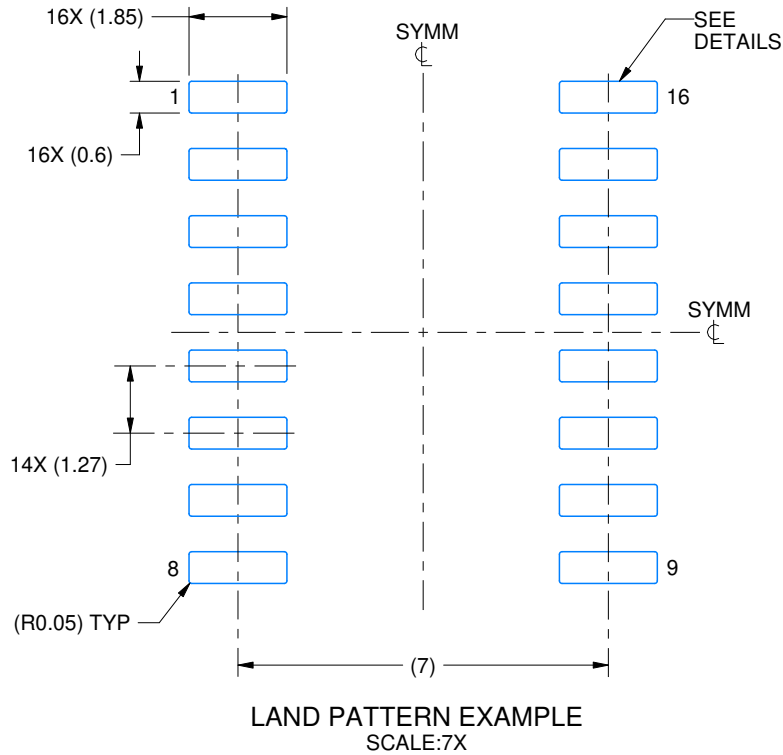
4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
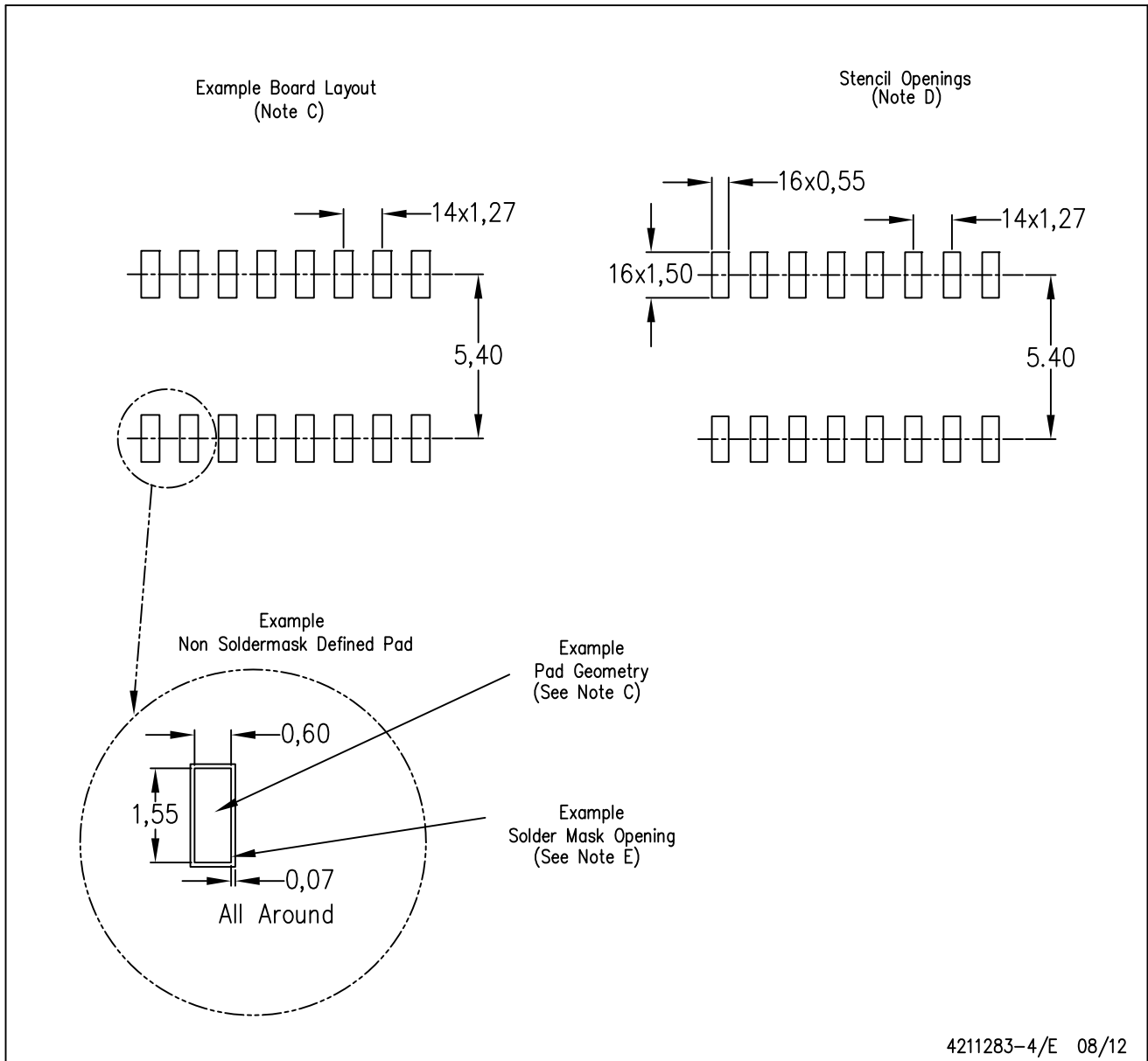
D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
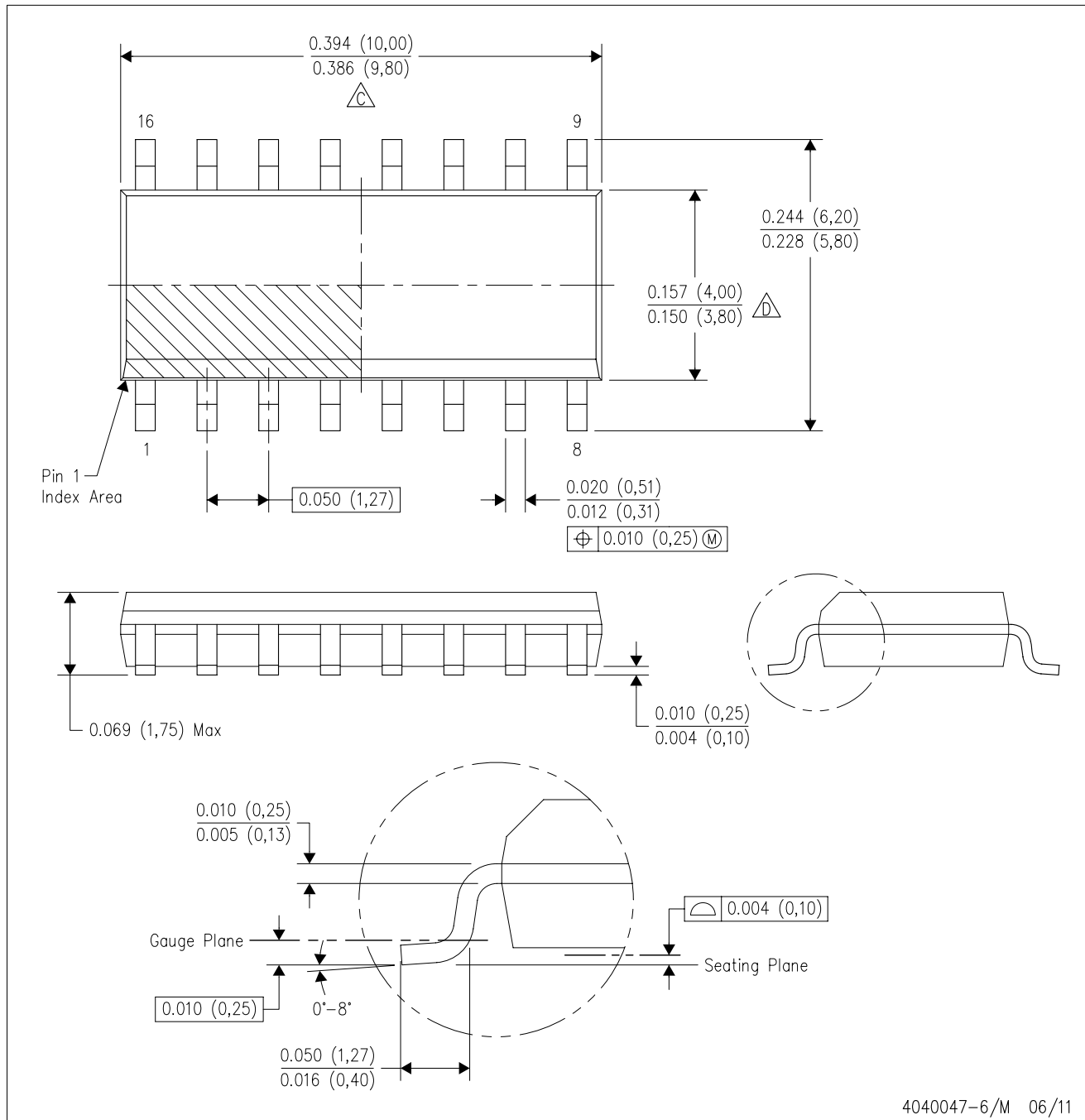
0.394 (10,00)
0.386 (9,80)
⟋C⟍

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⟋D⟍

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      ⟋C⟍   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
      ⟋D⟍   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←14x1,27

←16x0,55

←14x1,27

5,40

16x1,50─

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

─0,60

1,55

Example
Solder Mask Opening
(See Note E)

─0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

2X

4.55

5.1
4.9
NOTE 3

1

8

9

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

SEATING
PLANE

C

⌴ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50
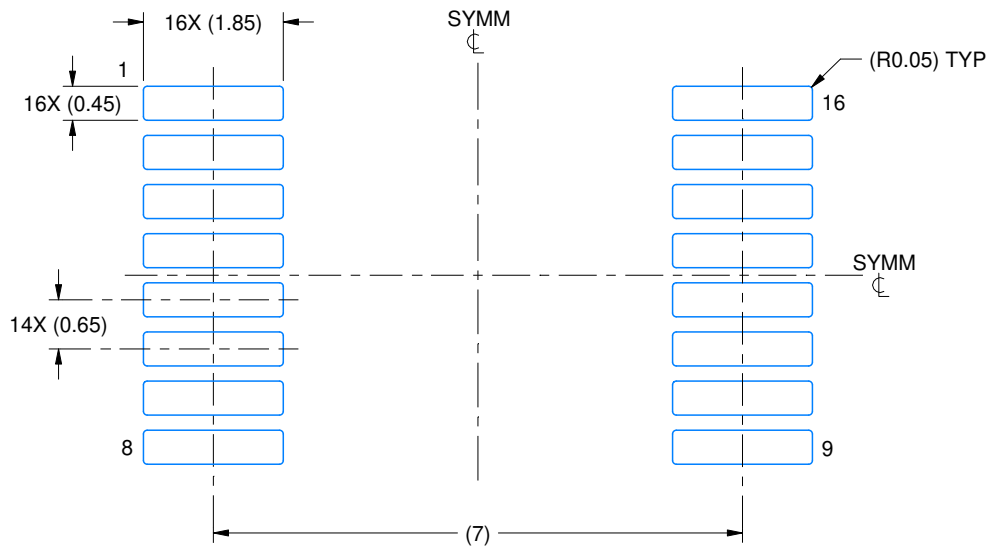
DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
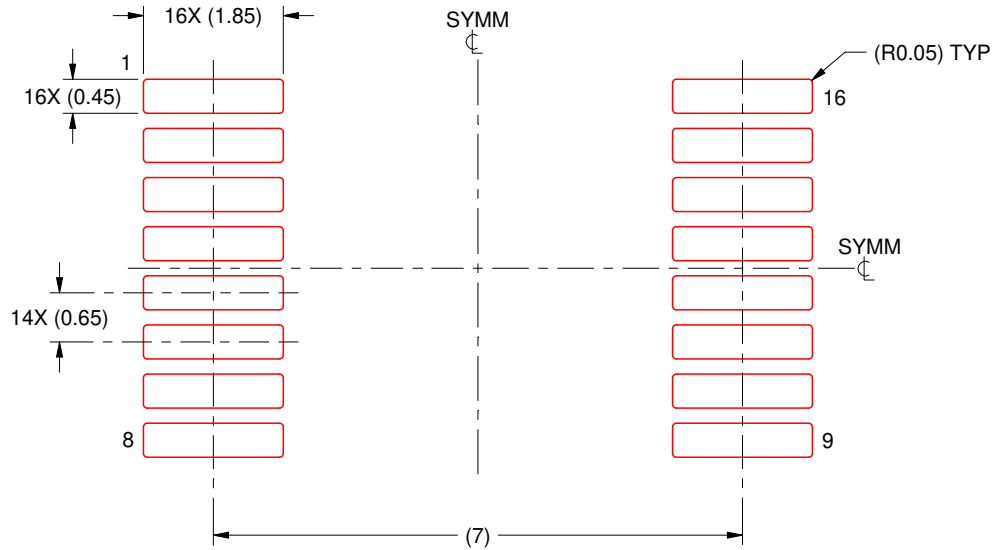
SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

16X (1.5)

16X (0.45)

14X (0.65)

SYMM

SYMM

(R0.05) TYP

(5.8)

1

16

8

9

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

2X

4.55

6.5 / 5.9
NOTE 3

8

9

16X 0.38 / 0.22

B

5.6 / 5.0
NOTE 4

⊕ 0.1 Ⓜ C A B

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

0.25 / 0.09

GAGE PLANE

0.25

2 MAX

0°-8°

0.95 / 0.55

0.05 MIN

DETAIL A
TYPICAL

4220763/A   05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

16X (1.85)

1

16X (0.45)

14X (0.65)

8

SYMM
℄

(R0.05) TYP

16

SYMM
℄

9

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220763/A   05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

16X (0.45)

14X (0.65)

SYMM

SYMM

(R0.05) TYP

1

16

8

9

(7)
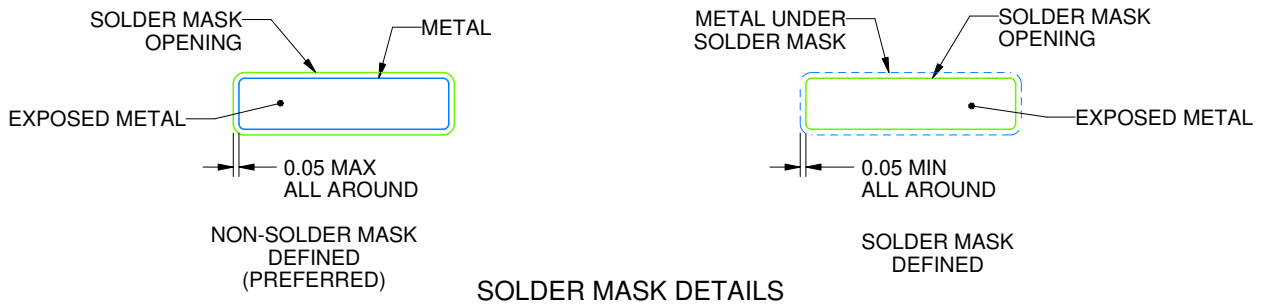
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A   05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,15 NOM

Gage Plane

0°–10°

0,25

1,05
0,55

1,27

0,51
0,35

⊕ 0,25 Ⓜ

14

8

5,60
5,00

8,20
7,40

1

7

A

0,15
0,05

2,00 MAX

Seating Plane

△ 0,10

DIM ＼ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION (C)	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) (D)

0.045 (1,14) / 0.030 (0,76) (D)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) (M)

14/18 Pin Only
20 Pin vendor option (D)

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
       B. This drawing is subject to change without notice.
      (C) Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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