EL1510

Medium Power Differential Line Driver

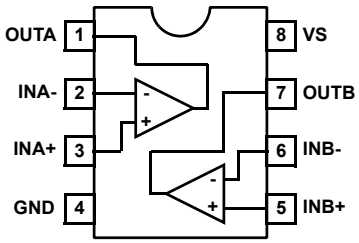
FN7122
Rev 2.00
March 26, 2007

The EL1510 is a dual operational amplifier designed for central office and customer premise line driving in both SDSL and ADSL solutions. This device features a high drive capability of 250mA while consuming only 7.5mA of supply current per amplifier, operating from ±12V supplies. This driver achieves a typical distortion of less than -85dBc, at 150kHz into a 25Ω load. The EL1510 is available in the power 8 Ld DFN package and is specified for operation over the full -40°C to +85°C temperature range. The DFN package has the potential for a very low junction to ambient thermal resistance of 43°C/W, making it suitable for high power applications. The EL1510 is in the 8 Ld SOIC package and thus is limited to applications where the power dissipation in the device is less than 781mW.

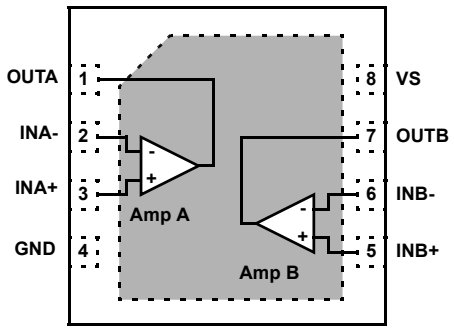
The EL1510 is ideal for CPE modem applications in ADSL, HDSL2, G.SHDSL, and VDSL.

Pinouts

EL1510
(8 LD SOIC)
TOP VIEW



EL1510
(8 LD DFN)
TOP VIEW



Features

- 40V_{P-P} differential output drive into 100Ω
- -85dBc typical driver output distortion at full output at 150kHz
- Low quiescent current of 7.5mA per amplifier
- Pb-free plus anneal available (RoHS compliant)

Applications

- ADSL G.lite CO line driving
- G.SHDSL, HDSL2 line drivers
- ADSL full rate CPE line driving
- Video distribution amplifiers
- Video twisted-pair line drivers

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL1510CS	1510CS	-	8 Ld SOIC	MDP0027
EL1510CS-T7	1510CS	7”	8 Ld SOIC	MDP0027
EL1510CS-T13	1510CS	13”	8 Ld SOIC	MDP0027
EL1510CSZ (See Note)	1510CSZ	-	8 Ld SOIC (Pb-Free)	MDP0027
EL1510CSZ-T7 (See Note)	1510CSZ	7”	8 Ld SOIC (Pb-Free)	MDP0027
EL1510CSZ-T13 (See Note)	1510CSZ	13”	8 Ld SOIC (Pb-Free)	MDP0027
EL1510CL	1510CL	-	8 Ld DFN	MDP0047
EL1510CL-T7	1510CL	7”	8 Ld DFN	MDP0047
EL1510CL-T13	1510CL	13”	8 Ld DFN	MDP0047

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Voltage to Ground . . . . . -0.3V to +26.4V
V_{IN}+ Voltage . . . . . GND to V_S+
Current into any Input 8mA
Continuous Output Current 75mA

Ambient Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . -40°C to +150°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = ±12V, R_F = 1.5kΩ, R_L = 100Ω to mid supply, T_A = 25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +4		70		MHz
HD	Total Harmonic Distortion	f = 1MHz, V_O = 16V_{P-P}, R_L = 50Ω		-75		dBc
dG	Differential Gain	A_V = +2, R_L = 37.5Ω		0.17		%
dθ	Differential Phase	A_V = +2, R_L = 37.5Ω		0.1		°
SR	Slewrate	V_{OUT} from -4.5V to +4.5V	350	500		V/µs
DC PERFORMANCE						
V_{OS}	Offset Voltage		-17		17	mV
ΔV_{OS}	V_{OS} Mismatch		-10		10	mV
R_{OL}	Transimpedance	V_{OUT} from -4.5V to +4.5V	1	2	3.5	MΩ
INPUT CHARACTERISTICS						
I_B+	Non-Inverting Input Bias Current		-5		5	µA
I_B-	Inverting Input Bias Current		-30		30	µA
ΔI_B-	I_B- Mismatch		-20		20	µA
e_N	Input Noise Voltage			2.8		nV/√Hz
i_N+	+Input Noise Current			1.8		pA/√Hz
i_N-	-Input Noise Current			19		pA/√Hz
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing Single Ended	R_L = 100Ω to GND	±10.3	±10.9		V
V_{OUT} P	Loaded Output Swing Single Ended	R_L = 25Ω to GND	9.5	10.2		V
V_{OUT} N	Loaded Output Swing Single Ended	R_L = 25Ω to GND	-8.2	-9.8		V
I_{OUT}	Output Current	R_L = 0Ω		500		mA
SUPPLY						
V_S	Supply Voltage	Single Supply	5		24	V
I_S	Supply Current per Amplifier	All Outputs at 0V		7.5	9	mA

Typical Performance Curves

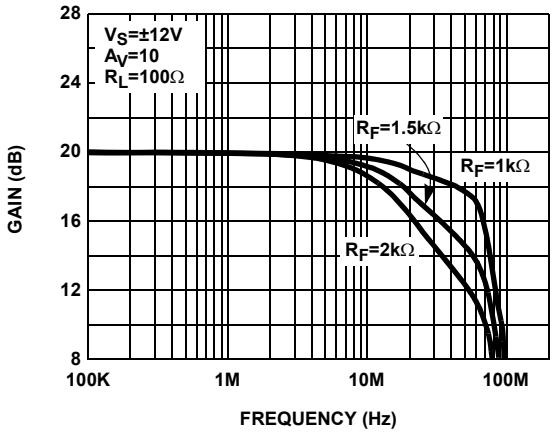


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE vs R_F

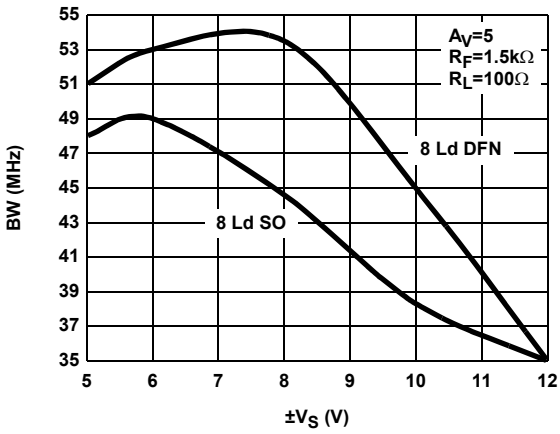


FIGURE 2. DIFFERENTIAL BANDWIDTH vs SUPPLY VOLTAGE

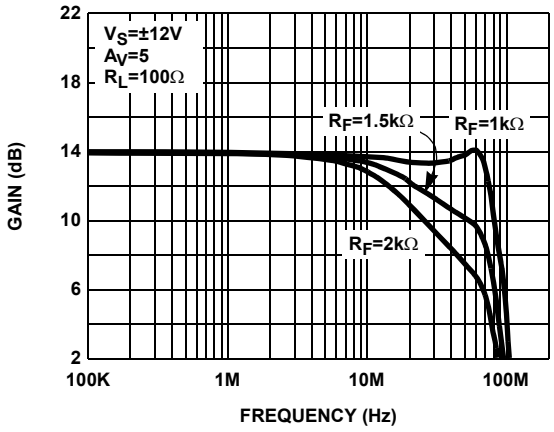


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs R_F

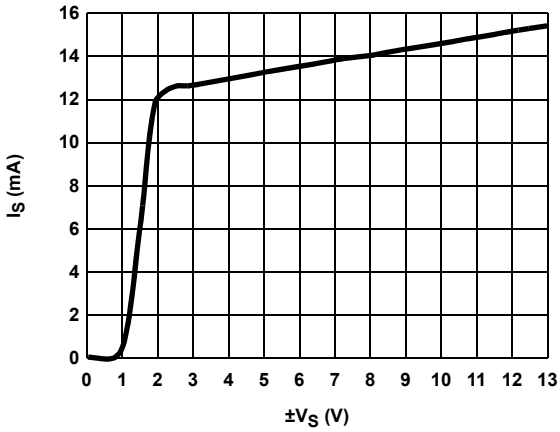


FIGURE 4. SUPPLY CURRENT vs SUPPLY VOLTAGE

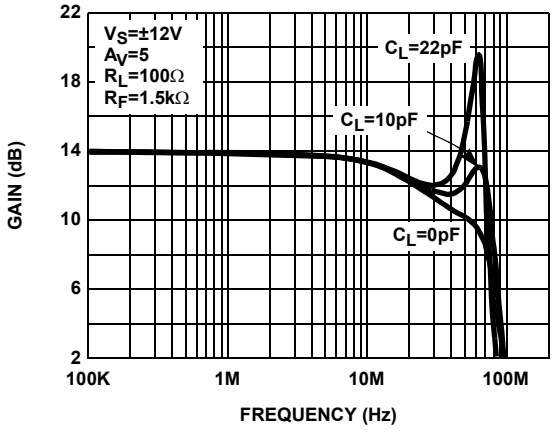


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE vs C_L

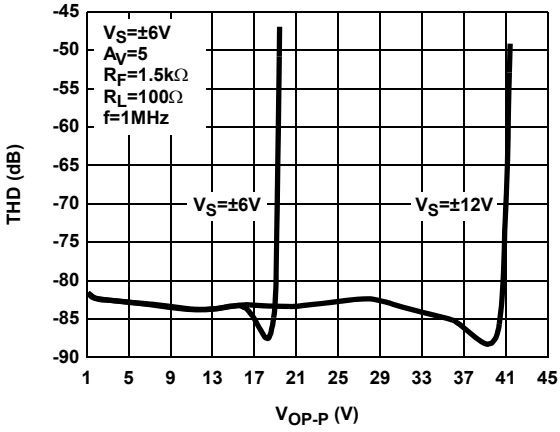


FIGURE 6. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE - ALL PACKAGES

Typical Performance Curves (Continued)

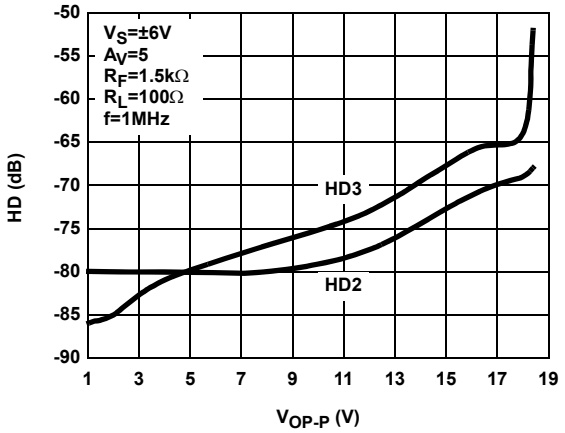


FIGURE 7. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE - ALL PACKAGES

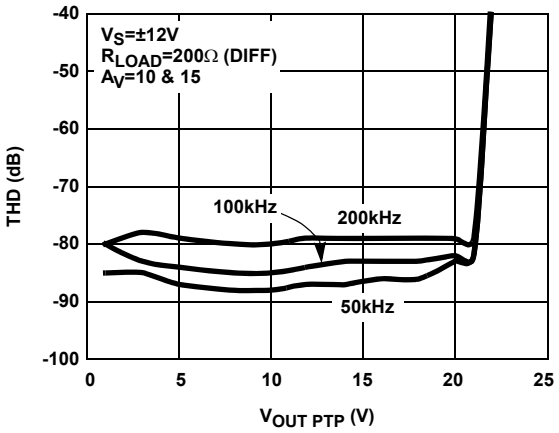


FIGURE 8. DISTORTION RESULTS

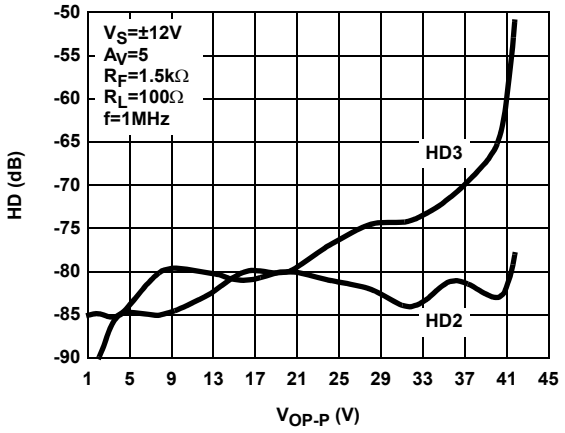


FIGURE 9. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE - ALL PACKAGES

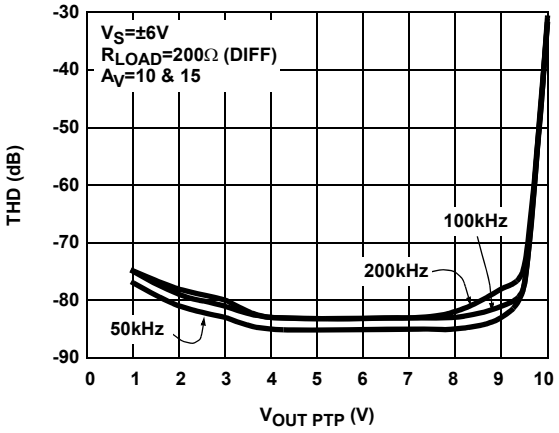


FIGURE 10. DISTORTION RESULTS

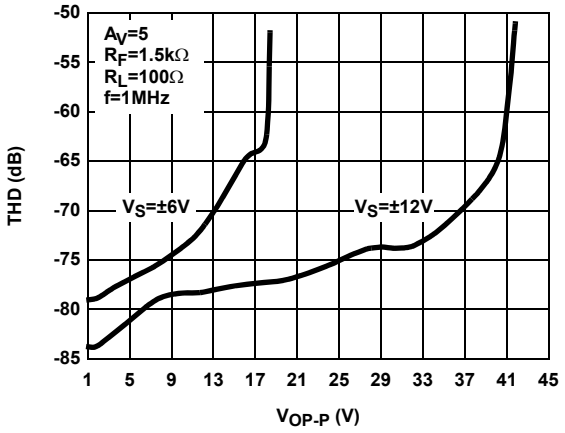


FIGURE 11. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE - ALL PACKAGES

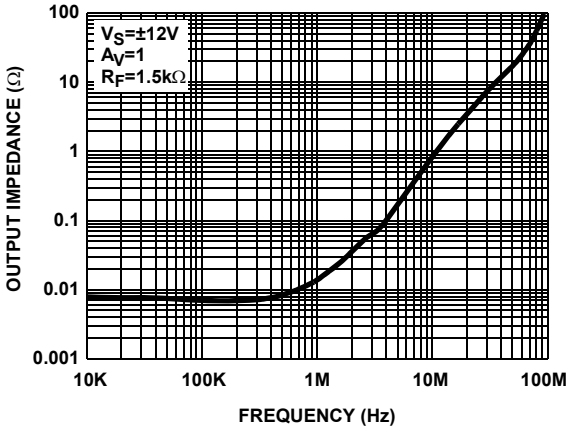


FIGURE 12. OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

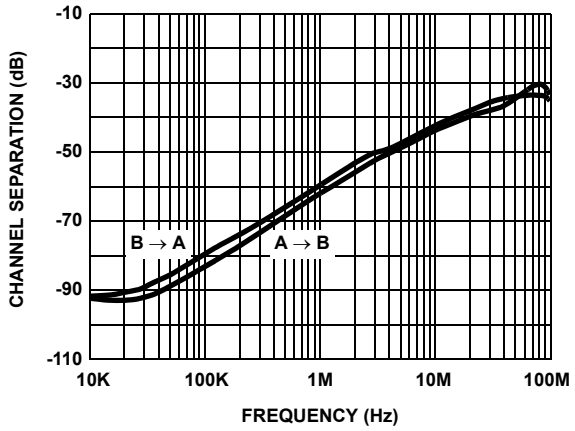


FIGURE 13. CHANNEL SEPARATION vs FREQUENCY

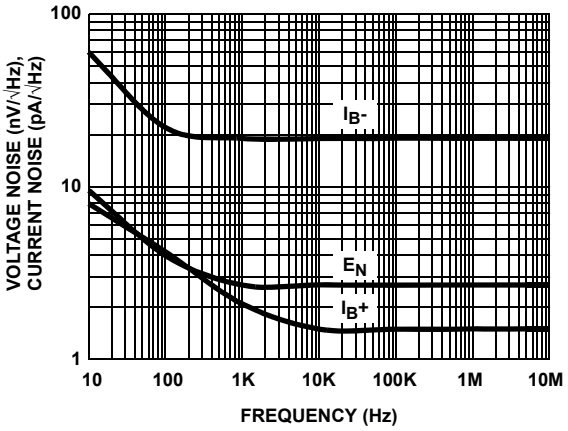


FIGURE 14. VOLTAGE AND CURRENT NOISE vs FREQUENCY

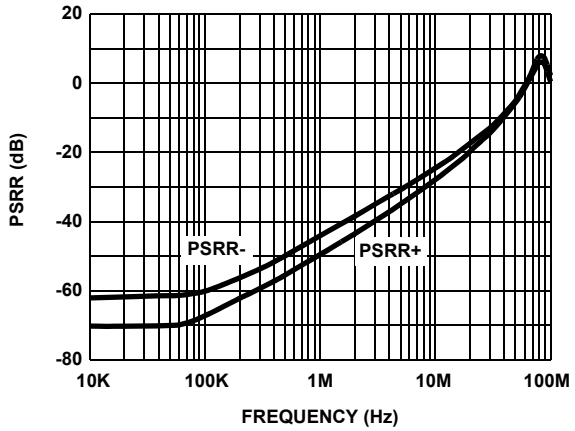


FIGURE 15. PSRR vs FREQUENCY

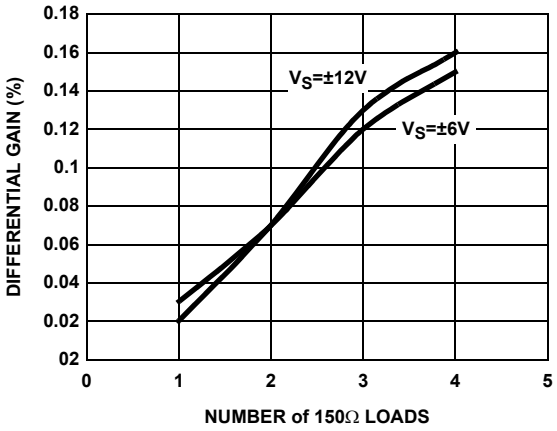


FIGURE 16. DIFFERENTIAL GAIN

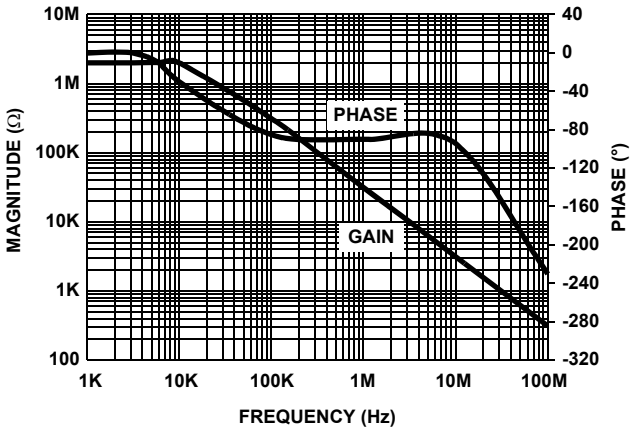


FIGURE 17. TRANSIMPEDANCE (ROL) vs FREQUENCY

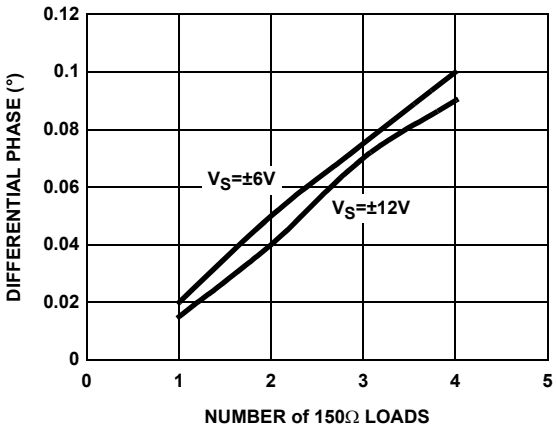


FIGURE 18. DIFFERENTIAL PHASE

Typical Performance Curves (Continued)

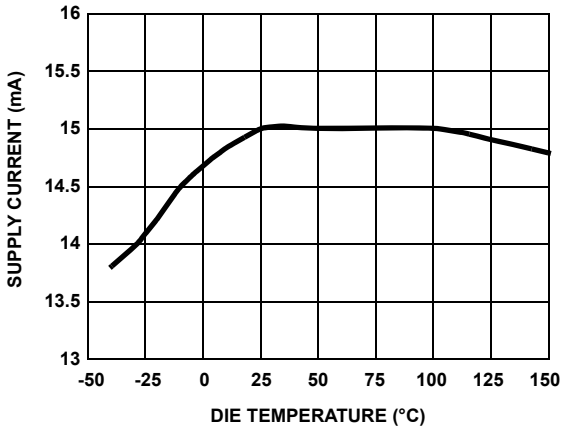


FIGURE 19. SUPPLY CURRENT vs TEMPERATURE

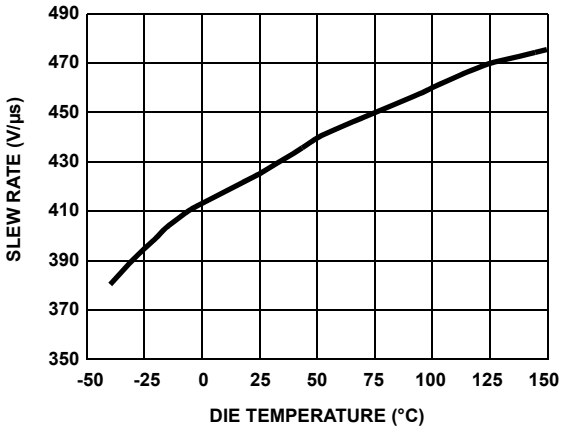


FIGURE 20. SLEW RATE vs TEMPERATURE

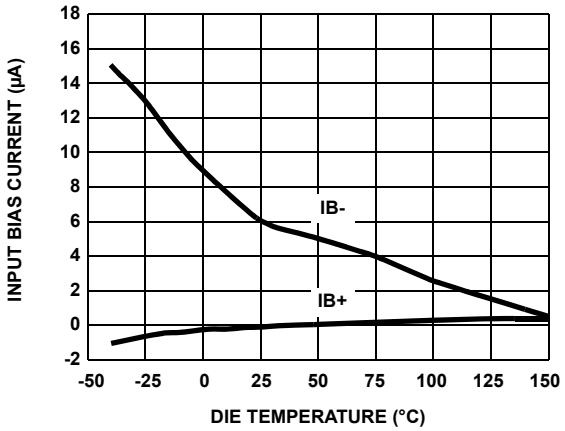


FIGURE 21. INPUT BIAS CURRENT vs TEMPERATURE

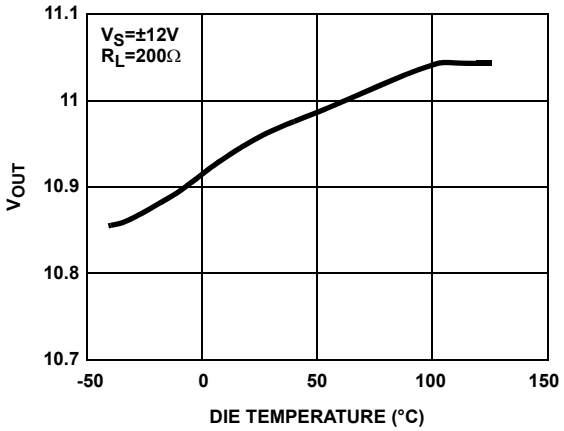


FIGURE 22. OUTPUT VOLTAGE vs TEMPERATURE

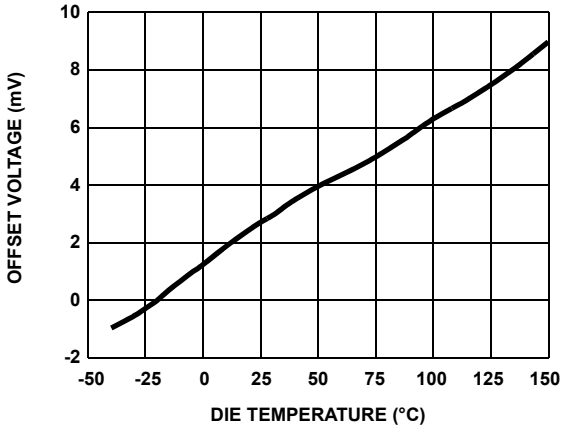


FIGURE 23. OFFSET VOLTAGE vs TEMPERATURE

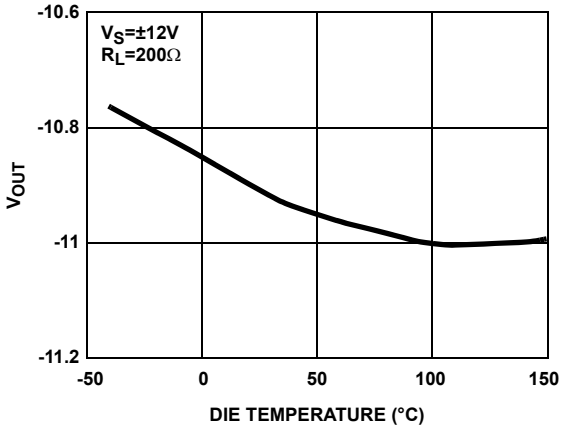


FIGURE 24. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

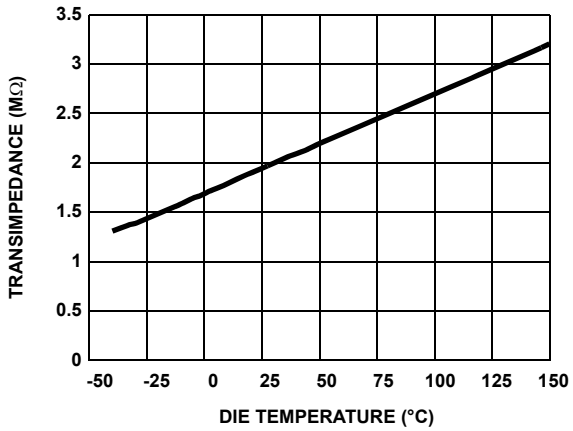


FIGURE 25. TRANSIMPEDANCE vs TEMPERATURE

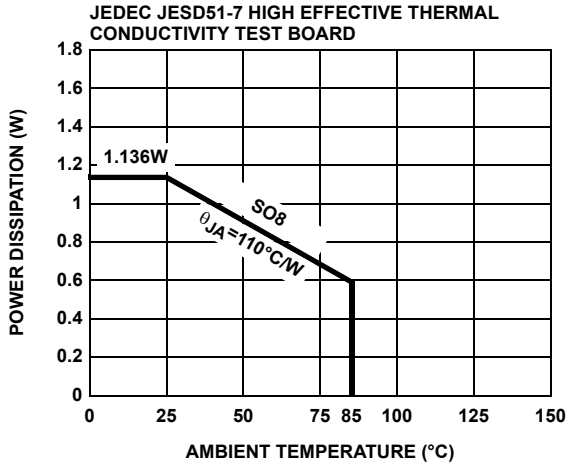


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

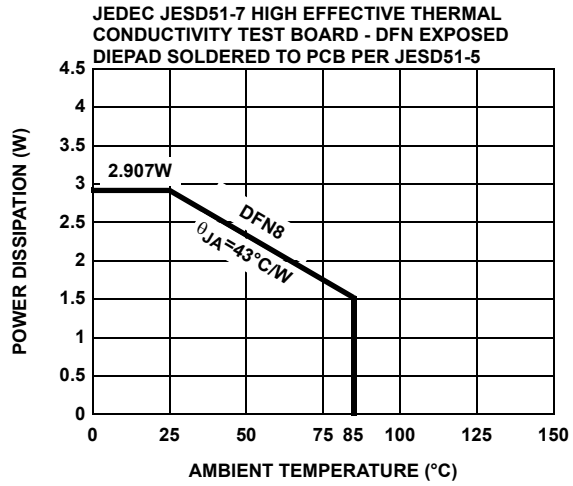


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

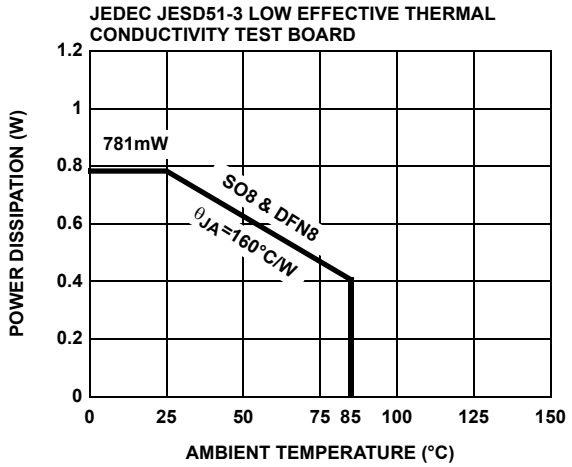


FIGURE 28. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL1510 is a dual operational amplifier designed for line driving in DMT ADSL solutions. It is a dual current mode feedback amplifier with low distortion while drawing moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL1510 closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3dB bandwidth is somewhat dependent on the power supply voltage.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input. This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL1510 when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not “seen” by the amplifier.

Feedback Resistor Values

The EL1510 has been designed and specified with R_F=1.5kΩ for A_V=+5. This value of feedback resistor yields extremely flat frequency response with no peaking out to 40MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. See the curves in the Typical Performance Curves section which show 3dB bandwidth and peaking vs frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifiers’ supply current and consequently 3dB bandwidth drop-off at high temperature, the EL1510 was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3dB bandwidth does not drop off drastically with temperature.

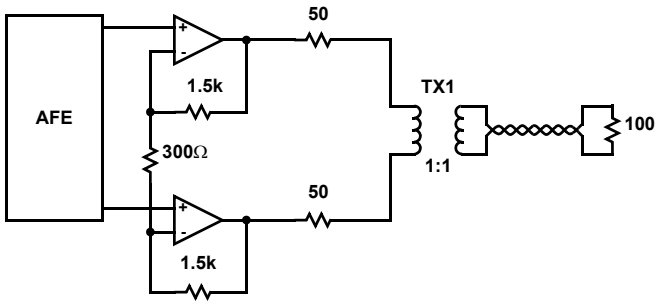
Supply Voltage Range and Operation

The EL1510 has been designed to operate with supply voltages from ±2.5V to ±12V. If a single supply is desired, values from +5V to +24V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL1510.

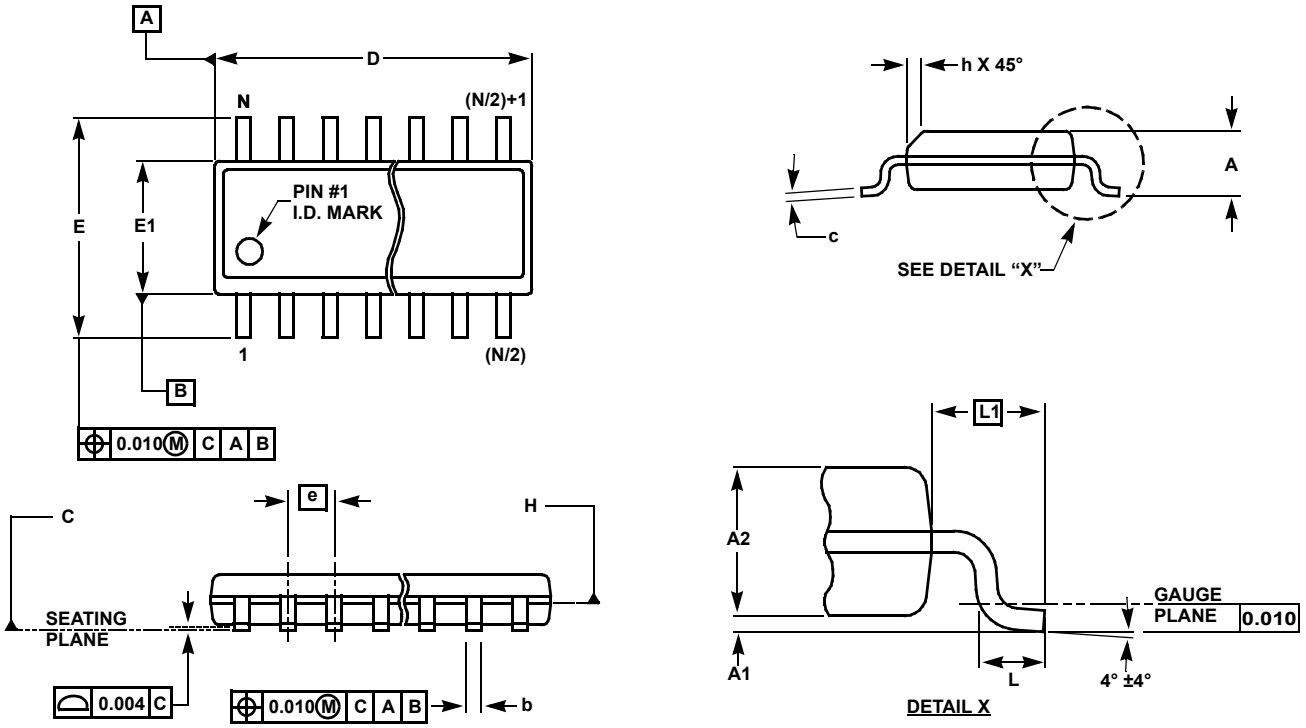
ADSL CPE Applications

The EL1510 is designed as a line driver for ADSL CPE modems. It is capable of outputting 400mA of output current with a typical supply voltage headroom of 1.8V. It can achieve -85dBc of distortion at low 7.5mA of supply current per amplifier.

The average line power requirement for the ADSL CPE application is 13dBm (20mW) into a 100Ω line. The average line voltage is 1.41V_{RMS}. The ADSL DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 7.5V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:1 is selected. The circuit configuration is as shown below.



Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

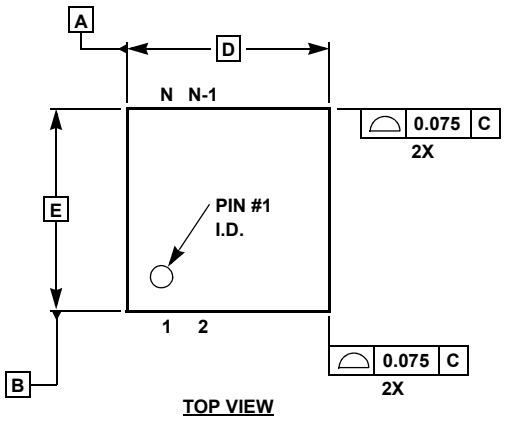
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

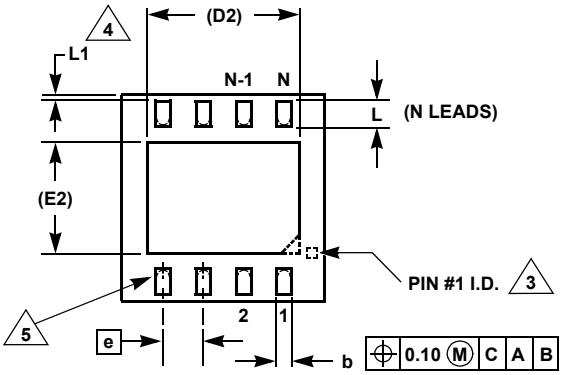
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

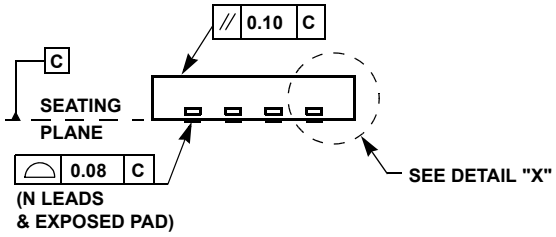
Dual Flat No-Lead Package Family (DFN)

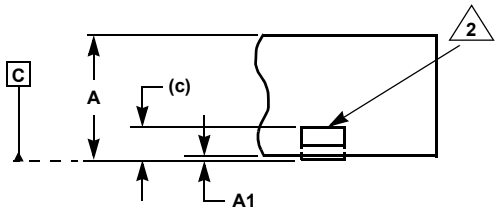


TOP VIEW



BOTTOM VIEW





DETAIL X

MDP0047

DUAL FLAT NO-LEAD PACKAGE FAMILY (JEDEC REG: MO-229)

SYMBOL	MILLIMETERS		TOLERANCE
	DFN8	DFN10	
A	0.85	0.90	±0.10
A1	0.02	0.02	+0.03/-0.02
b	0.30	0.25	±0.05
c	0.20	0.20	Reference
D	4.00	3.00	Basic
D2	3.00	2.25	Reference
E	4.00	3.00	Basic
E2	2.20	1.50	Reference
e	0.80	0.50	Basic
L	0.50	0.50	±0.10
L1	0.10	0	Maximum

Rev. 2 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Exposed lead at side of package is a non-functional feature.
3. Bottom-side pin #1 I.D. may be a diepad chamfer, an extended tiebar tab, or a small square as shown.
4. Exposed leads may extend to the edge of the package or be pulled back. See dimension “L1”.
5. Inward end of lead may be square or circular in shape with radius (b/2) as shown.
6. N is the total number of leads on the device.