

December 1996

Fast CMOS Bus Interface Latches

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (FCT2841 Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

These devices are buffered interface latches. These transparent latches with three-state outputs, are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When \overline{OE} is HIGH, the bus output is in the high impedance state. The CD74FCT841T and CD74FCT2841T are 10-bit latches, the CD74FCT843T is a 9-bit latch, and the CD74FCT845T is an 8-bit latch.

The CD74FCT2841T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT841ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT841BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT841CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841CTQM	-40 to 85	24 Ld QSOP	M24.15-P

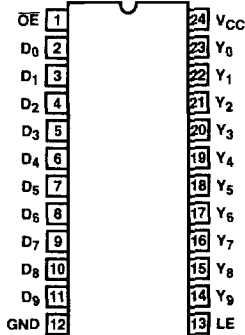
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

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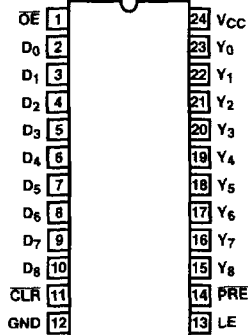
OCTAL 5V FCT
5V FCT 25Ω

Pinouts

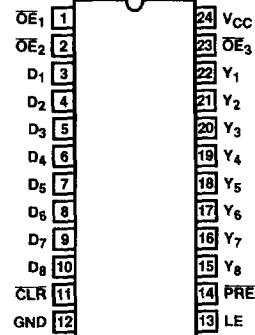
CD74FCT841T, CD74FCT2841T
(QSOP, SOIC)
TOP VIEW



CD74FCT843T
(QSOP, SOIC)
TOP VIEW



CD74FCT845T
(QSOP, SOIC)
TOP VIEW

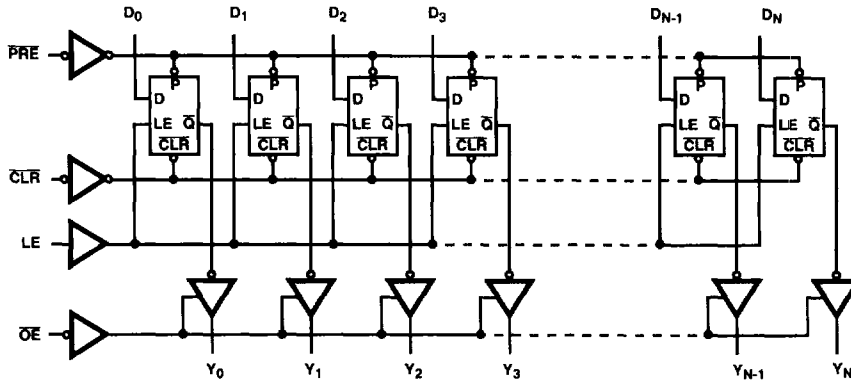


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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File Number 4177.2

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS	INTERNAL
	CLR	PRE	OE	LE	DN	YN	QN
High-Z	H	H	H	X	X	Z	X
	H	H	H	H	L	Z	L
	H	H	H	H	H	Z	H
Latched (High Z)	H	H	H	L	X	Z	NC
Transparent	H	H	L	H	L	L	L
	H	H	L	H	H	H	H
Latched	H	H	L	L	X	NC	NC
Preset	H	L	L	X	X	H	H
Clear	L	H	L	X	X	L	L
Preset	L	L	L	X	X	H	H
Latched (High Z)	L	H	H	L	X	Z	L
Latched (High Z)	H	L	H	L	X	Z	H

NOTE:

1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- NC = No Change
- Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
YN	Three-State Latch Outputs
DN	Latch Data Inputs
LE	Latch Enable Input
OE	Output Enable Control
CLR	Clear Latch
PRE	Preset Latch High, Preset Overrides CLR
GND	Ground
VCC	Power

CD74FCT841T, CD74FCT843T, CD74FCT845T, CD74FCT2841T

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4)	MAX	UNITS
					TYP		
Total Power Supply Current (Note 10)	I _C	V _{CC} = Max, Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = GND; LE = V _{CC} f _I = 5MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	1.8	4.5 (Note 9)	mA
		V _{CC} = Max, Outputs Open f _{CP} = 10MHz 50% Duty Cycle OE = GND; LE = V _{CC} Eight Bits Toggling f _I = 2.5MHz, 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	3.0	6.0 (Note 9)	mA
			V _{IN} = 3.4V V _{IN} = GND	-	5.0	14.0 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT		UNITS
			(NOTE 12)		(NOTE 12)		(NOTE 12)		
			MIN	MAX	MIN	MAX	MIN	MAX	
CD74FCT841T, CD74FCT2841T									
Propagation Delay D _N to Y _N (LE = HIGH)	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
Setup Time Data to LE	t _{SU}	C _L = 50pF R _L = 500Ω	2.5	-	2.5	-	2.5	-	ns
Hold Time Data to LE	t _H		2.5	-	2.5	-	2.5	-	ns
Propagation Delay LE to Y _N	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C _L = 300pF (Note 13) R _L = 500Ω	-	16.0	-	15.5	-	15.0	ns
LE Pulse Width (HIGH)(Note 3)	t _W	C _L = 50pF R _L = 500Ω	4.0	-	4.0	-	4.0	-	ns
Output Enable Time OE to Y _N	t _{PZH} , t _{PZL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
Output Disable Time(Note 3) OE to Y _N	t _{PHZ} , t _{PLZ}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns
		C _L = 5 pF (Note 13) R _L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns
CD74FCT843T, CD74FCT845T									
Propagation Delay D _N to Y _N (LE = HIGH)	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
Setup Time Data to LE	t _{SU}	C _L = 50pF R _L = 500Ω	2.5	-	2.5	-	2.5	-	ns
Hold Time Data to LE	t _H		2.5	-	2.5	-	2.5	-	ns

Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
Propagation Delay LE to Y _N	t _{PLH} , t _{PHL}	C _L = 50pF R _L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
Propagation Delay PRE to Y _N	t _{PLH}	C _L = 50pF R _L = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
Recovery Time PRE to Y _N	t _{REM}		1.5	11.0	1.5	10.0	1.5	9.0	ns
Propagation Delay CLR to Y _N	t _{PLH}		1.5	11.0	1.5	10.0	1.5	9.0	ns
Recovery Time(Note 13) CLR to Y _N	t _{REM}		1.5	13.0	1.5	10.0	1.5	9.0	ns
LE Pulse Width (Note 13) (HIGH)	t _w		4.0	-	4.0	-	4.0	-	ns
PRE Pulse Width (Note 13) (LOW)	t _w		5.0	-	4.0	-	4.0	-	ns
CLR Pulse Width (Note 13) (LOW)	t _w		4.0	-	4.0	-	4.0	-	ns
Output Enable Time OE to Y _N	t _{PZH} , t _{PZL}	C _L = 50pF R _L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C _L = 300pF (Note 13) R _L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
Output Disable Time (Note 13) OE to Y _N	t _{PHZ} , t _{PLZ}	C _L = 50pF R _L = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		C _L = 5pF (Note 13) R _L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

NOTES:

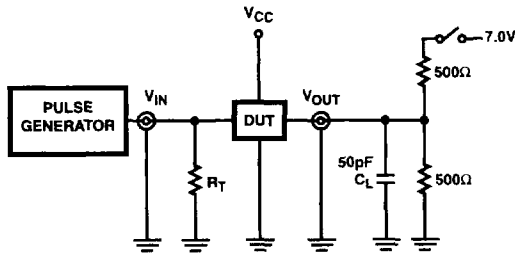
- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.

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OCTAL 5V FCT
5V FCT 25Ω

Test Circuits and Waveforms



NOTE:

14. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

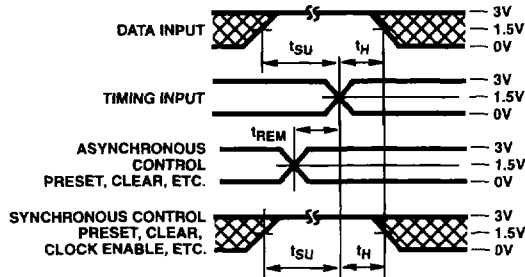


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

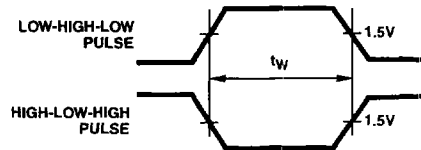


FIGURE 3. PULSE WIDTH

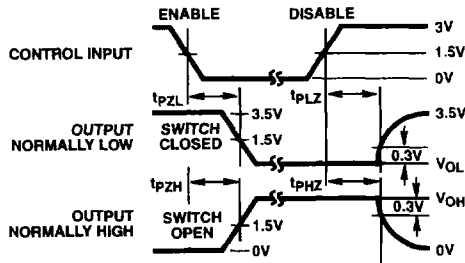


FIGURE 4. ENABLE AND DISABLE TIMING

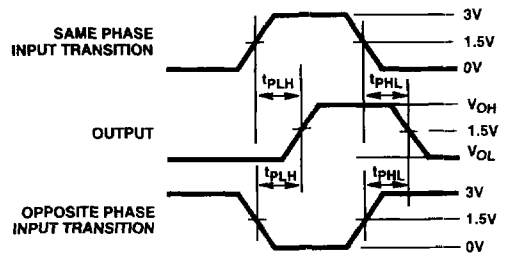


FIGURE 5. PROPAGATION DELAY