SanDisk®

iNAND™

e.MMC 4.41 I/F

Released Data Sheet
80-36-03433
V1.3

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REVISION HISTORY

Doc. No	Revision	Date	Description	Reference
80-36-03433	1.0	25-Feb-10	Preliminary	
80-36-03433	1.1	17-May-10	Released version. New device marking spec was added	
80-36-03433	1.2	12-Aug-10	Added X3 SKUs	
80-36-03433	1.3	16-Dec-10	Fixed 64GB P/N Added Max Enhanced Area Size for X3 Added System Performance numbers.	

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1. INTRODUCTION

1.1. General Description

iNAND is an Embedded Flash Drive (EFD) designed for mobile handsets and consumer electronic devices. iNAND is a hybrid device combining an embedded thin flash controller and standard MLC NAND flash memory, with an industry standard e.MMC 4.41[1] interface.

Empowered with a new e.MMC4.41 feature set such as Boot and RPMB partitions, HPI (implemented on MLC products only), and HW Reset the iNAND e.MMC is the optimal device for reliable code and data storage.

Designed specifically for mobile multimedia applications, iNAND is the most mature on board SD/MMC device since 2005, providing mass storage of up to 32GB in JEDEC compatible form factors, with low power consumption and high performance - an ideal solution for multimedia handsets of 2.5G, 3G, 3.5G and 4G.

In addition to the high reliability and high system performance offered by the current iNAND family of products, iNAND offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as advanced power management scheme.

iNAND uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by SanDisk's embedded flash management software running as firmware on the flash controller.

iNAND architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximize flash life expectancy.

SanDisk iNAND provides up to 32GB of memory for use in mass storage applications. In addition to the mass-storage-specific flash memory chip, iNAND includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

iNAND enables multimedia driven applications such as music, photo, video, TV, GPS, games, email, office and other applications.

The breakthrough in performance and design makes iNAND the ideal solution for mobile handset vendors, portable navigation and Automotive Infotainment vendors who require easy integration, fast time to market and high-capacity.

1.2. Plug-and-Play Integration

iNAND optimized architecture eliminates the need for complicated software integration and testing processes and enables a practically plug-and-play integration in the system. The replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This makes iNAND the perfect solution for platforms and reference designs, as it allows for the

[1] Compatible to JESD84-A441

utilization of more advanced NAND Flash technology with minimal integration or qualification efforts.

SanDisk iNAND is well-suited to meet the needs of small, low power, electronic devices. With JEDEC form factors measuring 12mm x 16mm (169 balls), 12x18mm (169 balls) and 11.5x13mm (153 balls) compatible with 0.5mm ball pitch, iNAND is fit for a wide variety of portable devices such as multi-media mobile handsets, personal media players, GPS devices and Automotive infotainment (car multimedia and car navigation).

To support this wide range of applications, iNAND is offered with an MMC/SD Interface.

The MMC interface allows for easy integration into any design, regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the SanDisk iNAND with MMC Interface.

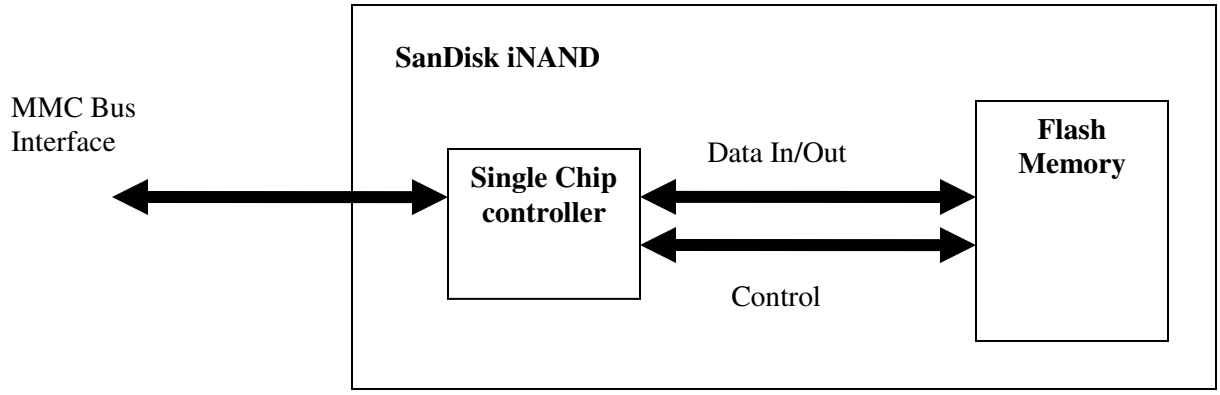


Figure 1 - SanDisk iNAND with MMC I/F Block Diagram

1.3. Feature Overview

SanDisk iNAND, with MMC interface, features include the following:

- Memory controller and NAND flash
- Complies with e.MMC Specification Ver. 4.41[2]
- Mechanical design complies with JEDED MO-276C Specification
- Offered in five TFBGA packages of e.MMC 4.41[3]
  - 11.5mm x 13mm x 1.2mm (2GB)
  - 12mm x 16mm x 1.2mm (4GB, 8GB, 16GB)
  - 14mm x 18mm x 1.4mm and 12mm x 18mm x 1.4mm (32GB)
  - 16mm x 20mm x 1.4mm (64GB)

[2] Refer to JEDEC Standards No. JESD84-A441

[3] Refer to JEDEC Standards No. JESD84-C441

- Operating temperature range: –25C° to +85C°
- Dual power system
- Core voltage (VCC) 2.7-3.6v
- I/O (VCCQ) voltage, either: 1.7-1.95v or 2.7-3.6v
- Up to 32 GB of data storage.
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed)
- Up to 52 MB/sec bus transfer rate (using 8 parallel data lines at 52 MHz)
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage

1.4. Functional Description

SanDisk iNAND contains a high-level, intelligent subsystem as shown in Figure 1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of storage devices. These capabilities include:

- Host independence from details of erasing and programming flash memory
- Sophisticated system for managing defects
- Sophisticated system for error recovery including a powerful ECC
- Power management for low power operation

1.5. Technology Independence

SanDisk iNAND uses 512 bytes as sector size. To write or read a sector (or multiple sectors), the host software simply issues a read or write command to the device. The command contains the address and number of sectors to write or read. The host software then waits for the command to complete.

There is no host software involvement in the details of flash operations such as erase, program or read. This is extremely important since flash devices are becoming increasingly complex with current advanced NAND MLC processes. Because iNAND uses an intelligent on-board controller, host system software will not need to be updated as new flash memory evolves. In other words, systems that support iNAND technology today will be able to access future SanDisk devices built with new flash technology without having to update or change the host software.

1.6. Defect and Error Management

The SanDisk iNAND contains a sophisticated defect and error management system. If necessary, iNAND will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid state construction, give SanDisk iNAND unparalleled reliability.

1.7. MMC bus and Power Lines

SanDisk iNAND with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-A441.

The iNAND bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input
- VCCQ: VCCQ is the power supply line for host interface.
- VCC: VCC is the power supply line for internal flash memory.
- VDDi: VDDi is iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: ground lines.

1.7.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Symbol	Min	Max	Unit
Peak voltage on all lines		-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)		-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)		-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)		-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)		-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.5	0.5	V

2. E.MMC4.41 FEATURES OVERVIEW

2.1. Boot

iNAND supports e.MMC 4.41 boot operation modes, 1MB is size.

2.2. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. Typically the entrance to sleep mode occurs after 200ns, max value entering sleep mode is 850ms due to housekeeping operation. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.3. Sleep (CMD5)

An iNAND device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The Vcc power supply may be switched off in Sleep state is to enable even further system power consumption saving.

For additional information please refer JESD84-A441 section number 7.6.15

2.4. Enhanced Reliable Write

iNAND supports enhanced reliable write as defined in e.MMC 4.41 spec[4].

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.5. Secure Erase

In addition to the standard erase command the iNAND supports the optional Secure Erase command[5].
The Secure Erase command differs from the basic Erase command in that it requires the iNAND to execute the erase operation on the memory array when the command is issued and requires the iNAND and host to wait until the operation is complete before moving to the next iNAND operation.

[4] For additional information refer to JEDEC Standards No. JESD84-A441

[5] For additional information refer to JEDEC Standards No. JESD84-A441

The secure erase command requires the iNAND to perform a secure purge operation on the erase groups, and copy items identified for erase, in those erase groups .
A purge operation is defined as overwriting addressable locations with a single character and then performing an erase.

This new command meets high security application requirements (e,g, those used by military and government customers) that once data has been erased, it can no longer be retrieved from the device.

2.6. Secure Trim

The Secure Trim[6] command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups. The size of a write block in the iNAND device is 512B

2.7. Trim

The Trim function is similar to the Erase command but applies the erase operation to write blocks instead of erase groups. The size of a write block in the INAND device is 512B

For additional information on the Trim function, refer to JEDEC standards No. JESD84-A441

2.8. Partition management

The iNAND offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows[7]:

- Factory configuration supplies two boot partitions, each 1MB in size, implemented as enhanced storage media and one RPMB partitioning of 128KB in size.
- The host is free to configure one segment in the User Data Area to be implemented as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size and attributes can be programmed once in device life-cycle (one-time programmable). Each of the General Purpose Area Partitions can be implemented with enhanced technological features.

2.9. Enhanced Write Protection

To allow the host to protect data against erase or write, the iNAND supports two levels of write protect command[8]:

[6] For additional information refer to JEDEC Standards No. JESD84-A441

[7] For additional information refer to JEDEC Standards No. JESD84-A441

[8] For additional information refer to JEDEC Standards No. JESD84-A441

- The entire iNAND (including the Boot Area Partitions, General Purpose Area Partition, and User/Enhanced User Data Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD.
- Specific segments of the iNAND may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

For additional information please refer JESD84-A441 standard.

2.10. High Priority Interrupt (HPI)

Many operating-systems use demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in JESD84-A441 enables low read latency operation by suspending a lower priority operation before it is actually completed. This mechanism can reduce read latency, in typical condition to below 10msec.

For additional information on the HPI function, refer to JESD84-A441 standard section 7.6.20

Note: HPI is implemented on MLC products only

2.11. H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that was set as power-on write protect before the reset was asserted. For more information, refer to JESD84-A441 standard.

2.12. DDR I/F

Support DDR signaling to double bus performance. For additional information please refer to JESD84-A441 standard.

3. PRODUCT SPECIFICATIONS

3.1. Typical Power Requirements

Table 3 - iNAND Power Requirements (Ta=25°C@3.3V)

		Max Value	Measurement
Auto Sleep mode		350	uA
Sleep (CMD5)		200 (Max) 130 (Typical)	uA
Read	Default Speed	100	mA
	High-Speed	200	mA
Write	Default Speed	100	mA
	High-Speed	200	mA
VCC (ripple: max, 60mV peak-to-peak) 2.7 V – 3.6 V			

Note 1: Current measurements are average over 100 mSecs.

Note 2: Sleep is measured at room temperature

Note 3: In sleep state, triggered by CMD5, Flash Vcc power supply is switched off

3.2. Operating Conditions

3.2.1. Operating and Storage Temperature Specifications

Table 4 - Operating and Storage Temperatures

Temperature	Operating	-25° C to 85° C
	Non-Operating: After soldered onto PC Board	-40° C to 85° C

3.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND is MSL = 3.

3.3. System Performance

All performance values for iNAND in Table 5 were measured under the following conditions:

- Voltage range:

  Core voltage (VCC): 2.7-3.6v

  Host voltage (VCCQ), either: 1.7-1.95v or 2.7-3.6v
- Operating temperature -25° C to 85° C

Table 5a - System Performance

Capacity	X2		X3	
	Sustained Write	Sustained Read	Sustained Write	Sustained Read
4GB	9MB/s	20MB/s	5MB/s	20MB/s
8/16/32/64GB	9MB/s	20MB/s	8MB/s	20MB/s

Table 6b - System Timing Performance

Timing	Value
Block Read Access Time (MAX)	100 ms
Block Write Access Time (MAX)	250 ms
CMD1 to Ready after Power-up (MAX)	1000 ms

Physical Specifications

The SanDisk iNAND is a 169-pin, thin fine-pitched ball grid array (BGA). See Figure 2, Figure 3 and Table 7 for physical specifications and dimensions.

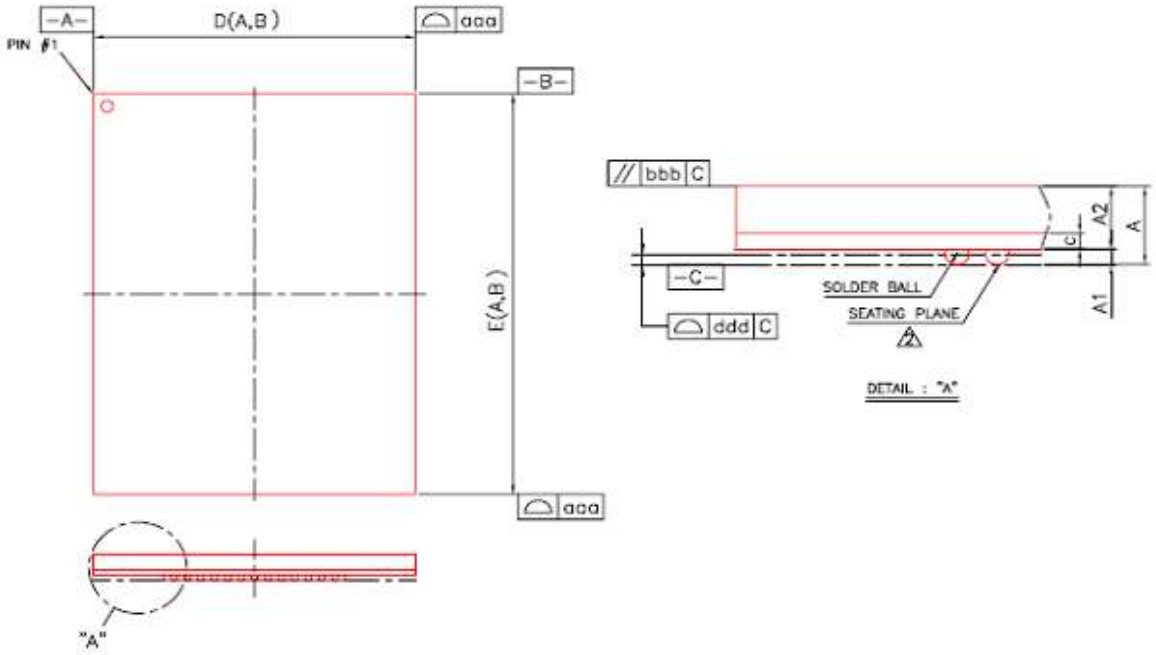
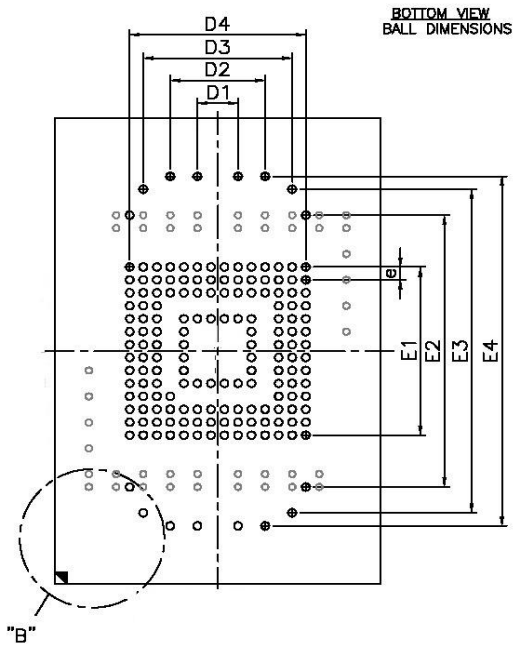


Figure 2- INAND Specification Top and Side View (Detail A)



Legend	
○	Ball
○	Test Pad (for SanDisk internal use only).

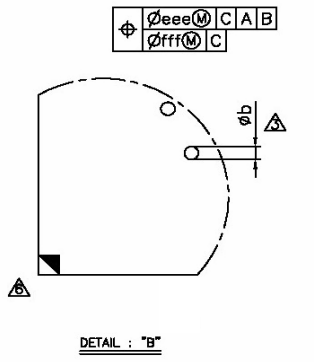


Figure 3- Package Outline Drawing – bottom view

Table 7 - iNAND Package Specification

		Dimension in millimeters			Dimension in inches		
Package Size	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
All	A	---	---	1.20[1]	---	---	0.047
All	A1	0.17	0.22	0.27	0.007	0.009	0.011
12X18mm	A2	0.98	1.03	1.08	0.038	0.040	0.042
12X16mm 11.5X13mm	A2	0.785	0.835	0.885	0.031	0.033	0.035
12X18mm	C	0.10	0.13	0.16	0.004	0.005	0.006
12X16mm 11.5X13mm	C	0.17	0.21	0.25	0.007	0.008	0.010
12X18mm 12X16mm	D(A)	11.93	12.00	12.07	0.470	0.472	0.476
11.5X13mm	D(B)	11.43	11.5	11.57	0.450	0.453	0.456
12X16mm	E(A)	15.93	16.00	16.07	0.627	0.630	0.633
12X18mm	E(B)	17.90	18.00	18.10	0.706	0.709	0.713
11.5X13mm	E(C)	12.93	13.00	13.07	0.509	0.512	0.515
12X18mm 12X16mm	D1	---	1.50	---	---	0.059	---
12X18mm 12X16mm	D2	---	3.50	---	---	0.138	---
12X18mm 12X16mm	D3	---	5.50	---	---	0.217	---
All	D4	---	6.50	---	---	0.256	---
All	E1	---	6.50	---	---	0.256	---
12X18mm 12X16mm	E2	---	10.50	---	---	0.413	---
12X18mm 12X16mm	E3	---	12.50	---	---	0.492	---
12X18mm 12X16mm	E4	---	13.50	---	---	0.531	---
All	E	---	.50	---	---	0.020	---
All	B	0.25	0.30	0.35	0.010	0.012	0.014
All	Aaa	0.10			0.004		

1 For SDIN5B2-32G maximum device height (A) is 1.40 mm

		Dimension in millimeters	Dimension in inches
All	Bbb	0.10	0.004
All	Ddd	0.08	0.003
All	Eee	0.15	0.006
All	Fff	0.05	0.002
All	MD/ME	14/14	14/14

4. INTERFACE DESCRIPTION

4.1. MMC I/F Ball Array

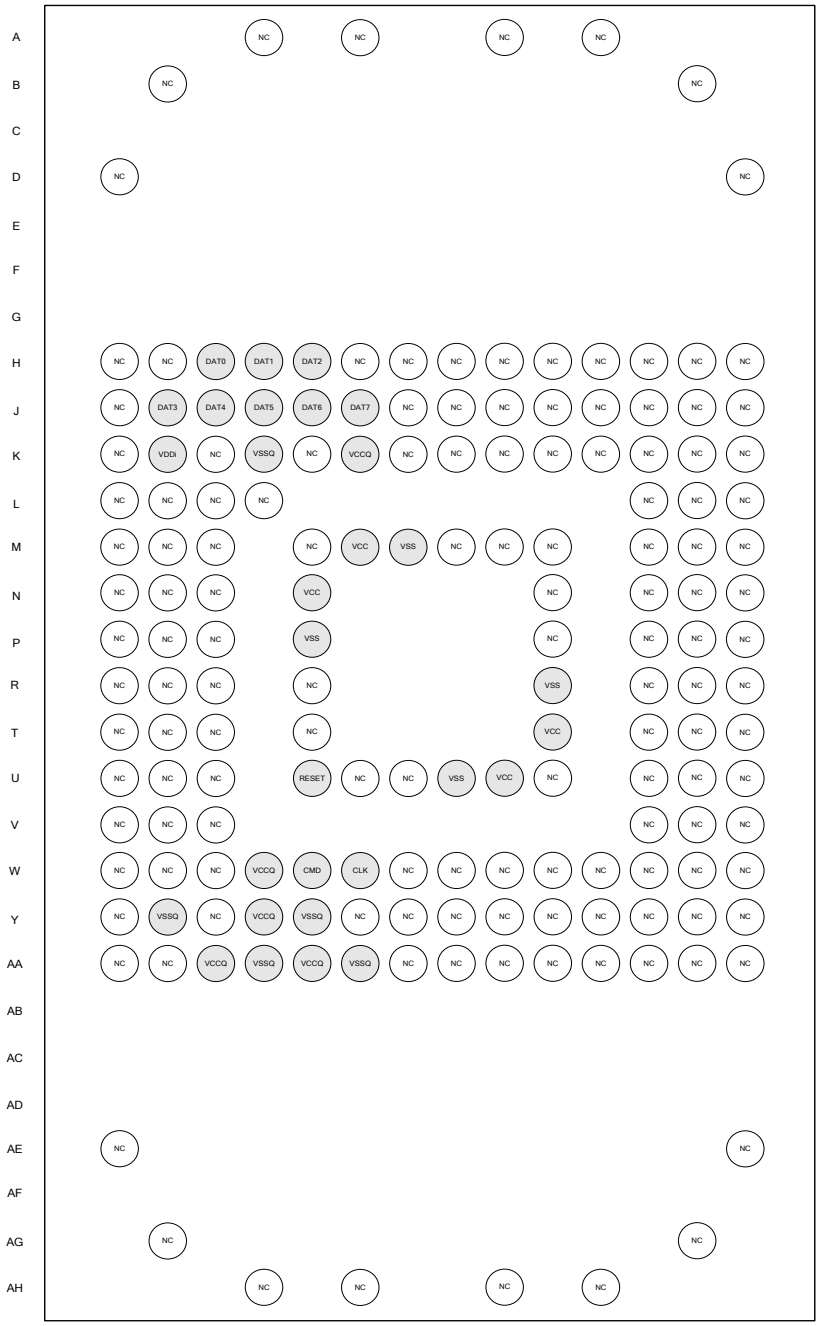


Figure 4 - 169 balls - Ball Array (Top View)

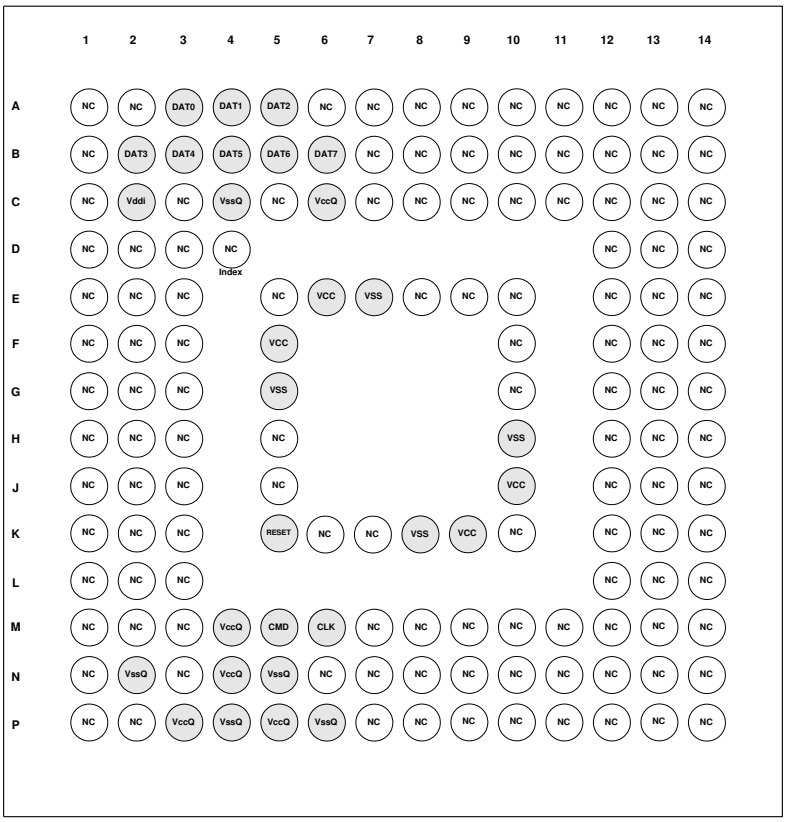
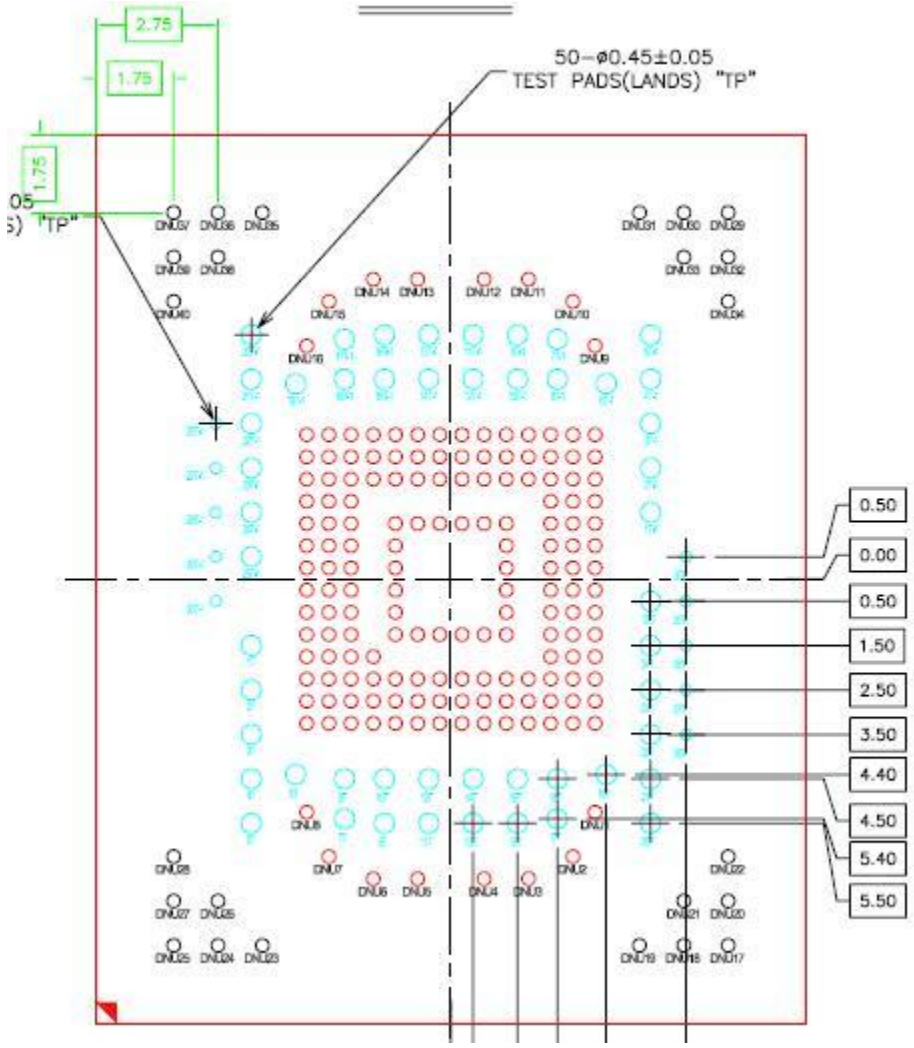


Figure 7 - 153 balls - Ball Array (Top View)

iNAND with 16x20x1.4mm package size contains an additional 24 Not-Connected balls that optimizes the device's bond with the PCB. The additional balls are located in the four corners of the device as shown in the following figure:



24 Not-Connected balls in 16x20x1.4mm package (Bottom View)

4.2. Pins and Signal Description

4.2.1. Table 9 contains the SanDisk iNAND, with MMC interface (153 balls), functional pin assignment.

Table 8 – Functional Pin Assignment, 153 balls

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n		Hardware Reset
E6	VCC	Supply	Flash I/O and memory power supply
F5	VCC		
J10	VCC		
K9	VCC		
D6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection
G5	VSS		
H10	VSS		
K8	VSS		
C4	VSSQ		Memory controller core and MMC I/F ground connection
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground

Note: All other pins are not connected [NC] and can be connected to GND or left floating.

4.2.2. Table 10 contains the SanDisk iNAND, with MMC interface (169 balls), functional pin assignment.

Table 10 – Functional Pin Assignment, 169 balls

Ball No.	Ball Signal	Type	Description
H3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
H4	DAT1		
H5	DAT2		
J2	DAT3		
J3	DAT4		
J4	DAT5		
J5	DAT6		
J6	DAT7		
W5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
W6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
U5	RST_n		Hardware Reset
M6	VCC	Supply	Flash I/O and memory power supply
N5	VCC		
T10	VCC		
U9	VCC		
K6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
W4	VCCQ		
Y4	VCCQ		
AA3	VCCQ		
AA5	VCCQ		
M7	VSS	Supply	Flash I/O and memory ground connection
P5	VSS		
R10	VSS		
U8	VSS		
K4	VSSQ		Memory controller core and MMC I/F ground connection
Y2	VSSQ		
Y5	VSSQ		
AA4	VSSQ		
AA6	VSSQ		
K2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground

Note: All other pins are not connected [NC] and can be connected to GND or left floating.

4.3. iNAND Registers

4.3.1. OCR Register

Value for 4GB-32GB: 0xC0FF8080

Value for 2GB: 0x40FF8080

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready

Parameter	OCR slice	Description	Value	**Width**
Access Mode	[30:29]	Access mode	<=2GB 00b >2GB 10b	2
	[23:15]	VDD: 2.7 - 3.6 range	111111111b	9
	[14:8]	VDD: 2.0 - 2.6 range	0000000b	7
	[7]	VDD: 1.7 - 1.95 range	1b	1

4.3.2. CID Register

Parameter	**CID slice**	**Description**	**Value**	**Width**
MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Card BGA	01h	2
OID	[111:104]	OEM/Application ID	0000h	8
PNM	[103:56]	Product name	2GB: 53454d303247h ("SEM02G") 4GB: 53454d303447h ("SEM04G") 8GB: 53454d303847h ("SEM08G") 16GB: 53454d313647h ("SEM16G") 32GB: 53454d333247h ("SEM32G")	48
PRV	[55:48]	Product revision	90h	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	CRC7 checksum	0000000b	7

4.3.3. DSR Register

Parameter	**DSR slice**	**Description**	**Value**	**Width**
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

DSR is not implemented; in case of read, value of 0x0404 will be returned.

4.3.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	11b	3
SPEC_VERS	[125:122]	System specification version	0100b	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	0F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h – Not 2GB Ah – for 2GB	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	0
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	0
DSR_IMP	[76:76]	DSR implemented	0b	0
*C_SIZE	[73:62]	Device size	2GB-E97h >2GB FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	111b	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	111b	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	111b	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	111b	3
C_SIZE_MULT	[49:47]	Device size multiplier	111b	3
ERASE_GRP_SIZE	[46:42]	Erase group size	11111b	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	2GB 00111b 4GB 01111b >=8GB 11111b	5
WP_GRP_SIZE	[36:32]	Write protect group size	11111b	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1b	1
DEFAULT_ECC	[30:29]	Manufacturer default	00b	2
R2W_FACTOR	[28:26]	Write speed factor	100b	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0b	1
CONTENT_PROT_APP	[16:16]	Content protection application	0b	1
FILE_FORMAT_GRP	[15:15]	File format group	0b	1
COPY	[14:14]	Copy flag (OTP)	1b	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0b	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0b	1
FILE_FORMAT	[11:10]	File format	00b	2
ECC	[9:8]	ECC code	00b	2
CRC	[7:1]	Calculated CRC	0000000b	7

4.3.5. EXT_CSD Register

Parameter	ECSD slice [bytes]	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	0h
BKOPS_STATUS	[246]	Background operations status	Default = 0h Updated in Run time
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h Updated in Run time
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	Ah
TRIM _MULT	[232]	TRIM Multiplier	1h
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	15h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	96h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	96h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULTI	[226]	Boot partition size	8h
ACCESS_SIZE	[225]	Access size	6h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	Table 9
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	1h
REL_WR_SEC_C	[222]	Reliable write sector count	1h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	Table 9
S_C_VCC	[220]	Sleep current [VCC]	8h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
S_A_TIMEOUT	[217]	Sleep/Awake time out	11h
SEC_COUNT	[215:212]	Sector count	Table 9
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0h

Parameter	ECSD slice [bytes]	Description	Value
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	0h
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition switching timing	1h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	1h
CARD_TYPE	[196]	Card Type	7h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	5h
CMD_SET	[191]	Command Set	0h
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	0h
HS_TIMING	[185]	High Speed Interface Timing	0h
BUS_WIDTH	[183]	Bus Width Mode	0h
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	0h
BOOT_CONFIG_PROT	[178]	Boot config protection	0h
BOOT_BUS_WIDTH	[177]	Boot bus width1	0h
ERASE_GROUP_DEF	[175]	High-density erase group definition	0h
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	1h
WR_REL_SET	[167]	Write reliability setting register	0h
WR_REL_PARAM	[166]	Write reliability parameter register	0h
BKOPS_START	[164]	Manually start background operations	0h
BKOPS_EN	[163]	Enable background operations handshake	0h
RST_n_FUNCTION	[162]	H/W reset function	0h
HPI_MGMT	[161]	HPI management	0h
PARTITIONING SUPPORT	[160]	Partitioning support	3h
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	<table><tr><td></td><td>X2</td><td>X3</td></tr><tr><td>2GB</td><td>E8h</td><td>NA</td></tr><tr><td>4GB</td><td>ECh</td><td>99h</td></tr><tr><td>8GB</td><td>ECh</td><td>9Ah</td></tr><tr><td>16GB</td><td>EDh</td><td>9Ah</td></tr><tr><td>32GB</td><td>EDh</td><td>9Ah</td></tr><tr><td>64GB</td><td>NA</td><td>98h</td></tr></table>
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	0h

Parameter	ECSD slice [bytes]	Description	Value
GP_SIZE_MULT	[154:143]	General Purpose Partition Size	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h

The following table shows the capacity available for user data for the various device capacities:

Table 9: Capacity for User Data*

Capacity	LBA [Hex]	LBA [Dec]	Capacity [Bytes]
SDIN5D2-2G	0x3A6000	3,825,664	1,958,739,968
SDIN5C2-4G	0x75F000	7,729,152	3,957,325,824
SDIN5C2-8G	0xECB000	15,511,552	7,941,914,624
SDIN5C2-16G	0x1DA9000	31,100,928	15,923,675,136
SDIN5B2-32G	0x3B6F000	62,320,640	31,908,167,680
SDIN5C1-4G	0x760000	7,733,248	3,959,422,976
SDIN5C1-8G	0xECC000	15,515,648	7,944,011,776
SDIN5C1-16G	0x1DAA000	31,105,024	15,925,772,288
SDIN5E1-32G	0x3B70000	62,324,736	31,910,264,832
SDIN5F1-64G	0x74F0000	122,617,856	62,780,342,272

***Note**: Exported capacity numbers in Table 11 are the Factory Default exported capacity. By implementing Enhanced User Data Area the exported capacity is reduced.

Table 10: Write protect group size

SKU	HC_ERASE_GROUP _SIZE	HC_WP_GRP_ SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
SDIN5D2-2G	4h	2h	2MB	4MB
SDIN5C2-4G	4h	4h	2MB	8MB
SDIN5C2-8G	4h	8h	2MB	16MB
SDIN5C2-16G	4h	10h	2MB	32MB
SDIN5B2-32G	4h	20h	2MB	64MB
SDIN5C1-4G	8h	2h	4MB	8MB
SDIN5C1-8G	8h	4h	4MB	16MB
SDIN5C1-16G	8h	8h	4MB	32MB
SDIN5E1-32G	8h	10h	4MB	64MB
SDIN5F1-64G	8h	20h	4MB	128MB

5. POWER DELIVERY AND CAPACITOR SPECIFICATIONS

5.1. SanDisk iNAND Power Domains

SanDisk iNAND has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 11.

Table 11 - Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges:
		High Voltage Region: 3.3V (nominal)
		Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range:
		High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

5.2. Capacitor Connection Guidelines

5.2.1. VDDi Connections

The VDDi (C2/K2) ball must only be connected to an external capacitor that is connected to VSS. This signal may not be left floating. The capacitor's specifications and its placement instructions are detailed below.

The capacitor is part of an internal voltage regulator that provides power to the controller.

Caution: Failure to follow the guidelines below, or connecting the VDDi ball to any external signal or power supply, may cause the device to malfunction.

The trace requirements for the VDDi (C2/K2) ball to the capacitor are as follows:

- Resistance: <2 ohm
- Inductance: <5 nH

The capacitor requirements are as follows:

- Capacitance: >=0.1 uF
- Voltage Rating: >=6.3 V
- Dielectric: X7R or X5R

5.2.2. VCC and VCCQ Connections

- All VCC balls should be connected to a 3.3V supply
- All VCCQ balls should be connected either to a 3.3V or 1.8V supply

SanDisk recommends providing separate bypass capacitors for each power domain as shown in Figure 8

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends on your PCB layout. Also, for clarity, the diagram does not show the VSS connection. All balls marked VSS should be connected to a ground (GND) plane.

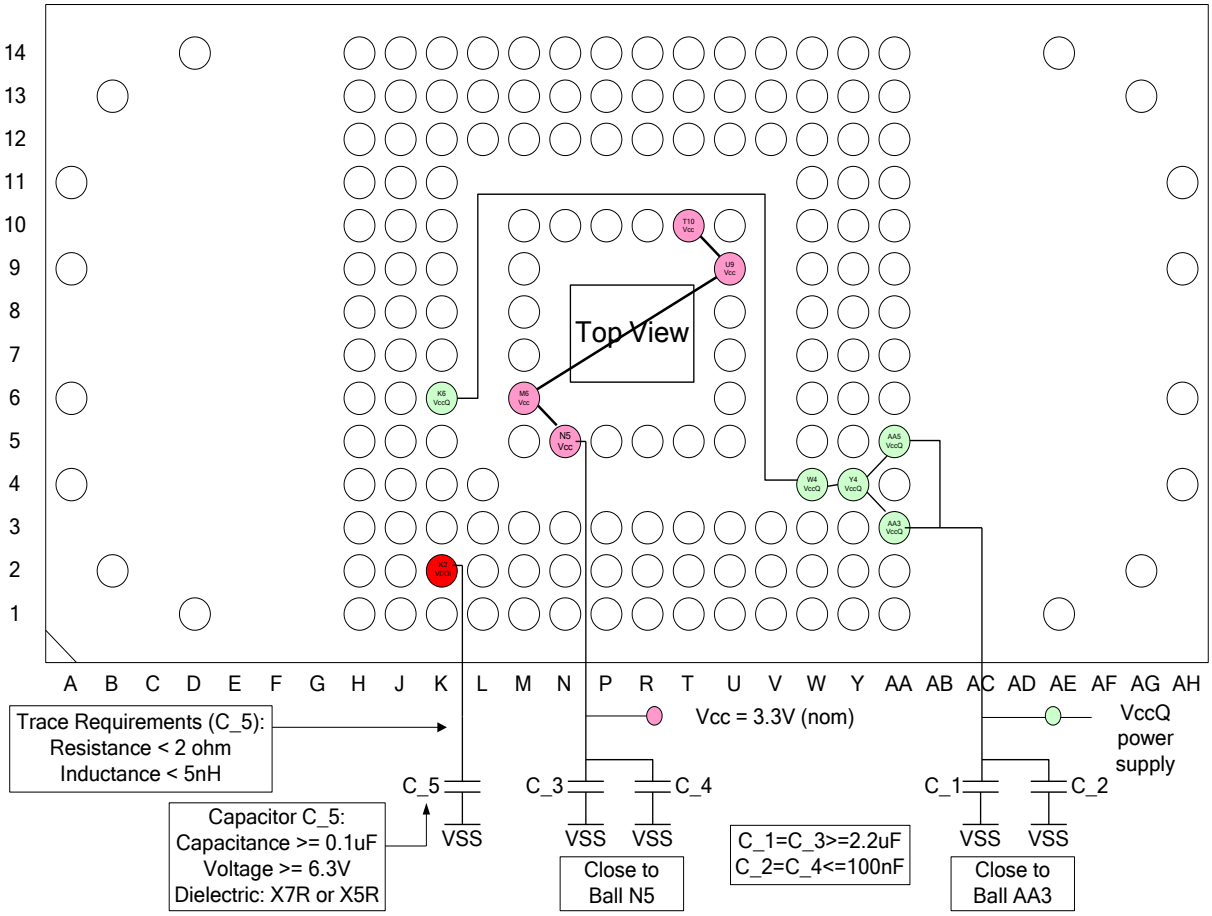


Figure 8- Recommended Power Domain Connections

6. MARKING

First row: Simplified SanDisk Logo

Second row: Sales item P/N

Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'

* No ES marking for product in mass production.

Fourth row: Y- Last digit of year

WW- Work week

D- A day within the week.

MLLXXX – Internal use

2D barcode: Store the 10 Digital unique ID information as reflected in the fourth row.

Figure 9: Product marking

7. ORDERING INFORMATION

Table 12 – Ordering Information

Capacity	Technology	Part Number	Package
2GB	X2	SDIN5D2-2G	11.5 mm x 13 mm x 1.2 mm
4GB	X2	SDIN5C2-4G	12 mm x 16 mm x 1.2 mm
	X3	SDIN5C1-4G	12 mm x 16 mm x 1.2 mm
8GB	X2	SDIN5C2-8G	12 mm x 16 mm x 1.2 mm
	X3	SDIN5C1-8G	12 mm x 16 mm x 1.2 mm
16GB	X2	SDIN5C2-16G	12 mm x 16 mm x 1.2 mm
	X3	SDIN5C1-16G	12 mm x 16 mm x 1.2 mm
32GB	X2	SDIN5B2-32G	12 mm x 18 mm x 1.4 mm
	X3	SDIN5E1-32G	14 mm x 18 mm x 1.4 mm
64GB	X3	SDIN5F1-64G	16 mm x 20 mm x 1.4 mm

Note: Suffix “T” added to the P/N indicates tape/reel. For example, SDIN5C2-8G would become SDIN5C2-8G-T. The default P/Ns in Table 14 are shipped in trays.

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