# High Accuracy, Dual-Axis Digital Inclinometer and Accelerometer

Data Sheet

# ADIS16209

## FEATURES

**Dual-mode inclinometer system**
**Dual-axis, horizontal operation, ±90°**
**Single-axis, vertical operation, ±180°**
**High accuracy, 0.1°**
**Digital inclination data, 0.025° resolution**
**Digital acceleration data, 0.244 m*g* resolution**
**±1.7 *g* accelerometer measurement range**
**Digital temperature sensor output**
**Digitally controlled bias calibration**
**Digitally controlled sample rate**
**Digitally controlled frequency response**
**Dual alarm settings with rate/threshold limits**
**Auxiliary digital I/O**
**Digitally activated self-test**
**Digitally activated low power mode**
**SPI-compatible serial interface**
**Auxiliary 12-bit ADC input and DAC output**
**Single-supply operation: 3.0 V to 3.6 V**
**3500 *g* powered shock survivability**

## APPLICATIONS

**Platform control, stabilization, and alignment**
**Tilt sensing, inclinometers, leveling**
**Motion/position measurement**
**Monitor/alarm devices (security, medical, safety)**
**Navigation**

## FUNCTIONAL BLOCK DIAGRAM

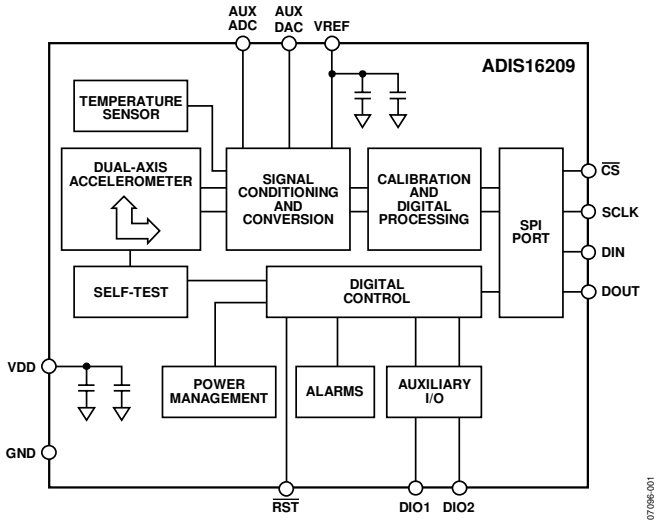


*Figure 1.*

## GENERAL DESCRIPTION

The ADIS16209 is a high accuracy, digital inclinometer that accommodates both single-axis (±180°) and dual-axis (±90°) operation. The standard supply voltage (3.3 V) and serial peripheral interface (SPI) enable simple integration into most industrial system designs. A simple internal register structure handles all output data and configuration features. This includes access to the following output data: calibrated acceleration, accurate incline angles, power supply, internal temperature, auxiliary analog and digital input signals, diagnostic error flags, and programmable alarm conditions.

Configurable operating parameters include sample rate, power management, digital filtering, auxiliary analog and digital output, offset/null adjustment, and self-test for sensor mechanical structure.

The ADIS16209 is available in a 9.2 mm × 9.2 mm × 3.9 mm LGA package that operates over a temperature range of −40°C to +125°C. It can be attached using standard RoHS-compliant solder reflow processes.

**Rev. H** **Document Feedback**


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## REVISION HISTORY

**3/2019—Rev. G to Rev. H**

Added Endnote 1, Table 1; Renumbered Sequentially ... 5
Deleted Figure 20; Renumbered Sequentially ... 11
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Added Introduction Section, Register Structure Section, Figure 20, SPI Section, Figure 21, Reading Sensor Data Section, Figure 22, Figure 23, and Device Configuration Section ... 12
Added Table 6 and Table 7; Renumbered Sequentially ... 12
Added Figure 24, Memory Structure Section, Figure 25, and Figure 26 ... 13
Moved Table 8 ... 14
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Change to the Power Supply Considerations Section ... 22
Added X-Ray Sensitivity Section ... 23
Changes to Ordering Guide ... 24

**8/2018—Rev. F to Rev. G**

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Added Figure 23; Renumbered Sequentially ... 19

**5/2017—Rev. E to Rev. F**

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Change to Basic Operation Section ... 11

**1/2015—Rev. D to Rev. E**

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Added Power-On Reset Function Section ... 19
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**6/2014—Rev. C to Rev. D**

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**7/2012—Rev. B to Rev. C**

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Updated Outline Dimensions ... 19

**8/2009—Rev. A to Rev. B**



**7/2008—Rev. 0 to Rev. A**



**3/2008—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = 25°C, VDD = 3.3 V, tilt = 0°, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| HORIZONTAL INCLINE | Each axis | | | | |
| Input Range | | | ±90 | | Degrees |
| Relative Accuracy[1] | ±30° from horizon, AVG_CNT = 0x08 | | ±0.1 | | Degrees |
| Sensitivity | ±30° from horizon | | 0.025 | | °/LSB |
| VERTICAL ROTATION | Rotational plane within ±30° of vertical | | | | |
| Input Range | | −180 | | +180 | Degrees |
| Relative Accuracy | 360° of rotation | | ±0.25 | | Degrees |
| Sensitivity | −40°C to +85°C | | 0.025 | | °/LSB |
| ACCELEROMETER | Each axis | | | | |
| Input Range[2] | 25°C | ±1.7 | | | *g* |
| Nonlinearity[2] | Percentage of full scale | | ±0.1 | ±0.2 | % |
| Alignment Error | X sensor to Y sensor | | ±0.1 | | Degrees |
| Cross Axis Sensitivity | | | ±2 | | % |
| Sensitivity | −40°C to +85°C, VDD = 3.0 V to 3.6 V | 0.243 | 0.244 | 0.245 | m*g*/LSB |
| ACCELEROMETER NOISE PERFORMANCE | | | | | |
| Output Noise | AVG_CNT = 0x00 | | 1.7 | | m*g* rms |
| Noise Density | AVG_CNT = 0x00 | | 0.19 | | m*g*/√Hz rms |
| ACCELEROMETER FREQUENCY RESPONSE | | | | | |
| Sensor Bandwidth | | | 50 | | Hz |
| Sensor Resonant Frequency | | | 5.5 | | kHz |
| ACCELEROMETER SELF-TEST STATE[3] | | | | | |
| Output Change When Active | At 25°C | 706 | 1343 | 1973 | LSB |
| TEMPERATURE SENSOR | | | | | |
| Output at 25°C | | | 1278 | | LSB |
| Scale Factor | | | −0.47 | | °C/LSB |
| ADC INPUT | | | | | |
| Resolution | | | 12 | | Bits |
| Integral Nonlinearity (INL) | | | ±2 | | LSB |
| Differential Nonlinearity (DNL) | | | ±1 | | LSB |
| Offset Error | | | ±4 | | LSB |
| Gain Error | | | ±2 | | LSB |
| Input Range | | 0 | | 2.5 | V |
| Input Capacitance | During acquisition | | 20 | | pF |
| ON-CHIP VOLTAGE REFERENCE | | | 2.5 | | V |
| Accuracy | At 25°C | −10 | | +10 | mV |
| Reference Temperature Coefficient | | | ±40 | | ppm/°C |
| Output Impedance | | | 70 | | Ω |
| DAC OUTPUT | 5 kΩ/100 pF to GND | | | | |
| Resolution | | | 12 | | Bits |
| Relative Accuracy | For Code 101 to Code 4095 | | 4 | | LSB |
| Differential Nonlinearity | | | 1 | | LSB |
| Offset Error | | | ±5 | | mV |
| Gain Error | | | ±0.5 | | % |
| Output Range | | | 0 to 2.5 | | V |
| Output Impedance | | | 2 | | Ω |
| Output Settling Time | | | 10 | | µs |

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{INL}$ | | | | 0.8 | V |
| Logic 1 Input High Current, $I_{INH}$ | $V_{IH}$ = 3.3 V | | ±0.2 | ±10 | µA |
| Logic 0 Input Low Current, $I_{INL}$ | $V_{IL}$ = 0 V | | | | |
| All Except $\overline{RST}$ | | | −40 | −60 | µA |
| $\overline{RST}$[4] | | | −1 | | mA |
| Input Capacitance, $C_{IN}$ | | | 10 | | pF |
| DIGITAL OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 1.6 mA | 2.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 1.6 mA | | | 0.4 | V |
| SLEEP TIMER | | | | | |
| Timeout Period[5] | | 0.5 | | 128 | Seconds |
| START-UP TIME[6] | Time until data is available | | | | |
| Power-On | Fast mode, SMPL_PRD ≤ 0x07 | | 150 | | ms |
| | Normal mode, SMPL_PRD ≥ 0x08 | | 190 | | ms |
| Reset Recovery | Fast mode, SMPL_PRD ≤ 0x07 | | 30 | | ms |
| | Normal mode, SMPL_PRD ≥ 0x08 | | 70 | | ms |
| Sleep Mode Recovery | | | 2.5 | | ms |
| FLASH MEMORY | | | | | |
| Endurance[7] | | 20,000 | | | Cycles |
| Data Retention[8] | $T_J$ = 85°C | 20 | | | Years |
| CONVERSION RATE SETTING | | 1.04 | | 2731 | SPS |
| POWER SUPPLY | | | | | |
| Operating Voltage Range | | 3.0 | 3.3 | 3.6 | V |
| Power Supply Current | Normal mode, SMPL_PRD ≥ 0x08 | | 11 | 14 | mA |
| | Fast mode, SMPL_PRD ≤ 0x07 | | 36 | 42 | mA |
| | Sleep mode, −40°C to +85°C | | 140 | 350 | µA |

[1] X-ray exposure may degrade this performance metric.
[2] Guaranteed by *i*MEMS® packaged part testing, design, and/or characterization.
[3] Self-test response changes as the square of VDD.
[4] The $\overline{RST}$ pin has an internal pull-up.
[5] Guaranteed by design.
[6] The times presented in this section represent the time it takes to start producing data in the output registers, after the minimum VDD reaches 3.0 V. They do not represent the settling time of the internal filters.
Note that for the default SENS_AVG and AVG_CNT settings, the typical settling time is ~1.28 seconds. For faster settling times, reduce the AVG_CNT and SMPL_PRD settings. Note that the trade-off associated with faster settling times is noise and power.
[7] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[8] Retention lifetime equivalent at junction temperature ($T_J$) 55°C as per JEDEC Standard 22 Method A117. Retention lifetime decreases with junction temperature.

## TIMING SPECIFICATIONS

$T_A$ = 25°C, VDD = 3.3 V, tilt = 0°, unless otherwise noted.

**Table 2.**

| Parameter | Description | Min[1] | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCLK}$ | Fast mode, SMPL_PRD ≤ 0x07 ($f_S$ ≥ 546 Hz)[2] | 0.01 | | 2.5 | MHz |
| | Normal mode, SMPL_PRD ≥ 0x08 ($f_S$ ≤ 482 Hz)[2] | 0.01 | | 1.0 | MHz |
| $t_{DATARATE}$ | Chip select period, fast mode, SMPL_PRD ≤ 0x07 ($f_S$ ≥ 546 Hz)[2] | 32 | | | µs |
| | Chip select period, normal mode, SMPL_PRD ≥ 0x08 ($f_S$ ≤ 482 Hz)[2] | 42 | | | µs |
| $t_{STALL}$ | Chip select period, fast mode, SMPL_PRD ≤ 0x07 ($f_S$ ≥ 546 Hz)[2] | 10 | | | µs |
| | Chip select period, normal mode, SMPL_PRD ≥ 0x08 ($f_S$ ≤ 482 Hz)[2] | 12 | | | µs |
| $t_{CS}$ | Chip select to clock edge | 48.8 | | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | | 100 | ns |
| $t_{DSU}$ | Data input setup time before SCLK rising edge | 24.4 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK rising edge | 48.8 | | | ns |
| $t_{DF}$ | Data output fall time | | 5 | 12.5 | ns |
| $t_{DR}$ | Data output rise time | | 5 | 12.5 | ns |
| $t_{SFS}$ | $\overline{CS}$ high after SCLK edge | 5 | | | ns |

[1] Guaranteed by design, not tested.
[2] Note that $f_S$ means internal sample rate.

## TIMING DIAGRAMS

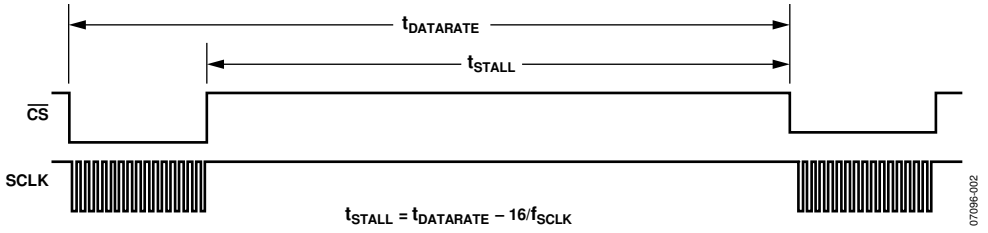



*Figure 2. SPI Chip Select Timing*

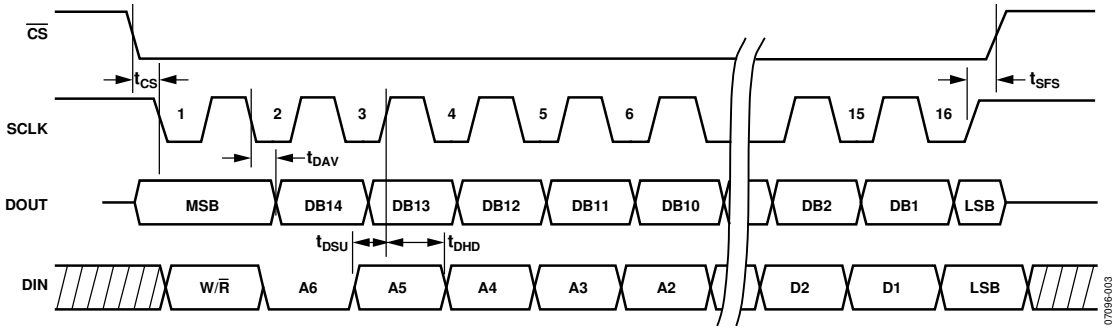



*Figure 3. SPI Timing*
*(Utilizing SPI Settings Typically Identified as Phase = 1, Polarity = 1)*

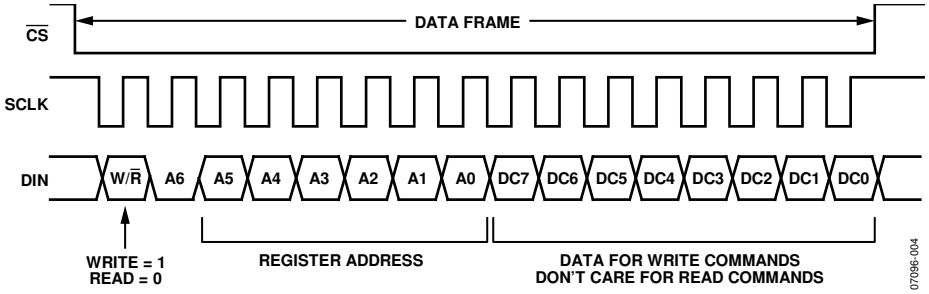



*Figure 4. DIN Bit Sequence*

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Acceleration (Any Axis, Unpowered) | 3500 *g* |
| Acceleration (Any Axis, Powered) | 3500 *g* |
| VDD to GND | −0.3 V to +7.0 V |
| Digital Input/Output Voltage to GND | −0.3 V to +5.3 V |
| Analog Inputs to GND | −0.3 to VDD + 0.3 V |
| Analog Inputs to GND | −0.3 to VDD + 0.3 V |
| Operating Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

**Table 4. Package Characteristics**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Device Weight |
|---|---|---|---|
| 16-Terminal LGA | 250°C/W | 25°C/W | 0.6 g |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

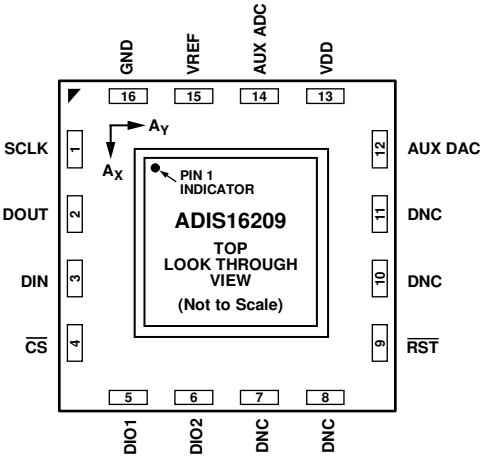



*Figure 5. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | SCLK | I | SPI, Serial Clock. |
| 2 | DOUT | O | SPI, Data Output. |
| 3 | DIN | I | SPI, Data Input. |
| 4 | $\overline{CS}$ | I | SPI, Chip Select. |
| 5, 6 | DIO1, DIO2 | I/O | Digital Input/Output Pins. |
| 7, 8, 10, 11 | DNC | N/A | Do not connect to this pin. |
| 9 | $\overline{RST}$ | I | Reset, Active Low. |
| 12 | AUX DAC | O | Auxiliary DAC Output. |
| 13 | VDD | S | Power Supply, 3.3 V. |
| 14 | AUX ADC | I | Auxiliary ADC Input. |
| 15 | VREF | O | Precision Reference. |
| 16 | GND | S | Ground. |

[1] S = supply; O = output; I = input.

## RECOMMENDED PAD GEOMETRY

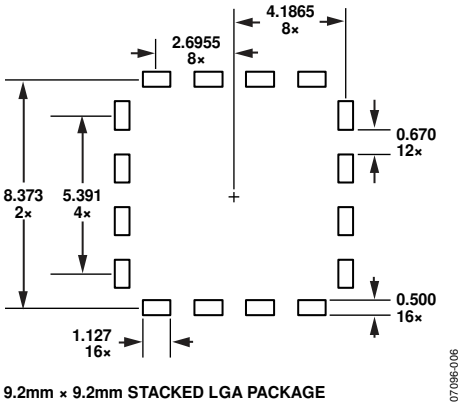



*Figure 6. Example of a Pad Layout*

# TYPICAL PERFORMANCE CHARACTERISTICS

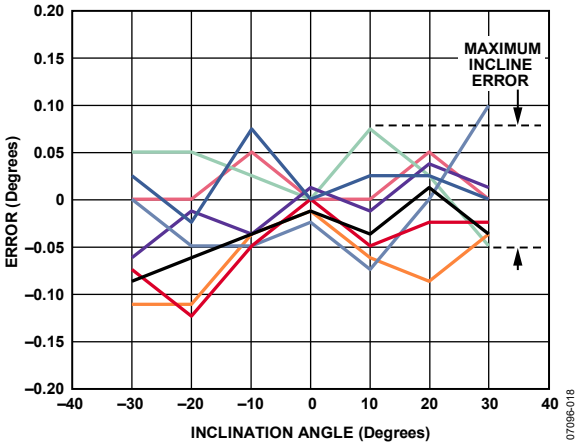



Figure 7. Horizontal Inclination Error (Eight Parts), Autonull at Horizontal Position, Stable Temperature, 3.3 V

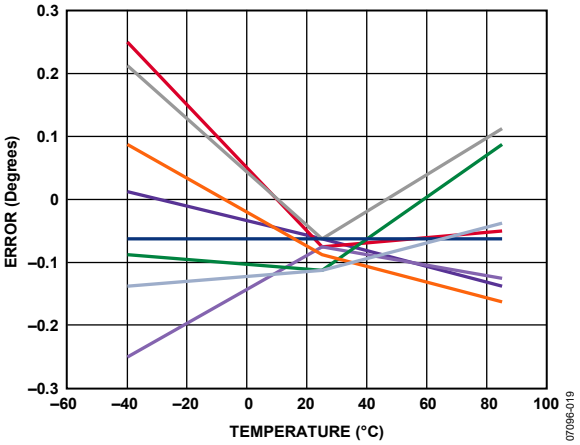



Figure 8. Maximum Incline Error Over a ±30° Incline Range (Eight Parts) Over Temperature, Autonull at Horizontal Position, 25°C, 3.3 V

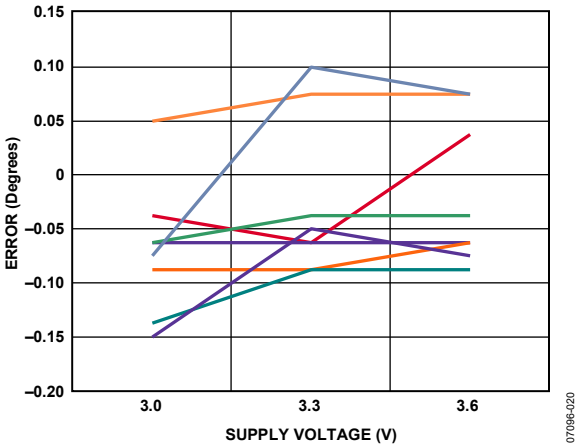



Figure 9. Maximum Incline Error Over a ±30° Incline Range (Eight Parts) Over Supply Voltage, Autonull Horizontal Position, 25°C, 3.3 V

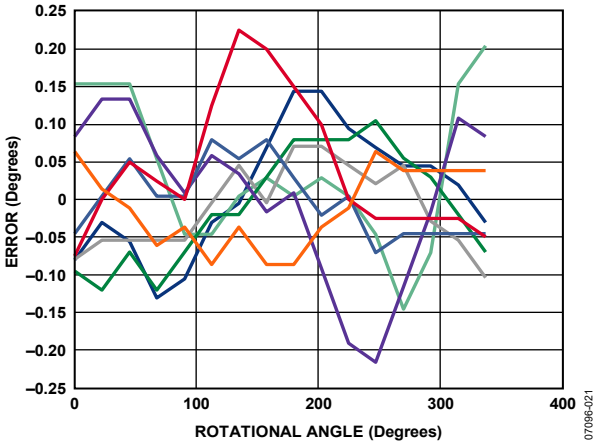



Figure 10. Vertical Mode Rotational Error (Eight Parts), 25°C, 3.3 V

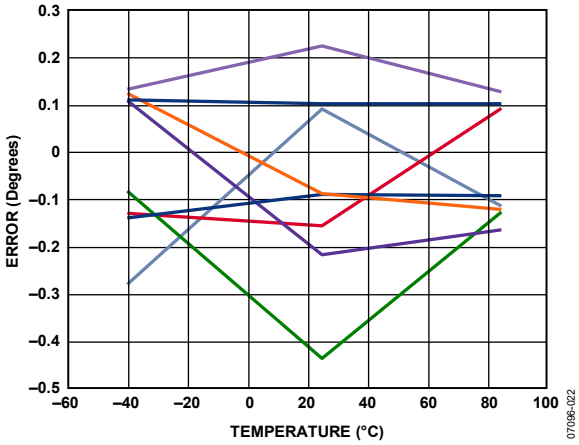



Figure 11. Vertical Mode Error (Eight Parts) vs. Temperature, 0° to 360°, 3.3 V

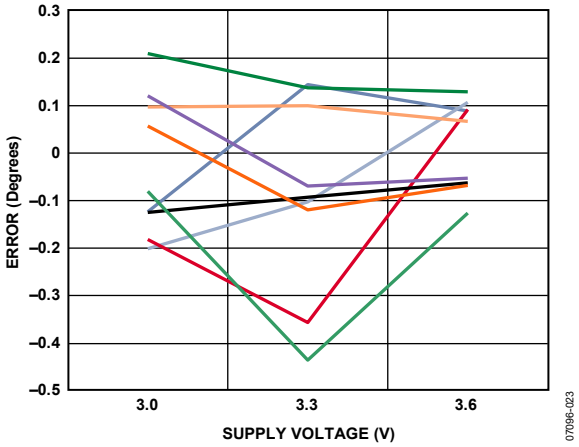



Figure 12. Vertical Mode Error (Eight Parts) vs. Supply Voltage, 0° to 360°, 25°C

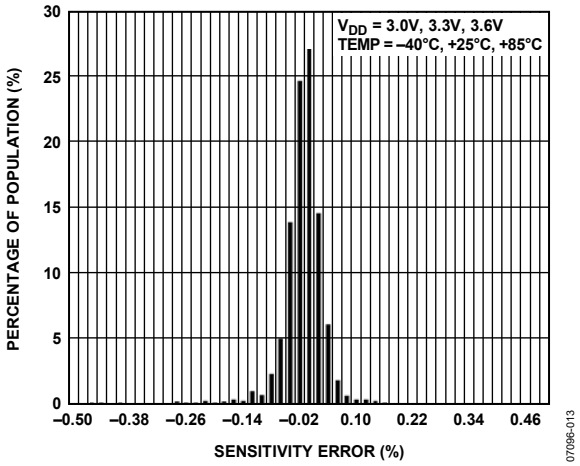



Figure 13. Accelerometer Output Sensitivity Error Distribution

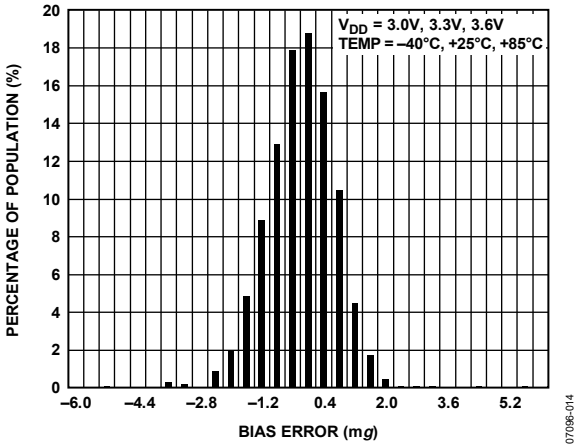



Figure 14. Accelerometer Output Bias Error Distribution

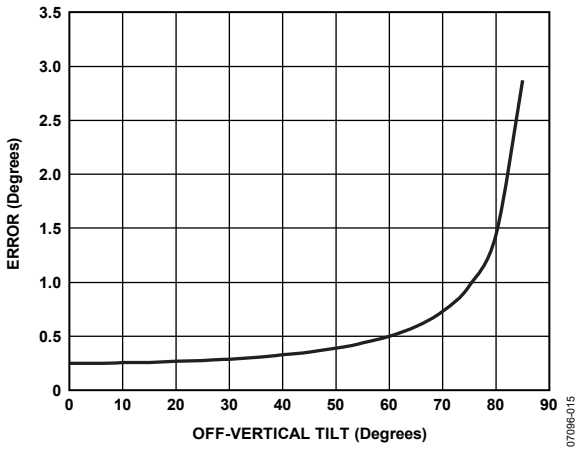



Figure 15. Error vs. Off-Vertical Tilt, 25°C, 3.3 V

# THEORY OF OPERATION

The ADIS16209 tilt sensing system uses gravity as its only stimulus, and a MEMS accelerometer as its sensing element. MEMS accelerometers typically employ a tiny, spring-loaded structure that is interlaced with a fixed pick-off finger structure. The spring constant of the floating structure determines how far it moves when subjected to a force. This structure responds to dynamic forces associated with acceleration and to static forces, such as gravity.

Figure 16 and Figure 17 illustrate how the accelerometer responds to gravity, according to its orientation, with respect to gravity. Figure 16 displays the configuration for the incline angle outputs, and Figure 17 displays the configuration used for the rotational angle position. This configuration provides greater measurement range than a single axis. The ADIS16209 incorporates the signal processing circuit that converts acceleration into an incline angle, and it corrects for several known error sources that would otherwise degrade the accuracy level.

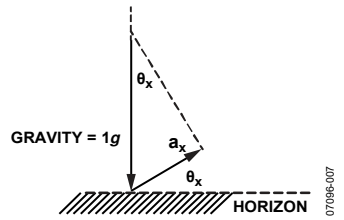



*Figure 16. Single-Axis Tilt Theory Diagram*

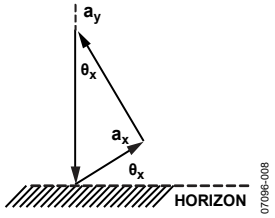



*Figure 17. Dual-Axis Tilt Theory Diagram*

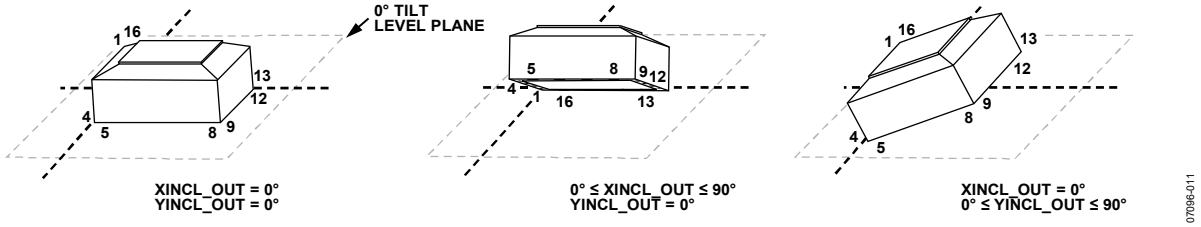
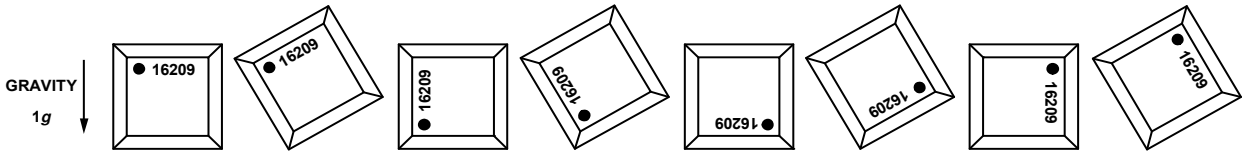



*Figure 18. Horizontal Incline Angle Orientation*




| ROT_OUT | 0° | +30° | +90° | +120° | +180° | –150° | –90° | –60° |
|---|---|---|---|---|---|---|---|---|
| XACCL_OUT | –1*g* | –0.866*g* | 0*g* | 0.5*g* | +1*g* | +0.866*g* | 0*g* | –0.5*g* |
| YACCL_OUT | 0*g* | +0.5*g* | +1*g* | +0.866*g* | 0*g* | –0.5*g* | –1*g* | –0.866*g* |

07096-012

NOTES
1. ROT_OUT = 180° IS 1 LSB DIFFERENT THAN ROT_OUT = –179.975°.

*Figure 19. Vertical Angle Orientation*

# BASIC OPERATION

## INTRODUCTION

When using the factory default configuration for all user configurable control registers, the ADIS16209 initializes itself and automatically starts a continuous process of sampling, processing, and loading calibrated incline angle and acceleration data into the output registers.

## REGISTER STRUCTURE

All communication between the ADIS16209 and an external processor involves either reading the contents of an output register or writing configuration (or command) information to a control register (see Figure 20). The output data registers include the latest sensor data, error flags, and identification information. The control registers include sample rate, filtering, calibration, self-test, input/output line operation, and error flags. Each user accessible register has two bytes (upper and lower), each of which has a unique address. See Table 8 for a detailed list of all user registers, along with the corresponding addresses.

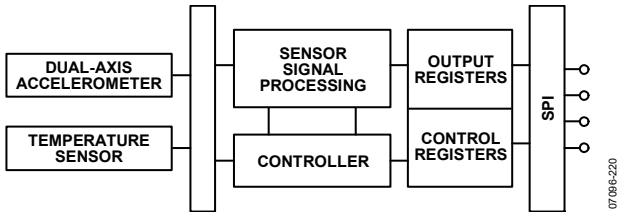



*Figure 20. Basic Operation of the ADIS16209*

## SPI

The SPI provides access to the user registers (see Table 8). Figure 21 shows the most common connections between the ADIS16209 and a SPI master device, which is often an embedded processor that has an SPI-compatible interface.

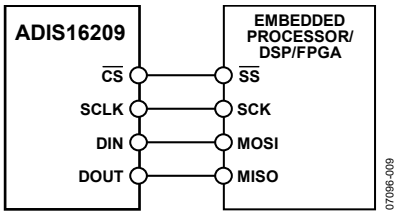



*Figure 21. Electrical Connection Diagram*

**Table 6. Generic SPI Master Pin Mnemonics and Functions**

| Mnemonic | Function |
|---|---|
| $\overline{SS}$ | Slave select |
| SCLK | Serial clock |
| MOSI | Master output, slave input |
| MISO | Master input, slave output |

Embedded processors typically use control registers to configure serial ports for communicating with SPI slave devices, such as the ADIS16209. Table 7 provides a list of common settings that describe the SPI protocol of the ADIS16209. The initialization routine of the master processor typically establishes these settings using firmware commands to write them to the control registers.

**Table 7. Generic Master Processor SPI Settings**

| Processor Setting | Description |
|---|---|
| Master | ADIS16209 operates as slave |
| SCLK ≤ 2.5 MHz | Maximum serial clock rate<br>SMPL_PRD < 0x08 |
| SCLK ≤ 1 MHz[1] | Maximum serial clock rate<br>SMPL_PRD ≥ 0x08 |
| SPI Mode 3 | CPOL = 1 (polarity), CPHA = 1 (phase) |
| MSB First Mode | Bit sequence, see Figure 26 for coding |
| 16-Bit Mode | Shift register and data length |

## READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 26) for a read request on the SPI has three parts: the read bit ($\overline{R}/W = 0$), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. Figure 22 shows an example that includes two register reads in succession. This example starts with DIN = 0x0C00 to request the contents of the XINCL_OUT register and follows with 0x0E00 to request the contents of the YINCL_OUT register. The sequence in Figure 22 also shows full duplex mode of operation, which means that the ADIS16465 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

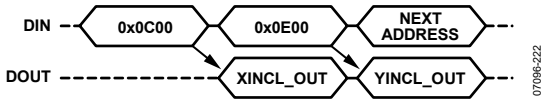



*Figure 22. SPI Read Example*

Figure 23 shows an example of the four SPI signals when reading the PROD_ID register in a repeating pattern. This pattern can be helpful when troubleshooting the SPI interface setup and communications because the signals are the same for each 16-bit sequence, except during the first cycle.

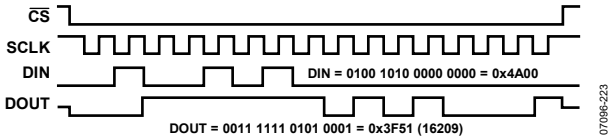



*Figure 23. SPI Signal Pattern, Repeating Read of the PROD_ID Register*

## DEVICE CONFIGURATION

Each configuration register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 8). Updating the contents of a register requires writing to both bytes in the following sequence: low byte first, high byte second. The only exception to this requirement is when writing to the COMMAND register. When using this register to trigger a command, only write to the low byte to trigger the command. Writing to the high byte after triggering a command can interrupt the operation, which the low byte triggers.

There are three parts to coding an SPI command (see Figure 26) that write a new byte of data to a register: the write bit ($\overline{R}/W = 1$), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 24 shows a coding example for writing 0x0001 to the SMPL_PRD register (see Table 24). In Figure 24, the 0xB601 command writes 0x01 to Address 0x36 (lower byte) and the 0xB700 command writes 0x00 to Address 0x37 (upper byte).

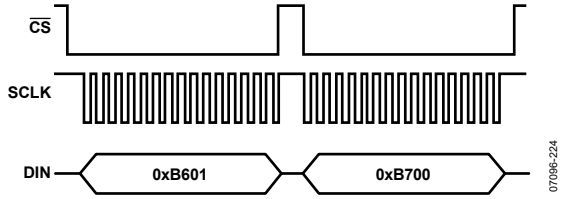



*Figure 24. SPI Sequence for Writing 0x0001 to the SMPL_PRD Register*

### *Memory Structure*

Figure 25 shows a functional diagram for the memory structure of the ADIS16209. The flash memory bank contains the operational code, unit specific calibration coefficients, and user configuration settings. During initialization (power application or reset recover), this information loads from the flash memory into the static random access memory (SRAM), which supports all normal operation, including register access through the SPI port. Writing to a configuration register using the SPI updates the SRAM location of the register but does not automatically update the settings in the flash memory bank. The manual flash memory update command (Register COMMAND, Bit 3, see Table 31) provides a convenient method for saving all of these settings to the flash memory bank at one time. A yes in the Flash Backup column of Table 8 identifies the registers that have storage support in the flash memory bank.

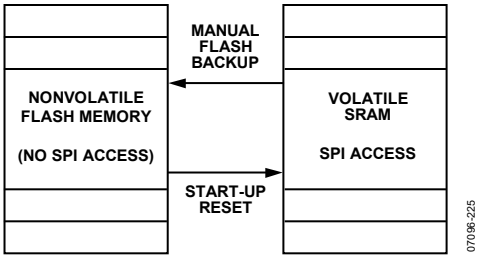



*Figure 25. SRAM and Flash Memory Diagram*

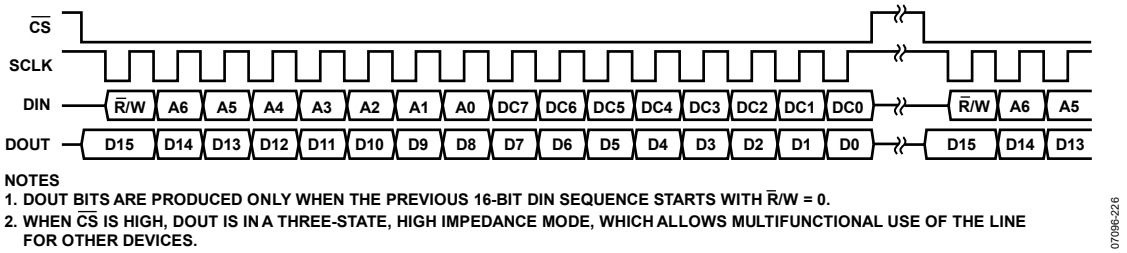



*Figure 26. SPI Communication Bit Sequence*

**Table 8. User Register Map**

| Name | R/W | Flash Backup | Address | Size (Bytes) | Function | Reference |
|---|---|---|---|---|---|---|
| ENDURANCE | R | Yes | 0x00 | 2 | Diagnostics, flash write counter (16-bit binary) | |
| SUPPLY_OUT | R | No | 0x02 | 2 | Output, power supply | Table 20 |
| XACCL_OUT | R | No | 0x04 | 2 | Output, x-axis acceleration | Table 10 |
| YACCL_OUT | R | No | 0x06 | 2 | Output, y-axis acceleration | Table 11 |
| AUX_ADC | R | No | 0x08 | 2 | Output, auxiliary ADC | Table 22 |
| TEMP_OUT | R | No | 0x0A | 2 | Output, temperature | Table 18 |
| XINCL_OUT | R | No | 0x0C | 2 | Output, ±90° x-axis inclination | Table 13 |
| YINCL_OUT | R | No | 0x0E | 2 | Output, ±90° y-axis inclination | Table 14 |
| ROT_OUT | R | No | 0x10 | 2 | Output, ±180° vertical rotational position | Table 16 |
| XACCL_NULL | R/W | Yes | 0x12 | 2 | Calibration, x-axis acceleration offset null | Table 32 |
| YACCL_NULL | R/W | Yes | 0x14 | 2 | Calibration, y-axis acceleration offset null | Table 32 |
| XINCL_NULL | R/W | Yes | 0x16 | 2 | Calibration, x-axis inclination offset null | Table 33 |
| YINCL_NULL | R/W | Yes | 0x18 | 2 | Calibration, y-axis inclination offset null | Table 33 |
| ROT_NULL | R/W | Yes | 0x1A | 2 | Calibration, vertical rotation offset null | Table 33 |
| | | | 0x1C to 0x1F | 4 | Reserved, do not write to these locations | |
| ALM_MAG1 | R/W | Yes | 0x20 | 2 | Alarm 1, amplitude threshold | Table 34 |
| ALM_MAG2 | R/W | Yes | 0x22 | 2 | Alarm 2, amplitude threshold | Table 34 |
| ALM_SMPL1 | R/W | Yes | 0x24 | 2 | Alarm 1, sample period | Table 35 |
| ALM_SMPL2 | R/W | Yes | 0x26 | 2 | Alarm 2, sample period | Table 35 |
| ALM_CTRL | R/W | Yes | 0x28 | 2 | Alarm, source control register | Table 36 |
| | | No | 0x2A to 0x2F | 6 | Reserved | |
| AUX_DAC | R/W | No | 0x30 | 2 | Auxiliary DAC data | Table 30 |
| GPIO_CTRL | R/W | No | 0x32 | 2 | Operation, digital I/O configuration and data | Table 29 |
| MSC_CTRL | R/W | No | 0x34 | 2 | Operation, data-ready and self-test control | Table 28 |
| SMPL_PRD | R/W | Yes | 0x36 | 2 | Operation, sample rate configuration | Table 24 |
| AVG_CNT | R/W | Yes | 0x38 | 2 | Operation, filter configuration | Table 26 |
| SLP_CNT | W | Yes | 0x3A | 2 | Operation, sleep mode control | Table 25 |
| STATUS | R | No | 0x3C | 2 | Diagnostics, system status register | Table 37 |
| COMMAND | W | No | 0x3E | 2 | Operation, system command register | Table 31 |
| | | No | 0x40 to 0x49 | 10 | Reserved | |
| PROD_ID | R | Yes | 0x4A | 2 | Product identification = 0x3F51 | N/A |

## OUTPUT DATA REGISTERS

Table 9 provides the data configuration for each output data register in the ADIS16209. Starting with the MSB of the upper byte, each output data register has the following bit sequence: new data (ND) flag, error/alarm (EA) flag, followed by 14 data bits. The data bits are LSB justified, and in the case of the 12-bit data formats, the remaining two bits are not used. The ND flag indicates that unread data resides in the output data registers. This flag clears and returns to 0 during an output register read sequence. It returns to 1 after the next internal sample update cycle completes. The EA flag indicates an error condition. The STATUS register contains all of the error flags and provides the ability to investigate the root cause.

**Table 9. Output Data Register Formats**

| Register | Bits | Format | Scale[1] |
|---|---|---|---|
| SUPPLY_OUT | 14 | Binary, 3.3 V = 0x2A3D | 0.30518 mV |
| XACCL_OUT | 14 | Twos complement | 0.24414 m*g* |
| YACCL_OUT | 14 | Twos complement | 0.24414 m*g* |
| AUX_ADC | 12 | Binary, 2 V = 0x0CCC | 0.6105 mV |
| TEMP_OUT | 12 | Binary, 25°C = 0x04FE | −0.47°C |
| XINCL_OUT[2] | 14 | Twos complement | 0.025° |
| YINCL_OUT[2] | 14 | Twos complement | 0.025° |
| ROT_OUT[3] | 14 | Twos complement | 0.025° |

[1] Scale denotes quantity per LSB.
[2] Range is −90° to +90°.
[3] Range is −179.975° to +180°.

### *Accelerometers*

The accelerometers respond to both static (gravity) and dynamic acceleration using the polarity shown in Figure 27.

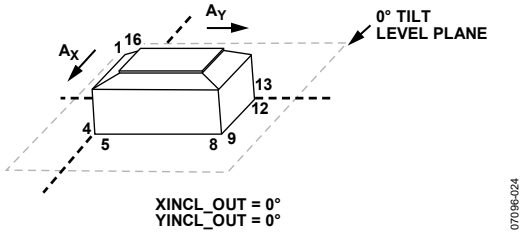



*Figure 27. Accelerometer Polarity*

The XACCL_OUT (see Table 10) and YACCL_OUT (see Table 11) registers provide access to acceleration data for each axis. For example, set DIN = 0x0400 to request data from the x-axis register on the next 16-bit SPI sequence. After reading the contents of one of these registers, mask off the upper two bits, convert the remaining 14-bit, twos complement number into a decimal equivalent, and then multiply that number by 0.024414 to convert the measurement into units of acceleration (m*g*). Table 12 provides several examples of this data format.

**Table 10. XACCL_OUT (Base Address = 0x04), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [13:0] | x-axis accelerometer output data, twos complement, 1 LSB = 0.24414 m*g*, 0 *g* = 0x0000 |

**Table 11. YACCL_OUT (Base Address = 0x06), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [13:0] | y-axis accelerometer output data, twos complement, 1 LSB = 0.24414 m*g*, 0 *g* = 0x0000 |

**Table 12. Accelerometer Data Format Examples**

| Acceleration (*g*) | Decimal | Hex | Binary |
|---|---|---|---|
| +1.7 | +6,963 | 0x1B33 | xx01 1011 0011 0011 |
| +1.0 | +4,096 | 0x1000 | xx01 0000 0000 0000 |
| +0.00048828 | +2 | 0x0002 | xx00 0000 0000 0010 |
| +0.00024414 | +1 | 0x0001 | xx00 0000 0000 0001 |
| 0 | 0 | 0x0000 | xx00 0000 0000 0000 |
| −0.00024414 | −1 | 0x3FFF | xx11 1111 1111 1111 |
| −0.00048828 | −2 | 0xFFFE | xx11 1111 1111 1110 |
| −1.0 | −4096 | 0x3000 | xx11 0000 0000 0000 |
| −1.7 | −27,853 | 0xE4CD | xx10 0100 1100 1101 |

### *Horizontal Incline Angle*

The XINCL_OUT (see Table 13) and YINCL_OUT (see Table 14) registers provide access to acceleration data for each axis. For example, set DIN = 0x0400 to request data from the x-axis register on the next 16-bit SPI sequence. After reading the contents of one of these registers, mask off the upper two bits, convert the remaining 14-bit, twos complement number into a decimal equivalent, and then multiply that number by 0.025 to convert the measurement into units of angle (°). Table 15 provides several examples of this data format.

**Table 13. XINCL_OUT (Base Address = 0x0C), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [13:0] | x-axis inclinometer output data, twos complement, 0° = 0x0000, 1 LSB = 0.025°/LSB, ±90° range |

**Table 14. YINCL_OUT (Base Address = 0x0E), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [13:0] | y-axis inclinometer output data, twos complement, 0° = 0x0000, 1 LSB = 0.025°/LSB, ±90° range |

**Table 15. Horizontal Incline Angle Data Format Examples**

| Orientation | Decimal | Hex | Binary |
|---|---|---|---|
| +90° − 0.025° | +3,599 | 0x0E0F | 0000 1110 0000 1111 |
| +0.05° | +2 | 0x0002 | xx00 0000 0000 0010 |
| +0.025° | +1 | 0x0001 | xx00 0000 0000 0001 |
| 0° | 0 | 0x0000 | xx00 0000 0000 0000 |
| −0.025° | −1 | 0x3FFF | xx11 1111 1111 1111 |
| −0.05° | −2 | 0x3FFE | xx11 1111 1111 1110 |
| −90° | −3,600 | 0x31F1 | xx11 0001 1111 0001 |

### *Vertical Incline Angle*

The ROT_OUT register (see Table 16) provides access to incline angle data for each axis. For example, set DIN = 0x1000 to request data from this register on the next 16-bit SPI sequence. After reading the contents of one of these registers, mask off the upper two bits, convert the remaining 14-bit, twos complement number into a decimal equivalent, and then multiply that number by 0.025 to convert the measurement into units of angle (°). Table 17 provides several examples of this data format.

**Table 16. ROT_OUT (Base Address = 0x10), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [13:0] | Vertical inclinometer output data, twos complement, 0° = 0x0000, 1 LSB = 0.025°/LSB, ±180° range |

**Table 17. Vertical Incline Angle Data Format Examples**

| Orientation | Decimal | Hex | Binary |
|---|---|---|---|
| +180° − 0.025° | +7,199 | 0x1C1F | xx01 1100 0001 1111 |
| +0.05° | +2 | 0x0002 | xx00 0000 0000 0010 |
| +0.025° | +1 | 0x0001 | xx00 0000 0000 0001 |
| 0° | 0 | 0x0000 | xx00 0000 0000 0000 |
| −0.025° | −1 | 0x3FFF | xx11 1111 1111 1111 |
| −0.05° | −2 | 0x3FFE | xx11 1111 1111 1110 |
| −180° | −7,200 | 0x23E0 | xx10 0011 1110 0000 |

### *Internal Temperature*

The TEMP_OUT register (see Table 18) provides access to an internal temperature measurement. Set DIN = 0x0A00 to request the contents of this register. Mask off the upper four bits, then convert the remaining 12-bit binary number into a decimal equivalent, subtract 1278, multiply it by −0.47 and add 25 to convert this number into °C. See Table 19 for examples of this format. Note that this internal temperature measurement provides an indicator of condition changes, not an absolute measurement of conditions outside of the package.

**Table 18. TEMP_OUT (Base Address = 0x0A), Read Only**

| Bits | Description |
|---|---|
| [15:0] | Internal temperature data, binary format, sensitivity = −0.47°/LSB, 25°C = 1278 LSB = 0x04FE |

**Table 19. Internal Temperature Data Format Examples**

| Temperature (°C) | LSB | Hex | Binary |
|---|---|---|---|
| +125 | 1065 | 0x0429 | xxxx 0100 0010 1001 |
| 25 + 0.47 | 1277 | 0x04FD | xxxx 0100 1111 1101 |
| +25 | 1278 | 0x04FE | xxxx 0100 1111 1110 |
| 25 − 0.047 | 1279 | 0x04FF | xxxx 0100 1111 1111 |
| 0 | 1331 | 0x0533 | xxxx 0101 0011 0011 |
| −40 | 1416 | 0x0588 | xxxx 0101 1000 1000 |

### *Power Supply*

The SUPPLY_OUT register (see Table 20) provides a digital measurement for the supply voltage on the VDD pins (see Figure 5). Set DIN = 0x0200 to request the contents of this register. See Table 21 for examples of this data format.

**Table 20. SUPPLY_OUT (Base Address = 0x02), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [15:0] | Power supply measurement data, binary format, 1 LSB = 0.00030518 V, 0 V = 0x0000 |

**Table 21. Power Supply Data Format Examples**

| Supply Level (V) | LSB | Hex | Binary |
|---|---|---|---|
| 3.6 | 11,796 | 0x2E14 | xx10 1110 0001 0100 |
| 3.3 + 0.00030518 | 10,814 | 0x2A3E | xx10 1010 0011 1110 |
| 3.3 | 10,813 | 0x2A3D | xx10 1010 0011 1101 |
| 3.3 − 0.00030518 | 10,812 | 0x2A3C | xx10 1010 0011 1100 |
| 3.0 | 9,830 | 0x2666 | xx10 0110 0110 0110 |

### Auxiliary ADC

The AUX_ADC register (see Table 22) provides a digital measurement for the AUX_ADC input pin (see Figure 5). Set DIN = 0x0800 to request the contents of this register. See Table 23 for examples of this data format.

**Table 22. AUX_ADC (Base Address = 0x08), Read Only**

| Bits | Description |
|---|---|
| 15 | New data bit = 1, when register contains un-read data |
| 14 | Error/alarm = 1, when STATUS ≠ 0x0000 |
| [13:12] | Not used |
| [15:0] | Auxiliary ADC data, binary format,<br>1 LSB = 0.0006105 V, 0 V = 0x0000 |

**Table 23. Auxiliary ADC Data Format Examples**

| Supply Level (V) | LSB | Hex | Binary |
|---|---|---|---|
| 2.5 | 4095 | 0xFFF | xxxx 1111 1111 1111 |
| 0.001221 | 2 | 0x002 | xxxx 0000 0000 0010 |
| 0.0006105 | 1 | 0x001 | xxxx 0000 0000 0001 |
| 0 | 0 | 0x000 | xxxx 0000 0000 0000 |

## OPERATION CONTROL REGISTERS

### Internal Sample Rate

The SMPL_PRD register controls the ADIS16209 internal sample rate and has two parts: a selectable time base and a multiplier. The following relationship produces the sample rate:

$$t_S = t_B \times N_S + 122.07\ \mu s$$

**Table 24. SMPL_PRD Bit Descriptions**

| Bit | Description (Default = 0x0014) |
|---|---|
| 15:8 | Not used |
| 7 | Time base ($t_B$): 0 = 244.14 µs, 1 = 7.568 ms |
| 6:0 | Increment setting ($N_S$) |

An example calculation of the default sample period follows:

$SMPL\_PRD$ = 0x01, $B7 - B0$ = 00000001

$B7 = 0 \rightarrow t_B = 244.14\ \mu s$, $B6 \ldots B0 = 000000001 \rightarrow N_S = 1$

$t_S = t_B \times N_S + 122.07\ \mu s = 244.14 \times 1 + 122.07 = 366.21\ \mu s$

$f_S = 1/t_S = 2731$ SPS

The sample rate setting has a direct impact on the SPI data rate capability. For sample rates ≥546 SPS, the SPI SCLK can run at a rate up to 2.5 MHz. For sample rates <546 SPS, the SPI SCLK can run at a rate up to 1 MHz. The sample rate setting also affects power dissipation. When the sample rate is set to <546 SPS, power dissipation typically reduces by a factor of 68%. The two different modes of operation offer a system-level trade-off between performance (sample rate, serial transfer rate) and power dissipation.

### Power Management

In addition to offering two different performance modes for power optimization, the ADIS16209 offers a programmable shutdown period that the SLP_CNT register controls.

**Table 25. SLP_CNT Bit Descriptions**

| Bit | Description (Default = 0x0000) |
|---|---|
| 15:8 | Not used |
| 7:0 | Data bits, 0.5 seconds/LSB |

For example, writing 0x08 to the SLP_CNT register places the ADIS16209 into sleep mode for 4 sec. The only way to stop this process is to remove power or reset the device.

### Digital Filtering

The AVG_CNT register controls the moving average digital filter, which determines the size of the moving average filter in eight power-of-two step sizes (that is, $2^M$ = 1, 2, 4, 16, 32, 64, 128, and 256). Filter setup requires one simple step: write the appropriate M factor to the assigned bits in the AVG_CNT register. Note that the default settings for AVG_CNT and SMPL_PRD provide the best accuracy but require approximately 1.28 seconds to settle.

**Table 26. AVG_CNT Bit Descriptions**

| Bit | Description (Default = 0x0008) |
|---|---|
| 15:4 | Not used |
| 3:0 | Power-of-two step size, maximum binary value = 1000 |

The following equation offers a frequency response relationship for this filter:

$$H_A(f) = \frac{\sin(\pi \times N \times f \times t_S)}{N \times \sin(\pi \times f \times t_S)}$$

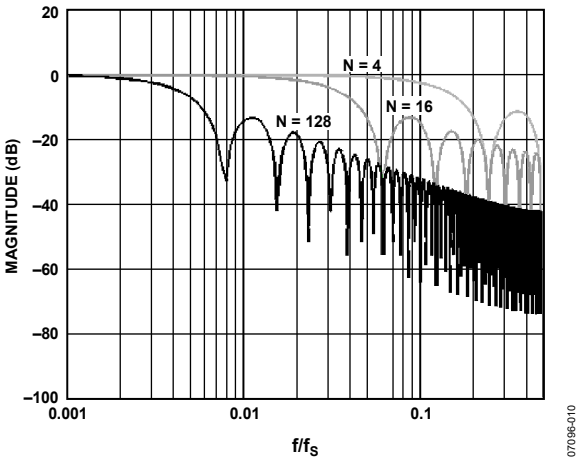



*Figure 28. Frequency Response—Moving Average Filter*

### Digital I/O Lines

The ADIS16209 provides two general-purpose, digital input/output lines that have several configuration options.

**Table 27. Digital I/O Line Configuration Registers**

| Function | Priority | Register |
|---|---|---|
| Data-Ready I/O Indicator | 1 | MSC_CTRL |
| Alarm Indicator | 2 | ALM_CTRL |
| General-Purpose I/O Configuration | 3 | GPIO_CTRL |
| General-Purpose I/O Line Communication | | GPIO_CTRL |

### Data-Ready I/O Indicator

The MSC_CTRL register provides controls for a data-ready function. For example, writing 0x05 to this register enables this function and establishes DIO2 as an active-low, data-ready line. The duty cycle is 25% (±10% tolerance).

**Table 28. MSC_CTRL Bit Descriptions**

| Bit | Description (Default = 0x0000) |
|---|---|
| 15:11 | Not used |
| 10 | Self-test at power-on: 1 = disabled, 0 = enabled |
| 9 | Not used |
| 8 | Self-test enable: 1 = enabled, 0 = disabled |
| 7:3 | Not used |
| 2 | Data-ready enable: 1 = enabled, 0 = disabled |
| 1 | Data-ready polarity: 1 = active high, 0 = active low |
| 0 | Data-ready line select: 1 = DIO2, 0 = DIO1 |

### Self-Test

The self-test function applies an electrostatic force to the MEMS structure, inside of the core sensor, which causes the structure to move in a manner that simulates its response to gravity or linear acceleration. This provides an observable response in the accelerometer outputs that can serve as a validation of functional operation throughout the entire signal chain. The MSC_CTRL register (Table 28) provides two different options for using this function: manual (user-command) and automatic (during start-up/reset recovery).

The manual self-test control is an on/off control for the electrostatic force. Set MSC_CTRL[8] = 1 to turn it on and set MSC_CTRL[8] = 0 to turn it off. For normal operation, this will be in the off state but this control bit provides an opportunity to activate it at any time, so that system processors can apply application-relevant pass/fail criteria to the responses. When MSC_CTRL[10] = 1, the automatic self-test process runs during the power-on process. This runs the ADIS16209 through on/off states for the self-test, while observing the difference in accelerometer response. This process concludes with a comparison of the differential response in each accelerometer, with internal pass/fail limits and a report of the result to STATUS[5]. Once the ADIS16209 completes is its start-up process, STATUS is available for a SPI-driven read, using DIN = 0x3C00 as the SPI input command (STATUS at Address 0x3C).

Linear motion during the start-up process, VDD ramp rates/waveform and the tilt of the device can introduce uncertainty into the on/off levels and in some cases, cause a false failure report to STATUS[5] (result = 0x0020). While the selection of the pass/fail limits incorporates most conditions, false failures are still possible.

When presented with a self-test failure indication, where STATUS ≥ 0x0020, use the following process to test for basic function. This process assumes a stable power supply voltage and zero motion.

1. Set AVG_CNT = 0x0000 and SMPL_PRD = 0x0008, to optimize the response times during the self-test transitions, while keeping the ADIS16209 in low power mode. In this configuration, the self-test response will be similar to a step response of a single-pole, low-pass filter that has a cutoff frequency of 50 Hz.
2. Read XACCL_OUT and YACCL_OUT.
3. Set MSC_CTRL[8] = 1.
4. Delay > 20 ms, which provides the 50 Hz filter (internal to ADIS16209) with at least six time constants to settle.
5. Read XACCL_OUT and YACCL_OUT.
6. Calculate difference in measurements:
   - D-XACCL_OUT = XACCL_OUT (Step 6) – XACCL_OUT (Step 3)
   - D-YACCL_OUT = YACCL_OUT (Step 6) – YACCL_OUT (Step 3)
7. Set MSC_CTRL[8] = 0.
8. Restore the SMPL_PRD and AVG_CNT registers to their operational values.
9. Determine normal operation by making sure that the D-XACCL_OUT and D-YACCL_OUT produced a change of at least 350 LSB.

The 350 LSB pass/fail limit is approximately one-half of the data sheet specification for the minimum response time and is well above the noise floor. Because the purpose of this function is to identify gross functional issues, such as a zero response, this is a safe approach, given a stable platform and supply. When experiencing modest motion, some of the parameters may need further consideration to account for application-specific conditions.

### General-Purpose I/O

The GPIO_CTRL register controls the direction and data of the general-purpose digital lines, DIO1 and DIO2. For example, writing a 0x02 to the GPIO_CTRL register sets DIO2 as an output line and DIO1 as an input line. Reading the data bits in GPIO_CTRL reveals the line logic level.

**Table 29. GPIO_CTRL Bit Descriptions**

| Bit | Description (Default = 0x0000) |
|---|---|
| 15:10 | Not used |
| 9 | General-Purpose I/O Line 2 data |
| 8 | General-Purpose I/O Line 1 data |
| 7:2 | Not used |
| 1 | General-Purpose I/O Line 2, data direction control:<br>1 = output, 0 = input |
| 0 | General-Purpose I/O Line 1, data direction control:<br>1 = output, 0 = input |

### *Auxiliary DAC*

The auxiliary DAC provides a 12-bit level adjustment function. The AUX_DAC register controls the operation of the auxiliary DAC function, which is useful for systems that require analog level controls. It offers a rail-to-rail buffered output that has a range of 0 V to 2.5 V. The DAC can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches ground, the linearity begins to degrade (100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC output latch function, contained in the COMMAND register, provides continuous operation while writing to each byte of this register. The contents of this register are volatile, which means that the desired output level must be set after every reset and power cycle event.

**Table 30. AUX_DAC Bit Descriptions**

| Bit | Description (Default = 0x0000) |
|---|---|
| 15:12 | Not used |
| 11:0 | Data bits, scale factor = 0.6105 mV/code<br>Offset binary format, 0 V = 0 codes |

### *Global Commands*

The COMMAND register provides initiation bits for several commands that simplify many common operations. Writing a 1 to the assigned COMMAND bit exercises its function. When triggering one of the operations in the COMMAND register, only write to the low byte of this register, then wait until the operation completes before attempting new communications requests on the SPI.

**Table 31. COMMAND Bit Descriptions**

| Bit | Description (Default = 0x0000) |
|---|---|
| 15:8 | Not used |
| 7 | Software reset |
| 6:5 | Not used |
| 4 | Clear status register (reset all bits to 0) |
| 3 | Flash update; backs up all registers, see Table 8 |
| 2 | DAC data latch |
| 1 | Factory calibration restore |
| 0 | Autonull |

The software reset command restarts the internal processor, which loads all registers with the contents in their flash memory locations.

The flash update copies the contents of all the flash backup registers into their assigned, nonvolatile flash memory locations. This process takes approximately 50 ms and requires a power supply that is within the specified operating range. After waiting the appropriate time for the flash update to complete, verify successful completion by reading the STATUS register (if successful, the flash update error is 0). If the flash update was not successful, reading this error bit accomplishes two things: it alerts the system processor to try again, and it clears the error flag, which is required for flash memory access.

The DAC data latch command loads the contents of AUX_DAC into the DAC latches. Because the AUX_DAC contents must be updated one byte at a time, this command ensures a stable DAC output voltage during updates.

The autonull command provides a simple method for removing offset from the sensor outputs by taking the contents of the output data registers and loading the equal but opposite number into the offset calibration registers.

To accomplish this, the autonull command executes the following operations:

1. Read the XACCL_OUT, YACCL_OUT, XINCL_OUT, YINCL_OUT, and ROT_OUT values.
2. Change the polarity of these measurements.
3. Write the results to the XACCL_NULL, YACCL_NULL, XINCL_NULL, YINCL_NULL, and ROT_NULL registers.
4. Perform a manual backup of all user registers, using the flash memory bank.

When using the horizontal incline angle measurements (XINCL_OUT and YINCL_OUT), the autonull helps remove bias errors in the accelerometers, as well as orientation error, with respect to the horizontal plane (0 *g*). When using the vertical incline measurement (ROT_OUT), do not use the autonull function.

The accuracy of this operation depends on stable inertial conditions (zero acceleration or change in orientation, with respect to gravity) and optimal noise management during the measurement (see the Digital Filtering section).

The factory calibration restore command sets the offset null registers (XACCL_NULL, for example) back to their default values.

## CALIBRATION REGISTERS

The ADIS16209 incorporates an extensive factory calibration and provides precision acceleration, incline, and rotational position data. For systems that require on-site calibration, user-programmable offset adjustment registers are available.

Table 32 provides the bit assignments for the following user-programmable calibration registers: XACCL_NULL and YACCL_NULL. Table 33 provides the bit assignments for the following user-programmable calibration registers: XINCL_NULL, YINCL_NULL, and ROT_NULL.

**Table 32. Acceleration Offset Register Bit Designations**

| Bit | Description | (Default = 0x0000) |
|---|---|---|
| 15:14 | Not used | |
| 13:0 | Data bits, twos complement, sensitivity = 0.24414 m*g*/LSB | |

**Table 33. Incline/Rotation Offset Register Bit Designations**

| Bit | Description | (Default = 0x0000) |
|---|---|---|
| 15:14 | Not used | |
| 13:0 | Data bits, twos complement, sensitivity = 0.025°/LSB | |

## ALARM REGISTERS

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source, data filtering (prior to comparison), static/dynamic, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations. The ALM_SMPLx registers provide the numbers of samples to use in the dynamic rate-of-change configuration. The rate-of-change calculation is

$$Y_C = \frac{1}{N_{DS}} \sum_{n=1}^{N_{DS}} y(n+1) - y(n) \Rightarrow Alarm \Rightarrow \text{is } Y_C > \text{or} < M_C \text{ ?}$$

where:
$N_{DS}$ is the number of samples in ALM_SMPLx.
$y(n)$ is the sampled output data.
$M_C$ is the magnitude for comparison in ALM_MAGx.
> or < is determined by the MSB in ALM_MAGx.

**Table 34. ALM_MAG1/ALM_MAG2 Bit Designations**

| Bit | Description | (Default = 0x0000) |
|---|---|---|
| 15 | Comparison polarity: 1 = greater than, 0 = less than | |
| 14 | Not used | |
| 13:0 | Data bits, matches format of trigger source selection | |

**Table 35. ALM_SMPL1/ALM_SMPL2 Bit Designations**

| Bit | Description | (Default = 0x0001) |
|---|---|---|
| 15:8 | Not used | |
| 7:0 | Data bits: number of samples (both 0x00 and 0x01 = 1) | |

**Table 36. ALM_CTRL Bit Descriptions**

| Bit | Value | Description | (Default = 0x0000) |
|---|---|---|---|
| 15:12 | | Trigger source, Alarm 2 | |
| | 0000 | Disabled | |
| | 0001 | Power supply | |
| | 0010 | X-acceleration | |
| | 0011 | Y-acceleration | |
| | 0100 | Auxiliary ADC | |
| | 0101 | Temperature sensor | |
| | 0110 | X-axis incline angle | |
| | 0111 | Y-axis incline angle | |
| | 1000 | Rotational position | |
| 11:8 | | Trigger source, Alarm 1, same as Bits[15:12] | |
| 7 | | Not used | |
| 6 | | Alarm 2 rate-of-change control: 1 = enabled | |
| 5 | | Alarm 1 rate-of-change control: 1 = enabled | |
| 4 | | Alarm 2 filter: 1 = filtered data, 0 = no filter[1] | |
| 3 | | Alarm 1 filter: 1 = filtered data, 0 = no filter[1] | |
| 2 | | Alarm indicator, using DIO1/DIO2: 1 = enabled | |
| 1 | | Alarm indicator polarity: 1 = active high | |
| 0 | | Alarm indicator line select: 1 = DIO2, 0 = DIO1 | |

[1] Incline and vertical angles always use filtered data in this comparison.

### *Status*

The STATUS register provides a series of error flags that provide indicator functions for common system-level issues. After reading the contents of this register, set COMMAND[4] = 1 (DIN = 0xBE10) to reset all of its flags to zero.

**Table 37. STATUS Bit Descriptions**

| Bit | Description | (Default = 0x0000) |
|---|---|---|
| 15:10 | Not used | |
| 9 | Alarm 2 status:<br>1 = active, 0 = inactive | |
| 8 | Alarm 1 status:<br>1 = active, 0 = inactive | |
| 7:6 | Not used | |
| 5 | Self-test diagnostic error flag:<br>1 = error condition, 0 = normal operation | |
| 4 | Not used | |
| 3 | SPI communications failure:<br>1 = error condition, 0 = normal operation | |
| 2 | Flash update failed:<br>1 = error condition, 0 = normal operation | |
| 1 | Power supply greater than 3.625 V:<br>1 > 3.625 V, 0 ≤ 3.625 V (normal) | |
| 0 | Power supply less than 2.975 V:<br>1 < 2.975 V, 0 ≥ 2.975 V (normal) | |

# APPLICATIONS INFORMATION

## POWER SUPPLY CONSIDERATIONS

The ADIS16209 is a precision sensing system that uses an embedded processor for critical interface and signal processing functions. Supporting this processor requires a low impedance power supply, which can manage transient current demands that happen during normal operation, as well as during the start-up process. Transient current demands start when the voltage on the VDD pin reaches ~2.1 V. Therefore, it is important for the voltage on the VDD pin to reach 3 V as quickly as possible. Linear VDD ramp profiles that reach 3 V in 100 µs provide reliable results when used in conjunction with design practices that support low dynamic source impedance. The ADP1712 is a linear regulator that can support the recommended ramp profile. See the ADIS1620x/21x/22x Power Regulator Suggestion page for a reference design for using this regulator with the ADIS16209.

### *Power-On-Reset Function*

The ADIS16209 has a power-on-reset (POR) function that triggers a reset if the voltage on the VDD pin fails to transition between 2.35 V and 2.7 V within 128 ms.

### *Transient Current from VDD Ramp Rate*

Because the ADIS16209 contains 2 µF of decoupling capacitance on VDD and some systems may use additional filtering capacitance, the VDD ramp rate will have a direct impact on initial transient current requirements. Use this formula to estimate the transient current, associated with a particular capacitance (C) and VDD ramp rate (dV/dt).

$$i(t) = C\,{}^{dV}\!/_{dt}$$

For example, if VDD transitions from 0 V to +3.3 V in 33 µs, dV/dt is equal to 100000V/S (3.3 V/33 µs). When charging the internal 2 µF capacitor (no external capacitance), the charging current for this ramps rate is 200 mA, during the 33 µs ramp time. This relationship provides a tool for evaluating the initial charging currents against the current limit thresholds of system power supplies, which can cause power supply interruptions and the appearance of failed start-ups. This may also be important for maintaining surge current ratings of any series elements as well

### *Filter Settling*

The SMPL_PRD and AVG_CNT settings have a direct impact on the filter settling during turn-on. For example, when using the default settings for these filters, the SUPPLY_OUT register takes approximately 1.28 seconds to settle. During this time, the SUPPLY_OUT register experiences a linear rise (assuming that VDD is stable and greater than 3.0 V) and the low-voltage flag (STATUS[0]) is low. When the SUPPLY_OUT register reaches a value that exceeds 2.975 V, the STATUS[0] flag automatically lowers.

## ASSEMBLY

When developing a process flow for installing ADIS16209 devices on PCBs, see the JEDEC standard document J-STD-020C for reflow temperature profile and processing information. The ADIS16209 can use the Sn-Pb eutectic process and the Pb-free eutectic process from this standard, with one exception: the peak temperature exposure is 240°C. For a more complete list of assembly process suggestion, see the ADIS162xx LGA Assembly Guidelines page at the Engineer Zone/MEMS Community website. Figure 29 provides an example pad layout for the location of the ADIS16209 on a printed circuit board (PCB).

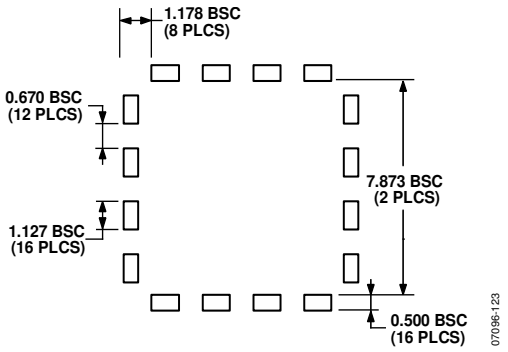



*Figure 29. Example Pad Layout*

## INTERFACE BOARD

The ADIS16209/PCBZ provides the ADIS16209 function on a 1.2 inch × 1.3 inch PCB, which simplifies the connection to an existing processor system. The four mounting holes accommodate either M2 (2 mm) or Type 2-56 machine screws. These boards are made of IS410 material and are 0.063 inches thick. The second level assembly uses a SAC305-compatible solder composition (Pb-free), which has a presolder reflow thickness of approximately 0.005 inches. The pad pattern on the ADIS16209/PCBZ matches that shown in Figure 31. J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon-crimp connector) and 3M Part Number 3625/12 (ribbon cable).

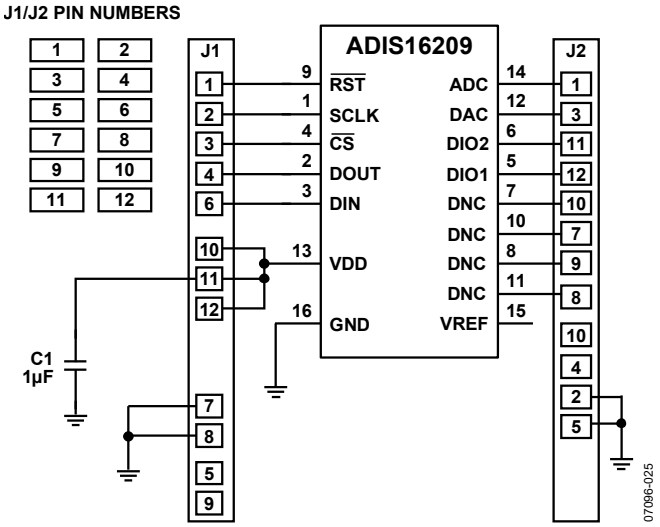



*Figure 30. Electrical Schematic*

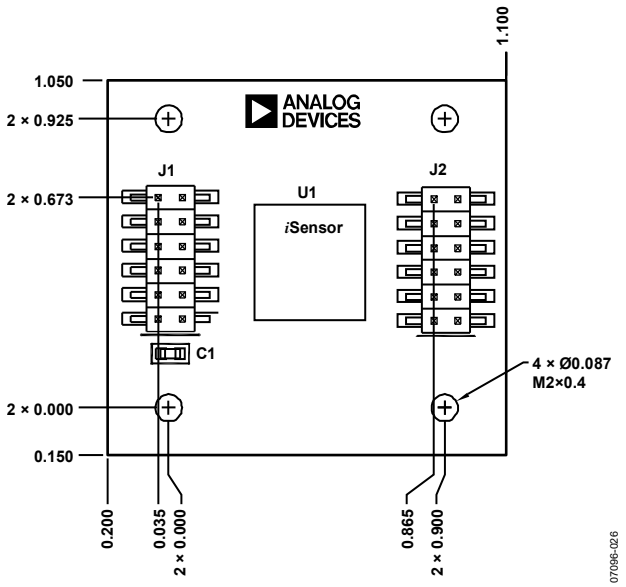



*Figure 31. PCB Assembly View and Dimensions*

## X-RAY SENSITIVITY

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, may affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16209 to this type of inspection.

# OUTLINE DIMENSIONS

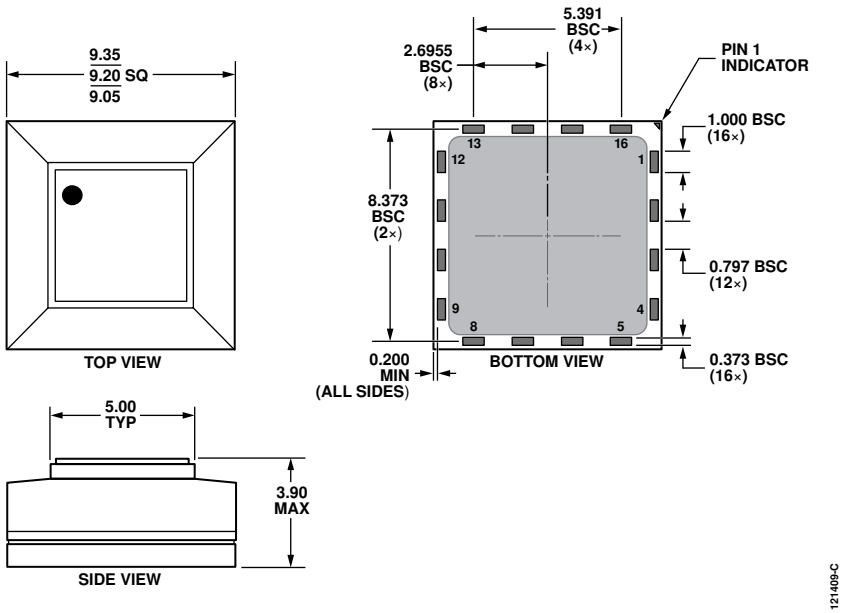



*Figure 32. 16-Terminal Stacked Land Grid Array [LGA]*
*(CC-16-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADIS16209CCCZ | −40°C to +125°C | 16-Terminal Stacked Land Grid Array [LGA] | CC-16-2 |
| ADIS16209/PCBZ | | Evaluation Board | |
| EVAL-ADIS2Z | | Evaluation System | |

[1] Z = RoHS Compliant Part.