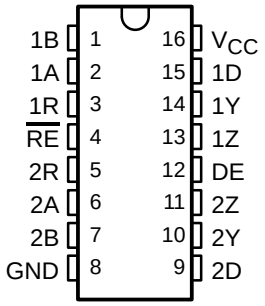
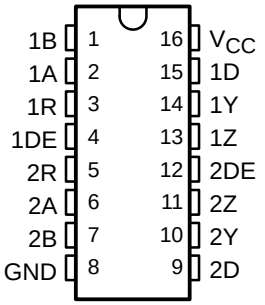
SLLS154B – MARCH 1993 – REVISED FEBRUARY 2001

- **Meet or Exceed Standards TIA/EIA-422-B and TIA/EIA-485-A**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply-Current Requirement 50 mA Max**
- **Driver Positive- and Negative-Current Limiting**
- **Driver Common-Mode Output Voltage Range of –7 V to 12 V**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of –12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver High Input Impedance . . . 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN75ALS1177 Only**
- **Operate From Single 5-V Supply**

SN75ALS1177 . . . N OR NS PACKAGE
(TOP VIEW)



SN75ALS1178 . . . N OR NS PACKAGE
(TOP VIEW)



description

The SN75ALS1177 and SN75ALS1178 dual differential drivers and receivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet standards TIA/EIA-422-B and TIA/EIA-485-A.

The SN75ALS1177 combines dual 3-state differential line drivers and dual 3-state differential input line receivers, both of which operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN75ALS1178 drivers each have an individual active-high enable. Fail-safe design ensures that when the receiver inputs are open, the receiver outputs are always high.

The SN75ALS1177 and SN75ALS1178 are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC DIP (N)	PLASTIC SMALL OUTLINE (NS)
0°C to 70°C	SN75ALS1177N	SN75ALS1177NSR
	SN75ALS1178N	SN75ALS1178NSR

The NS package is only available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS1177NSR).

Function Tables

SN75ALS1177, SN75ALS1178
(each driver)

INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN75ALS1177
(each receiver)

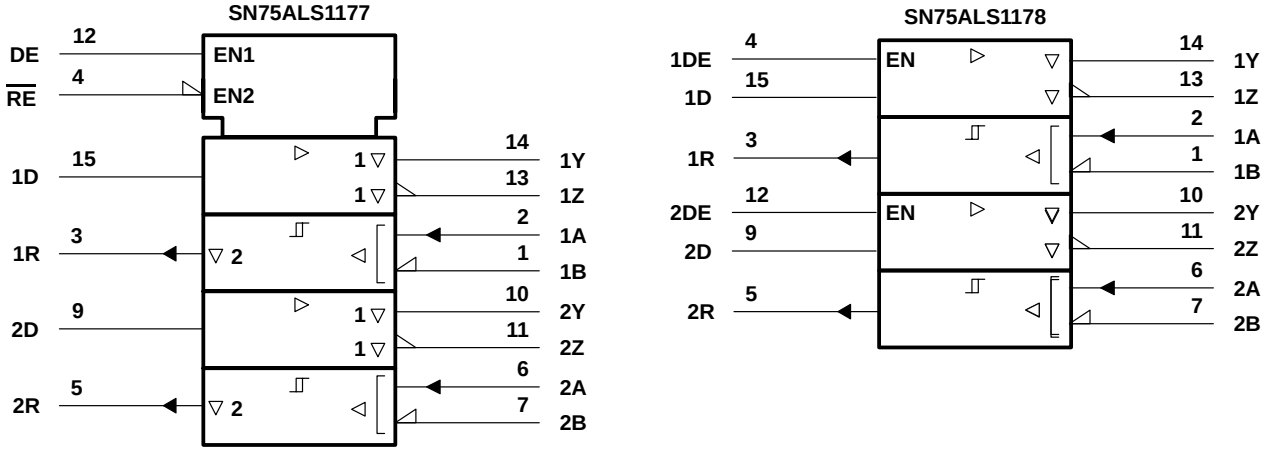
DIFFERENTIAL A–B	ENABLE $\overline{RE}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

SN75ALS1178
(each receiver)

DIFFERENTIAL A–B	OUTPUT Y
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open	H

H = High level, L = Low level,
? = Indeterminate, X = Irrelevant,
Z = High impedance (off)

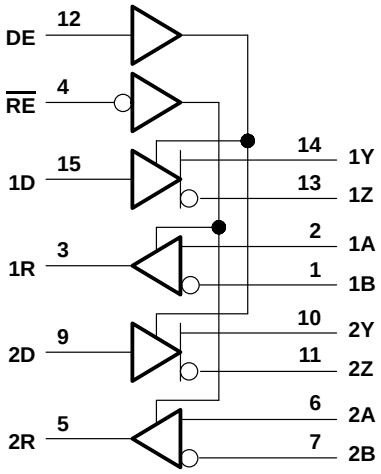
logic symbol†



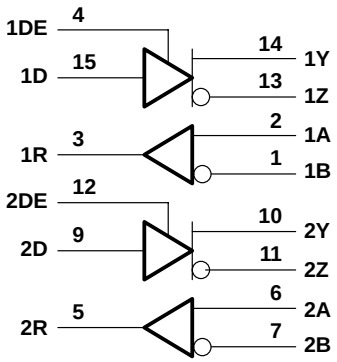
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

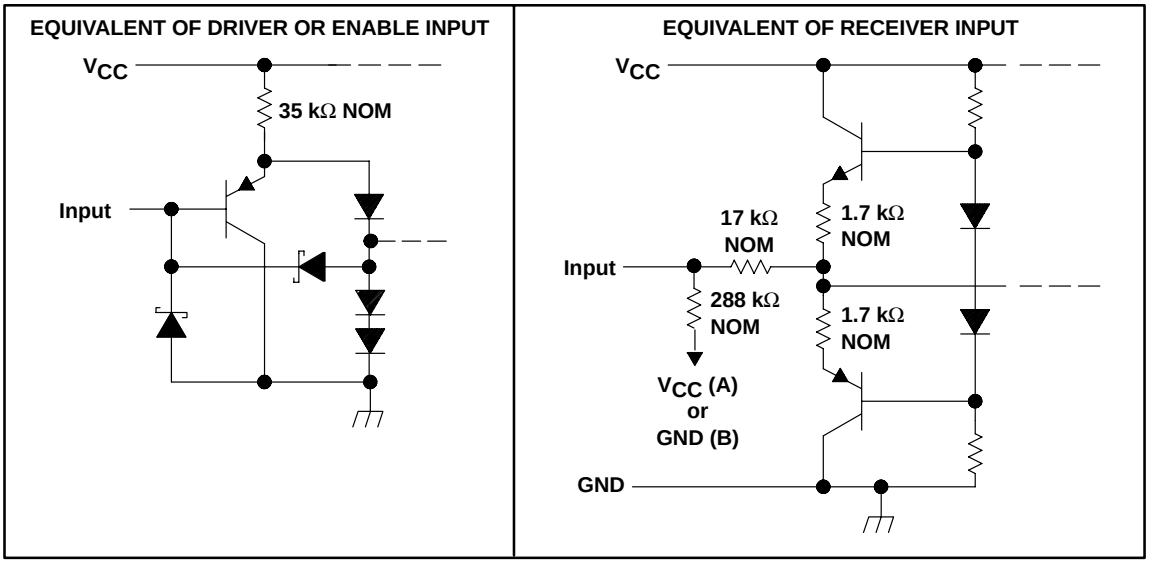
SN75ALS1177



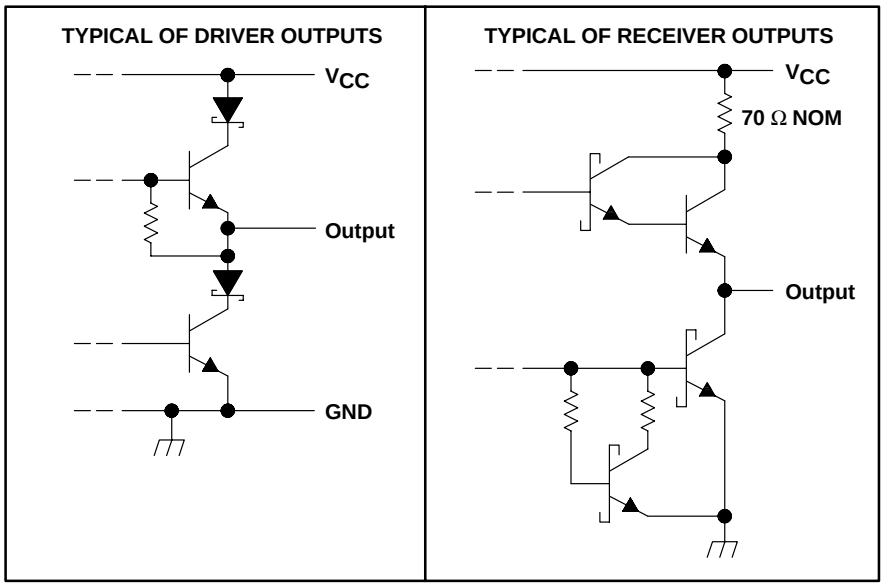
SN75ALS1178



equivalent schematics



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I (DE, $\overline{RE}$, and D inputs) . . . . . 7 V
Output voltage range, V_O (driver) . . . . . –9 V to 14 V
Input voltage range, receiver . . . . . –14 V to 14 V
Receiver differential-input voltage range (see Note 2) . . . . . –14 V to 14 V
Receiver low-level output current . . . . . 50 mA
Package thermal impedance, θ_{JA} (see Note 3): N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{ID}	Differential input voltage	Receiver			±12	V
V_{OC}	Common-mode output voltage	Driver	–7†		12	V
V_{IC}	Common-mode input voltage	Receiver			±12	V
V_{IH}	High-level input voltage	DE, $\overline{RE}$, D	2			V
V_{IL}	Low-level input voltage	DE, $\overline{RE}$, D			0.8	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	μA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = –33 mA		3.3		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 33 mA		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0			1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = 5 V,	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω,	See Figure 1		1.5	2.5	5	
$\lvert V_{OD3}\rvert$	Differential output voltage	See Note 4			1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage (see Note 5)	R_L = 54 Ω or 100 Ω,		See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,		See Figure 1	–1§		3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage (see Note 5)	R_L = 54 Ω or 100 Ω,		See Figure 1			±0.2	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V					±100	µA
I_{IH}	High-level input current	V_{IH} = 2.7 V					100	µA
I_{IL}	Low-level input current	V_{IL} = 0.4 V					–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V					–250	mA
		V_O = V_{CC}					250	
		V_O = 12 V					250	
		V_O = 0 V					150	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	50	mA
			Outputs disabled			20	50	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See TIA/EIA-485-A Figure 3.5, test termination measurement 2.
5. $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high- to low-level output	R_L = 60 Ω, C_{L1} = C_{L2} = 100 pF, See Figure 3		9	15	22	ns
t_{PHL}	Propagation delay time, low- to high-level output	R_L = 60 Ω, C_{L1} = C_{L2} = 100 pF, See Figure 3		9	15	22	ns
t_{sk}	Output-to-output skew	R_L = 60 Ω, C_{L1} = C_{L2} = 100 pF, See Figure 3		0	2	8	ns
t_{PZH}	Output enable time to high level	C_L = 100 pF,	See Figure 4	30	35	50	ns
t_{PZL}	Output enable time to low level	C_L = 100 pF,	See Figure 5	5	15	25	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 4	7	15	30	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See Figure 5	7	15	30	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage		V_O = 0.5 V,	I_O = 8 mA	–0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)					50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –400 μA, See Figure 2		2.7			V
V_{OL}	Low-level output voltage		V_{ID} = 200 mV, I_{OL} = 8 mA, See Figure 2				0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 6)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = –7 V			–0.8	
I_{IH}	High-level input current, $\overline{RE}$	SN75ALS1177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	SN75ALS1177	V_{IL} = 0.4 V				–100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		V_O = 0 V,	See Note 7	–15		–85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled		35	50	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 6. Refer to TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.
7. Not more than one output should be shorted at a time.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		C_L = 15 pF,	See Figure 6	15	25	37	ns
t_{PHL}	Propagation delay time, high- to low-level output		C_L = 15 pF,	See Figure 6	15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177	C_L = 15 pF,	See Figure 7	3.5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns

PARAMETER MEASUREMENT INFORMATION

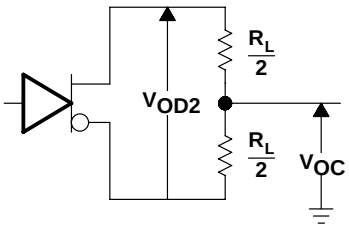


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

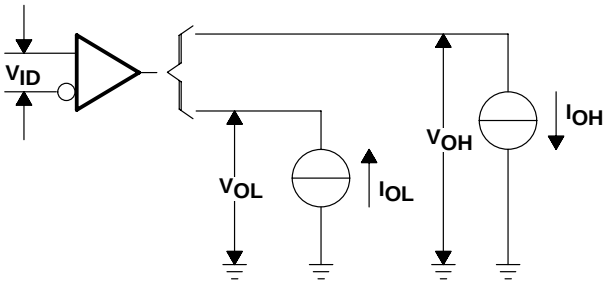
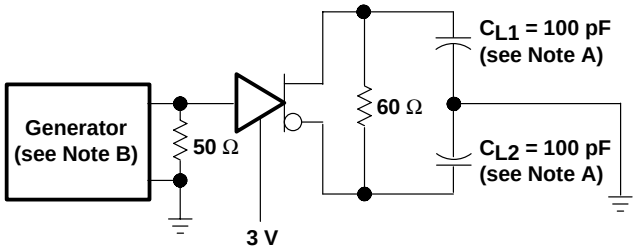
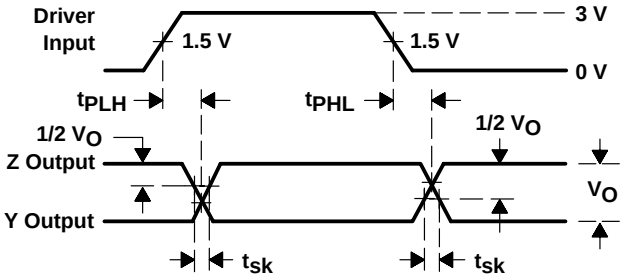


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



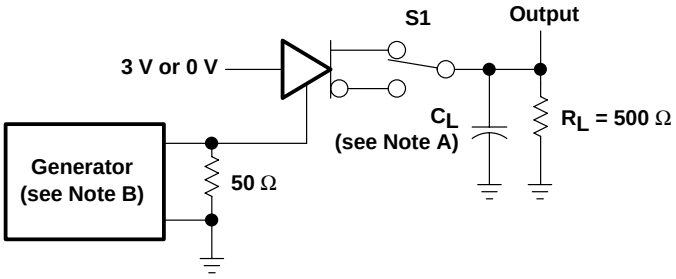
DRIVER TEST CIRCUIT



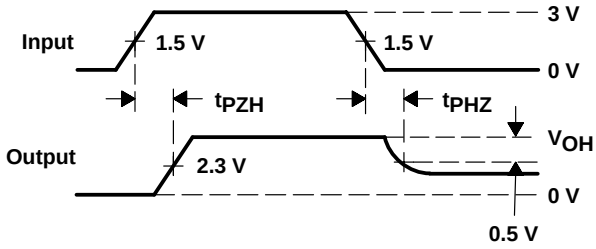
DRIVER VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 3. Driver Propagation Delay Times



DRIVER TEST CIRCUIT

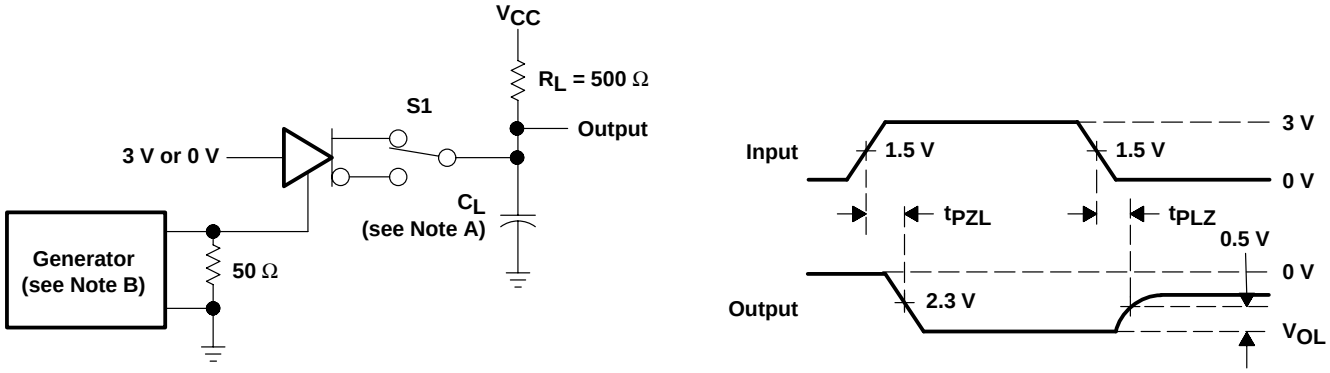


DRIVER VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 4. Driver Enable and Disable Times

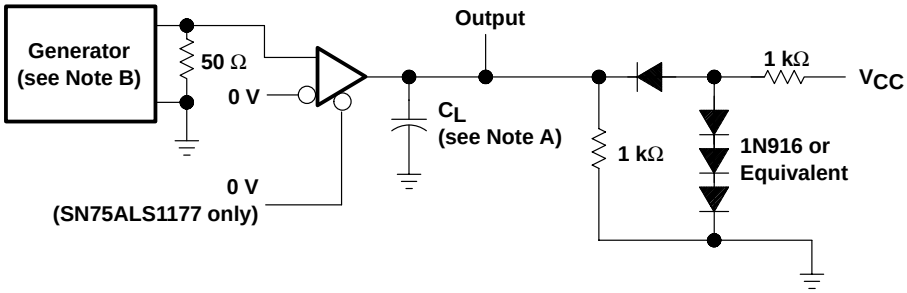
PARAMETER MEASUREMENT INFORMATION



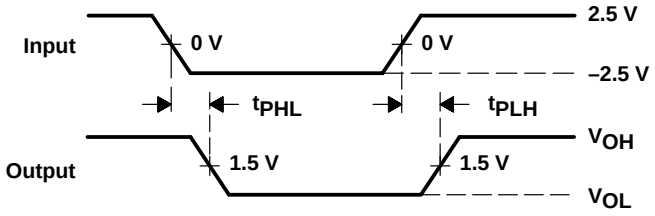
DRIVER TEST CIRCUIT **DRIVER VOLTAGE WAVEFORMS**

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 5. Driver Enable and Disable Times



RECEIVER TEST CIRCUIT

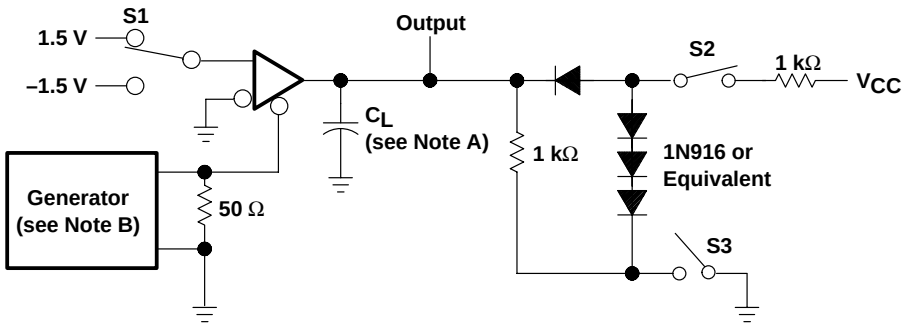


DRIVER VOLTAGE WAVEFORMS

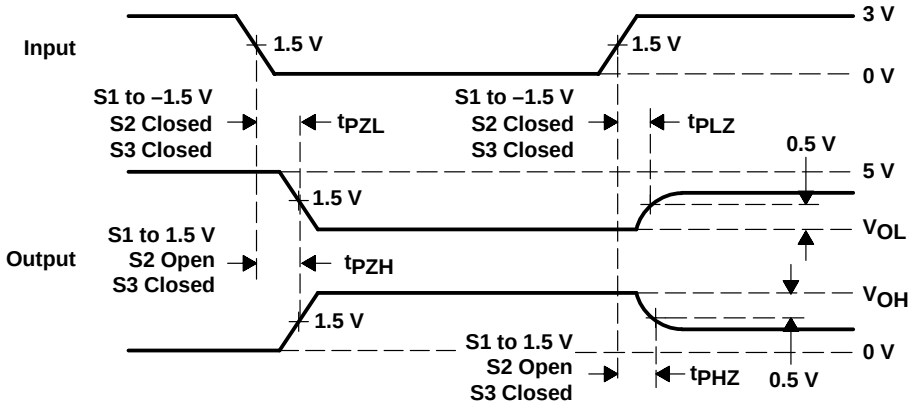
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 6. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



RECEIVER TEST CIRCUIT



RECEIVER VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 7. Receiver Output Enable and Disable Times

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS1177N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS1177N	Samples
SN75ALS1177NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1177	Samples
SN75ALS1178N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS1178N	Samples
SN75ALS1178NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1178	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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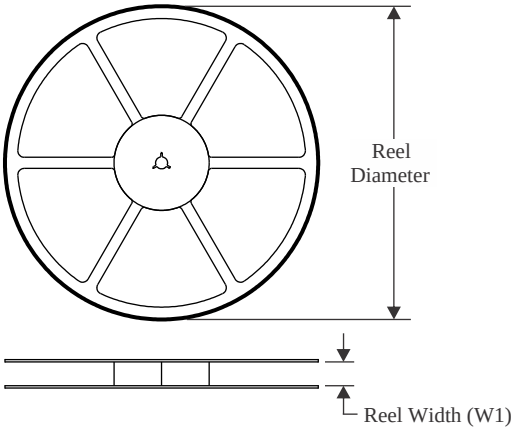
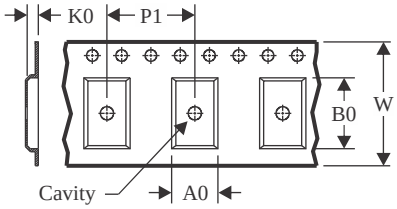
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

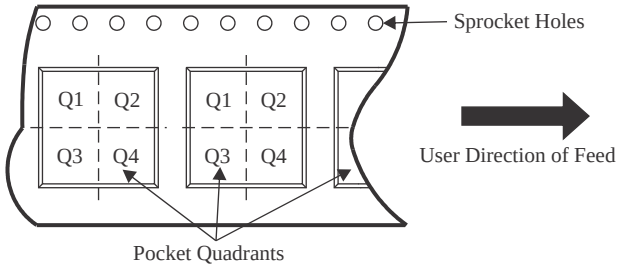


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

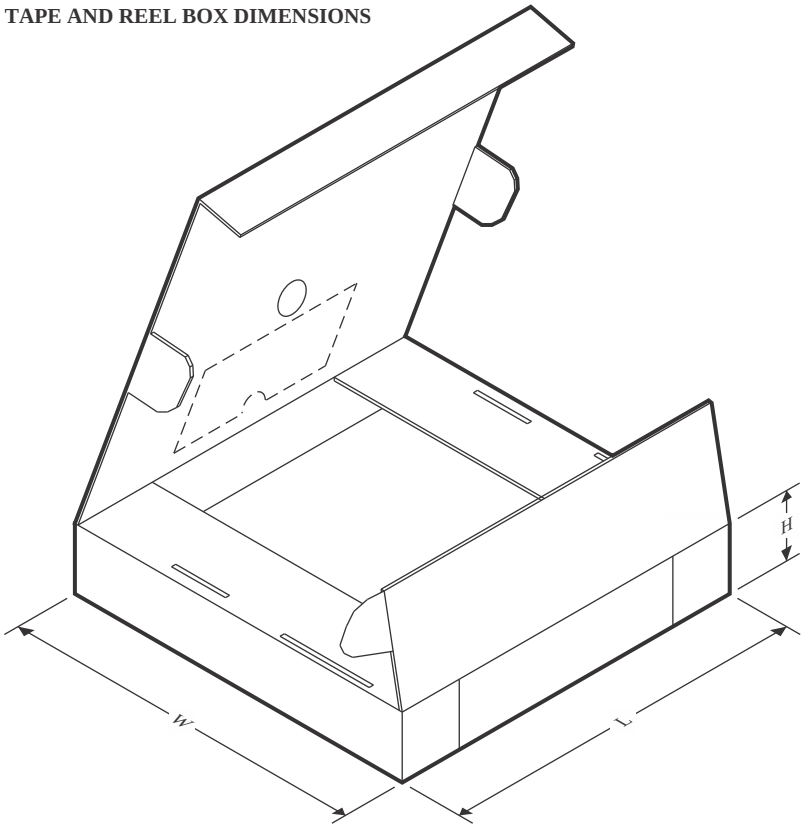
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS1177NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS1178NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

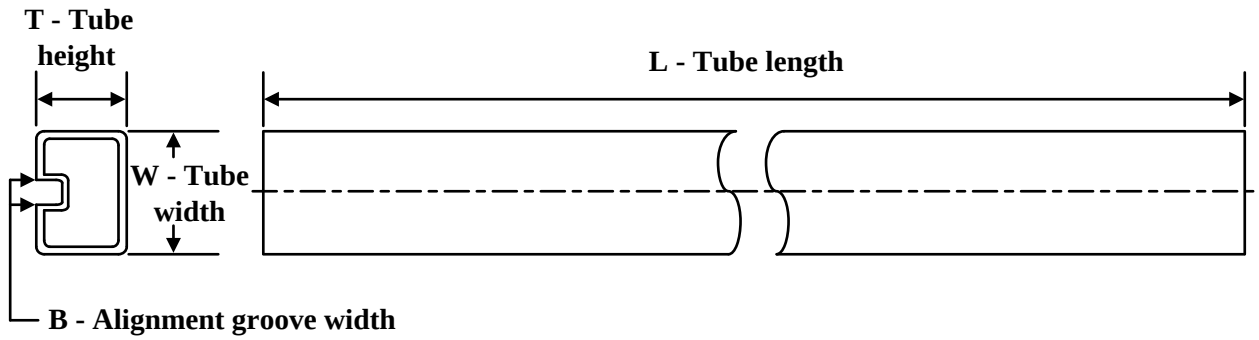
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

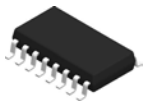
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS1177NSR	SO	NS	16	2000	356.0	356.0	35.0
SN75ALS1178NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS1177N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS1178N	N	PDIP	16	25	506	13.97	11230	4.32

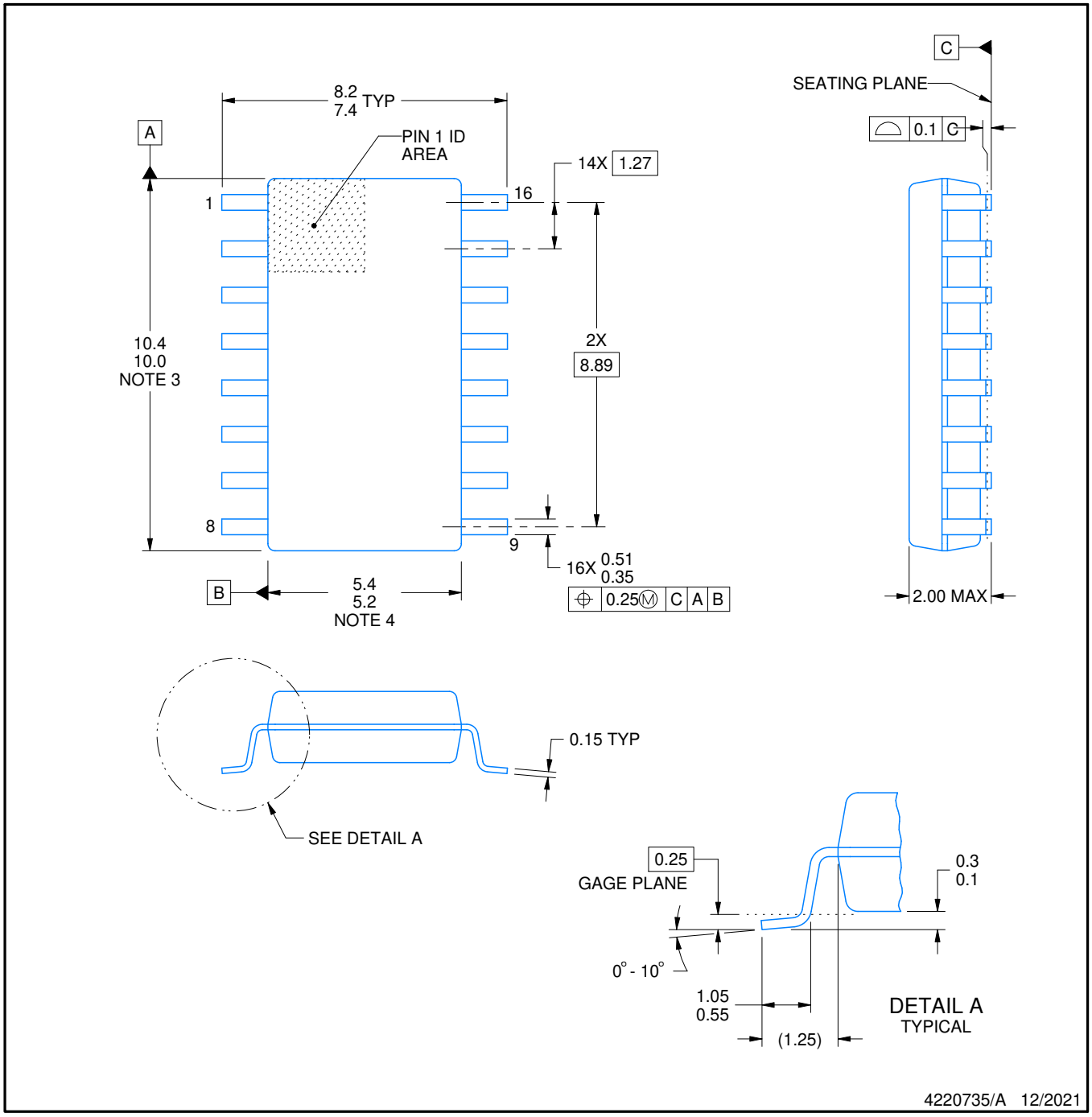


PACKAGE OUTLINE

NS0016A

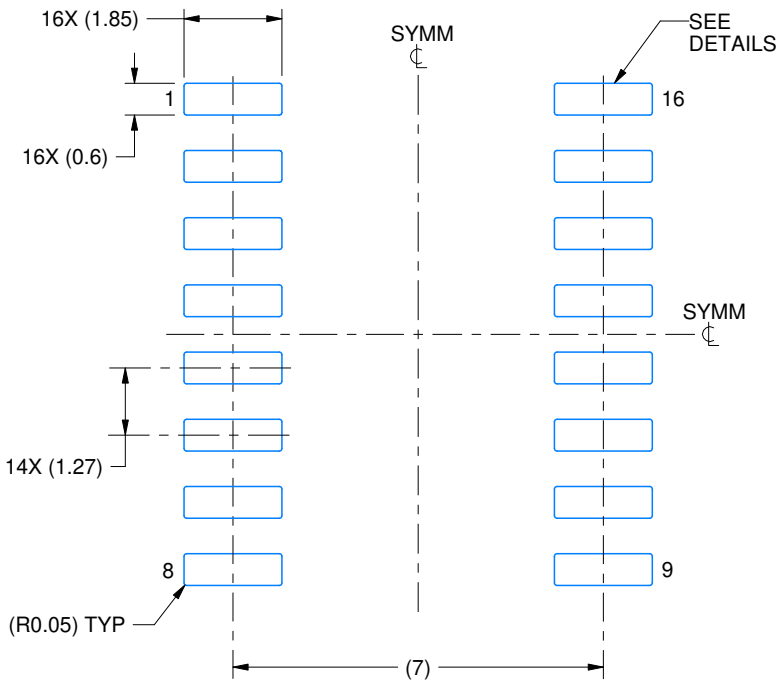
SOP - 2.00 mm max height

SOP

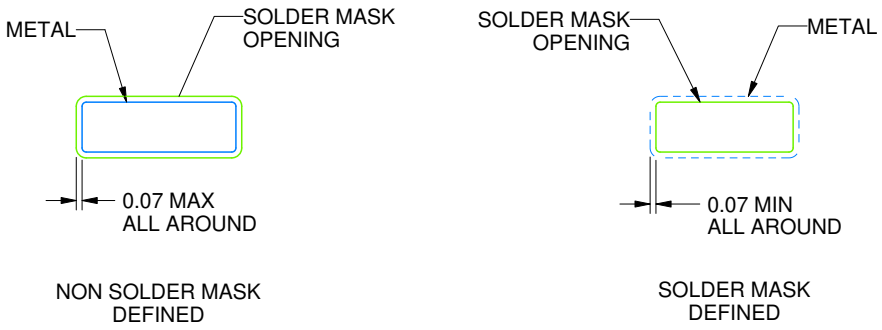


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

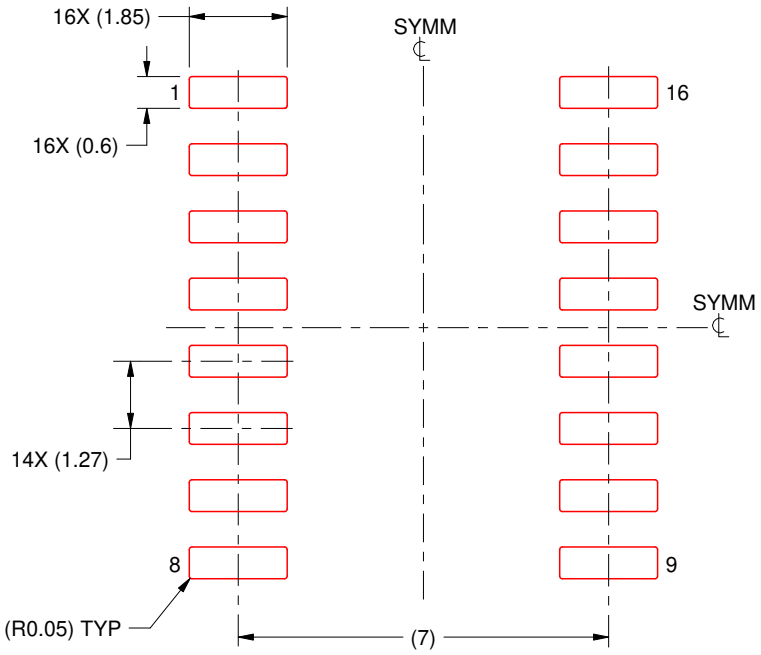


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

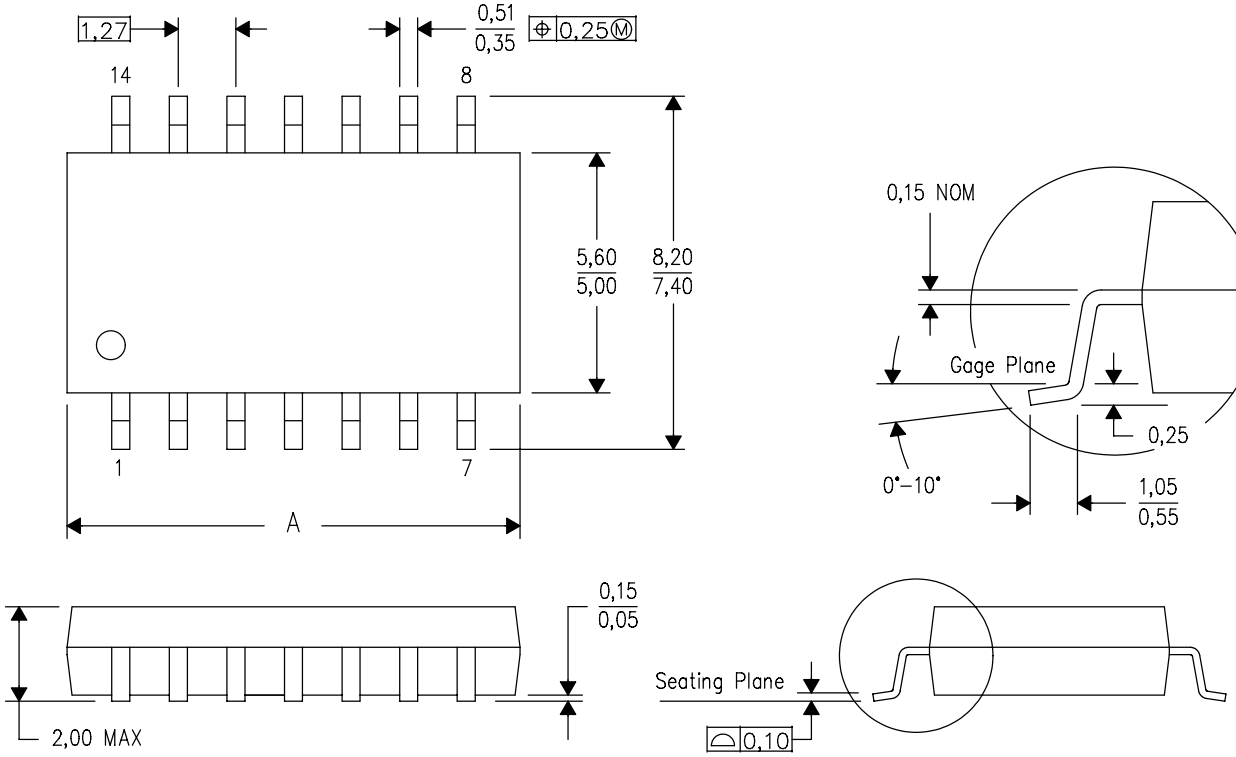
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

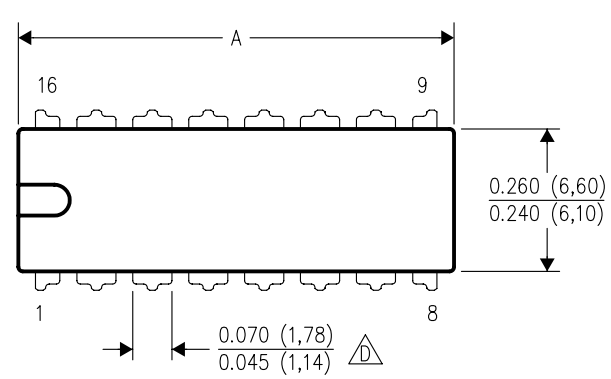
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

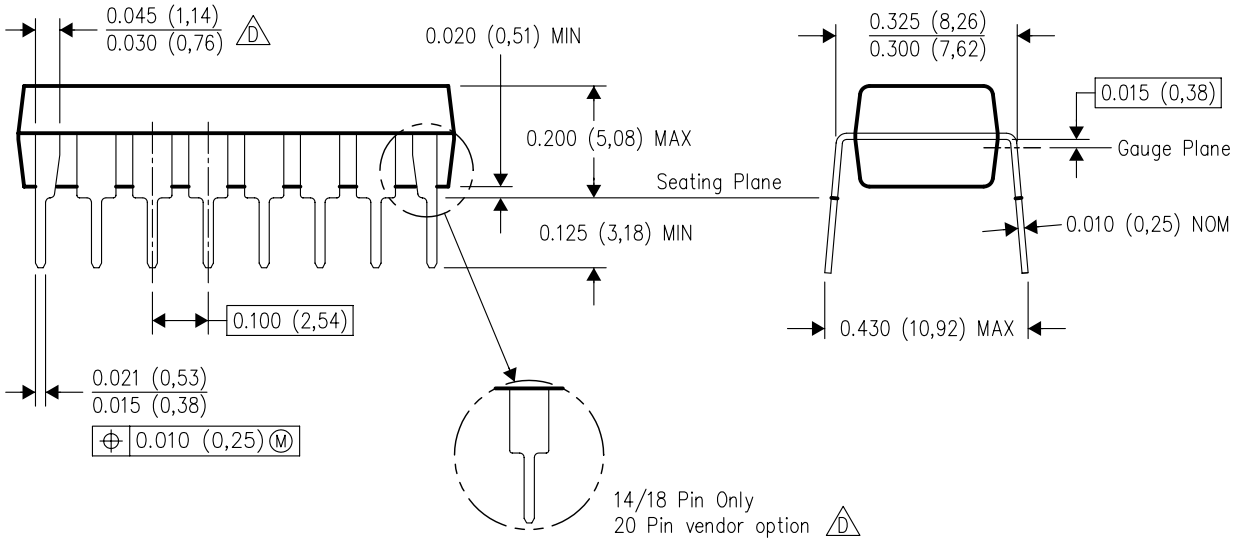
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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