

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL announced Product

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P-CHANNEL MOS FET  
FOR HIGH-SPEED SWITCHING

The 2SJ356 is a P-channel MOS FET of a vertical type and is a switching element that can be directly driven by the output of an IC operating at 5 V.

This product has a low ON resistance and superb switching characteristics and is ideal for driving the actuators and DC/DC converters.

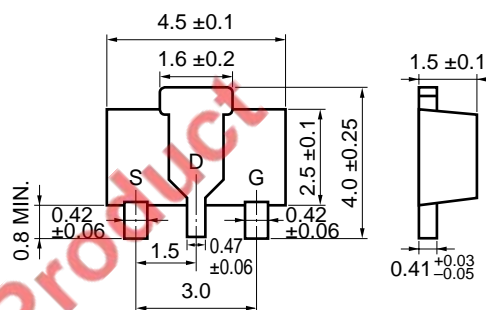
FEATURES

- Can be directly driven by 5-V IC
- Low ON resistance

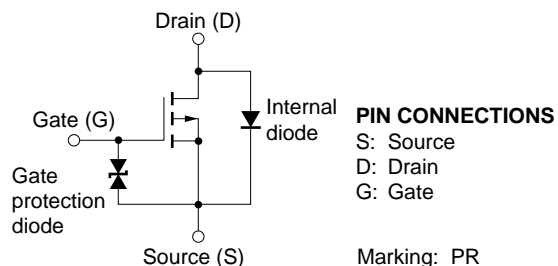
$R_{DS(on)} = 0.95 \Omega$  MAX. @  $V_{GS} = -4 V$ ,  $I_D = -1.0 A$

$R_{DS(on)} = 0.50 \Omega$  MAX. @  $V_{GS} = -10 V$ ,  $I_D = -1.0 A$

PACKAGE DIMENSIONS (in mm)



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Drain to Source Voltage	$V_{DSS}$	$V_{GS} = 0$	-60	V
Gate to Source Voltage	$V_{GSS}$	$V_{DS} = 0$	-20/+10	V
Drain Current (DC)	$I_{D(DC)}$		±2.0	A
Drain Current (Pulse)	$I_{D(pulse)}$	$PW \leq 10 \text{ ms}$ Duty cycle $\leq 1 \%$	±4.0	A
Total Power Dissipation	$P_T$	16 cm <sup>2</sup> × 0.7 mm, ceramic substrate used	2.0	W
Channel Temperature	$T_{ch}$		150	°C
Storage Temperature	$T_{stg}$		-55 to +150	°C

The internal diode connected between the gate and source of this product is to protect the product from static electricity. If the product is used in a circuit where the rated voltage of the product may be exceeded, connect a protection circuit.

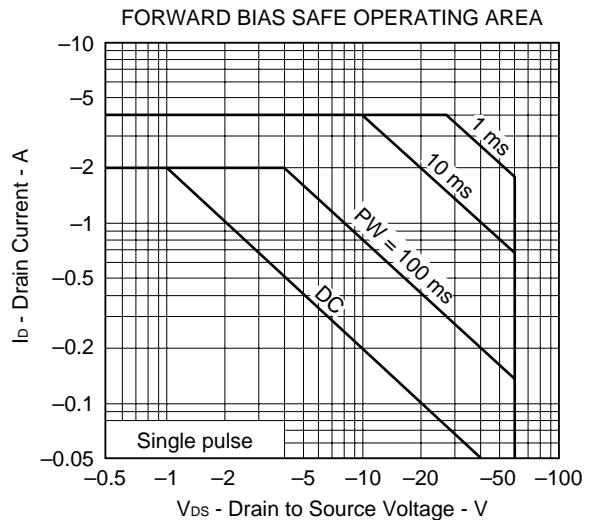
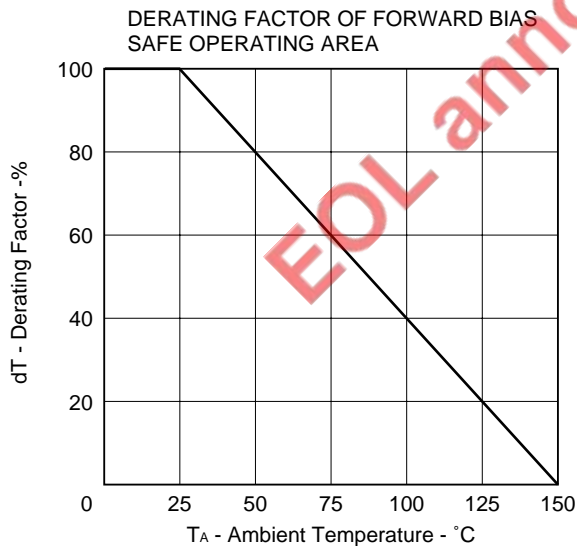
Take adequate preventive measures against static electricity when handling this product.

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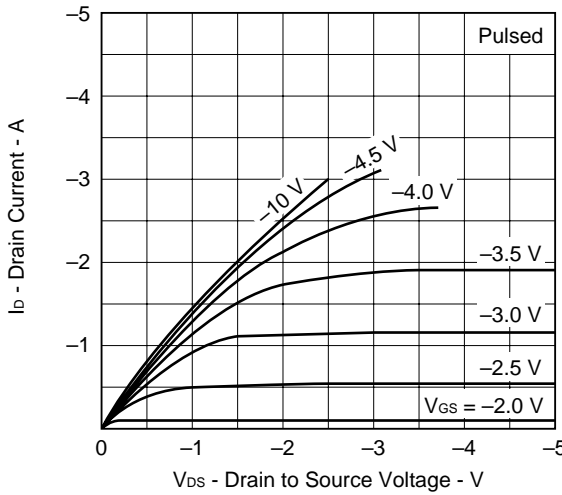
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-Off Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = -16/+10 V, V <sub>DS</sub> = 0			±10	μA
Gate Cut-Off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.4	-2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.0 A	1.0			S
Drain to Source On-State Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -1.0 A		0.65	0.95	Ω
Drain to Source On-State Resistance	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.0 A		0.41	0.50	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1.0 MHz		270		pF
Output Capacitance	C <sub>oss</sub>			145		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			55		pF
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -25 V, I <sub>D</sub> = -1.0 A V <sub>GS(on)</sub> = -10 V R <sub>G</sub> = 10 Ω, R <sub>L</sub> = 25 Ω		4.3		ns
Rise Time	t <sub>r</sub>			21		ns
Turn-Off Delay Time	t <sub>d(off)</sub>			115		ns
Fall Time	t <sub>f</sub>			75		ns
Gate Input Charge	Q <sub>G</sub>	V <sub>DS</sub> = -48 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.0 A, I <sub>G</sub> = -2 mA		11.6		nC
Gate to Source Charge	Q <sub>GS</sub>			1.0		nC
Gate to Drain Charge	Q <sub>GD</sub>			3.8		nC
Internal Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.0 A, di/dt = 50 A/μs		82		ns
Internal Diode Reverse Recovery Charge	Q <sub>rr</sub>			94		nC

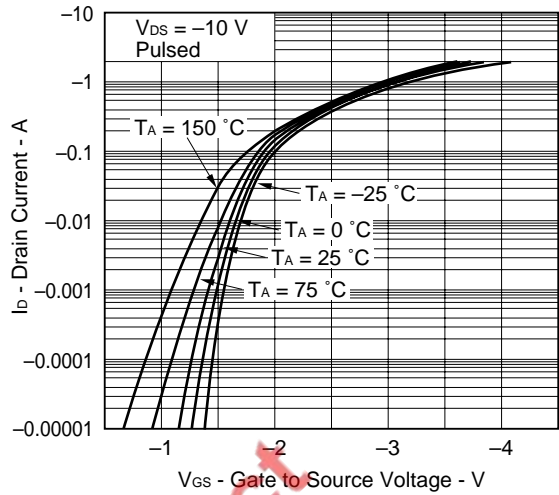
**TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**



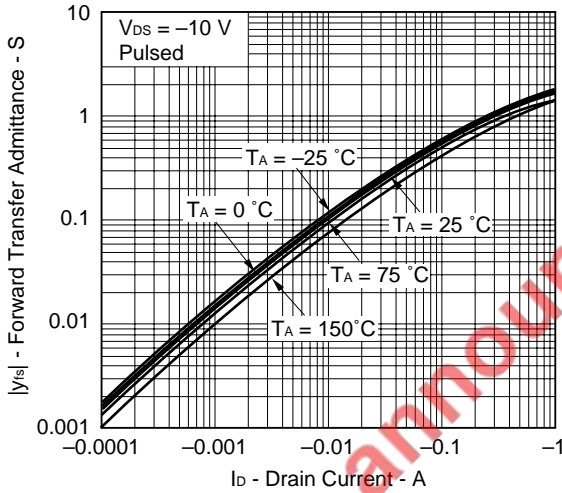
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



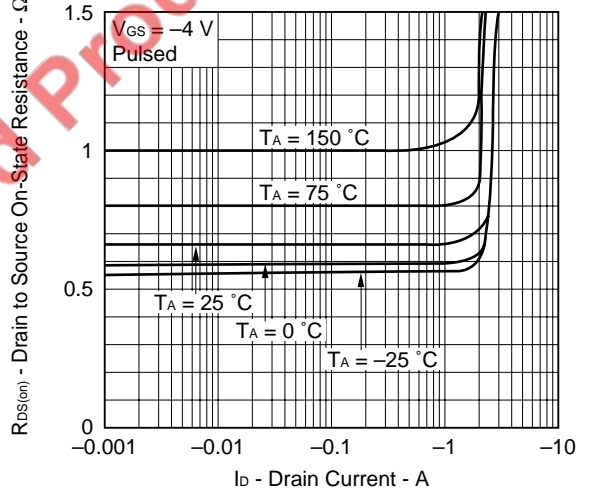
TRANSFER CHARACTERISTICS



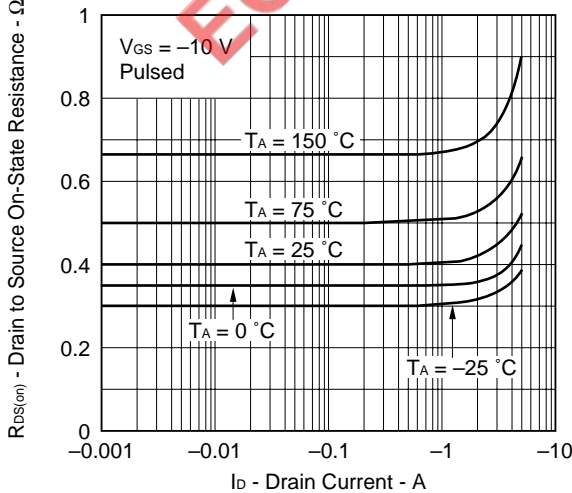
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



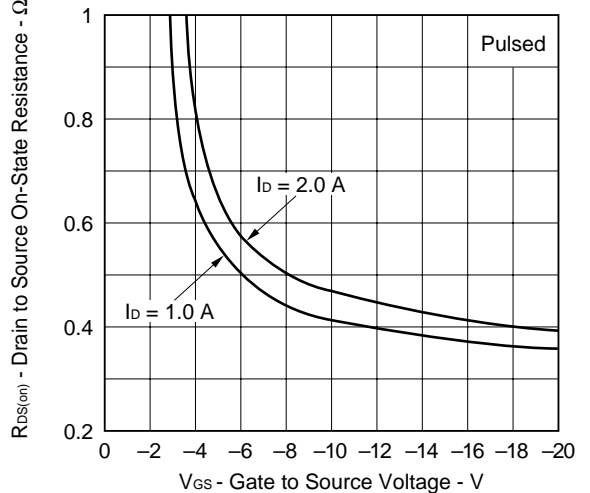
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



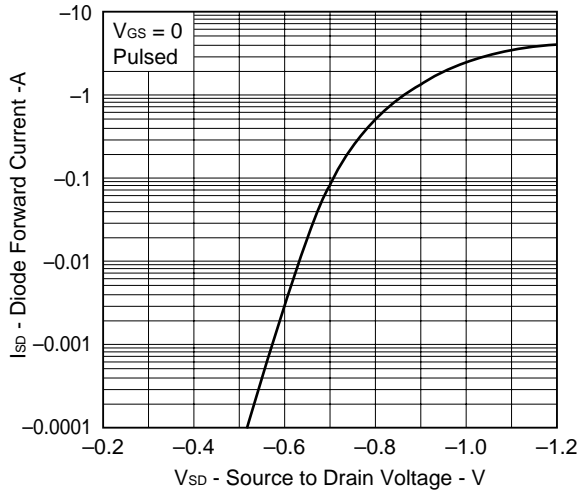
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



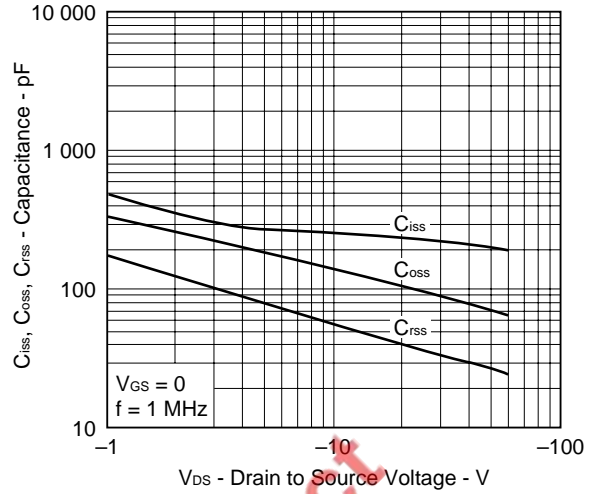
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



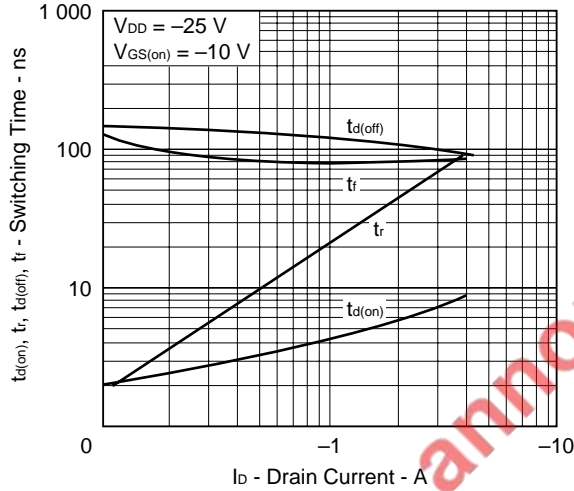
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



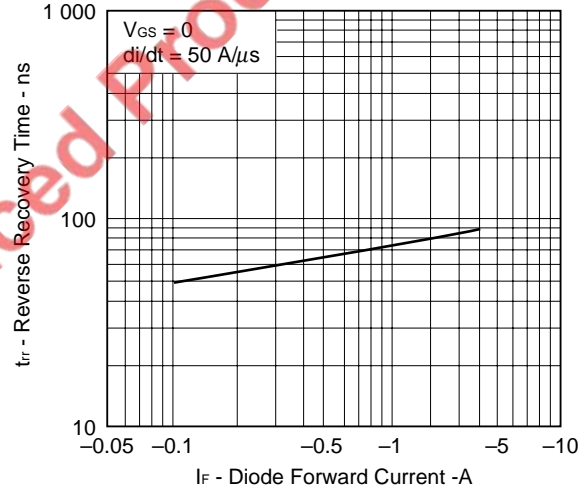
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



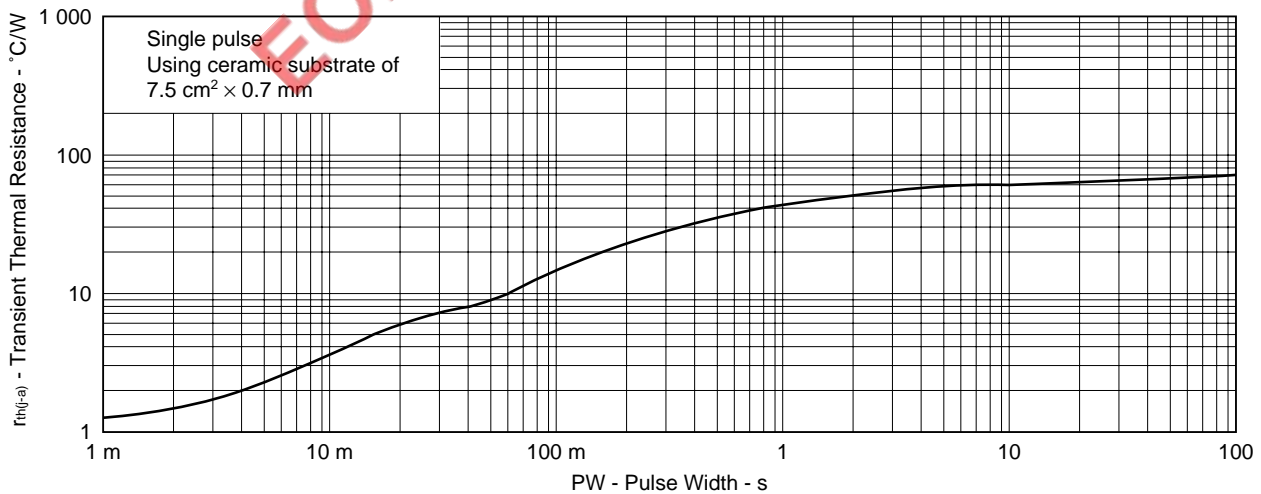
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

**EOL announced Product**

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Anti-radioactive design is not implemented in this product.