STM32 F4 series
High-performance Cortex-M4 MCU

32-bit Flash MCU, 168 MHz/210 DMIPS, with DSP instructions, floating point unit and advanced peripherals

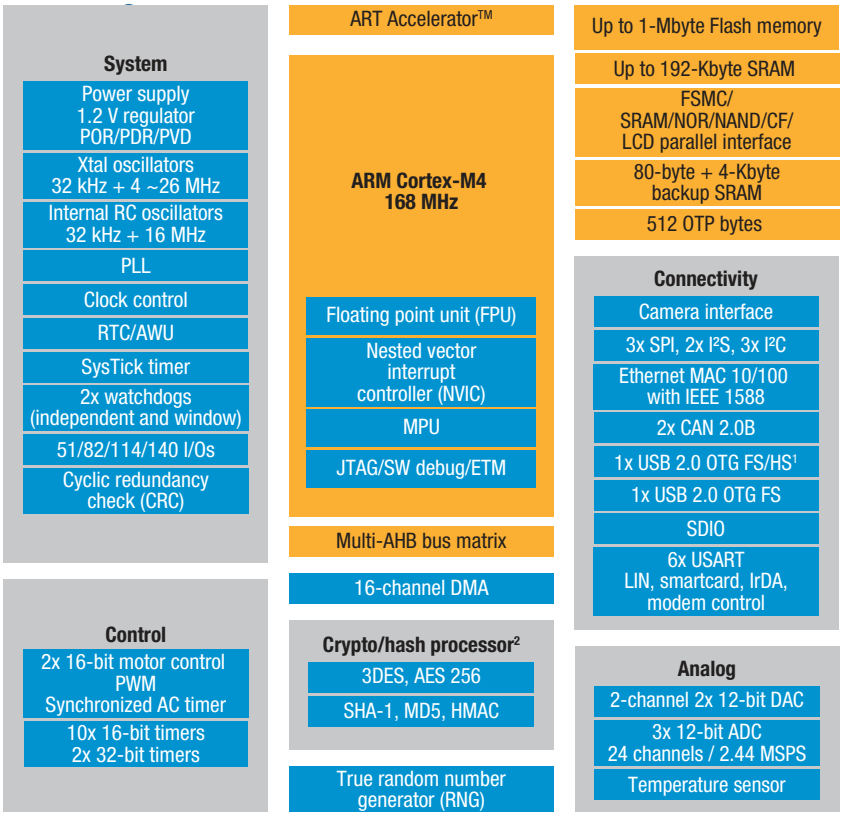
STM32 F4 DSC 32-bit Cortex-M4

ST is widening its target applications arena with the STM32 F4 series. Based on the Cortex-M4 core, this series opens the door to the digital signal controller (DSC) market. This extension to our STM32 product portfolio offers devices with pin-to-pin and software compatibility with the STM32 F2 series, but with more performance, DSP capability, a floating point unit, more SRAM, and peripheral improvements such as full duplex I²S, less than 1 µA RTC and 2.44 MSPS ADCs. The ARM Cortex-M4 core features built-in single-cycle multiply-accumulate (MAC) instructions, optimized SIMD arithmetic and saturating arithmetic instructions. The adaptive real-time ART Accelerator™ combined with ST's 90 nm technology provides linear performance up to 168 MHz, unleashing the full performance of the core. These features expand the number of addressable applications in the industrial, consumer and healthcare segments.

The STM32 F4 series includes devices with 512 Kbytes to 1 Mbyte of on-chip Flash memory, and 192 Kbytes of SRAM, and 15 communication interfaces.

WLCSP (< 4.5 x 4.5 mm), LQFP64, LQFP100, LQFP144, LQFP176 and UFBGA176 packages are available.

Block diagram



Notes:
1. HS requires an external PHY connected to the ULPI interface
2. Crypto/hash processor on STM32F417 and STM32F415

Key figures

- Performance
  - Coremark score: 363.17 at 168 MHz, Coremark/MHz: 2.162
  - Dhrystone score: 210 at 168 MHz
  - Power consumption
  - 230 µA/MHz at 168 MHz running Coremark benchmark from Flash memory (peripherals off)
  - 1.2 V voltage regulator with power scaling capability
  - 1.7 V[4] to 3.6 V V_{DD}
  - <1 µA typ RTC
- High-speed data transfer
  - 7 masters, 8 slaves on the multi AHB bus matrix
- Faster peripherals
  - USART: 10.5 Mbit/s
  - SPI: 37.5 Mbit/s
  - ADC: 2.44 MSPS

Note:
4. 1.7 V available on all packages except the LQFP64

Development tools

As for all STM32 products, a complete development tool offering is available, including the following dedicated kits.

- STM32 F4 Discovery kit (order code: STM32F4DISCOVERY)
- STM32 F4 evaluation board (order codes: STM3240G-EVAL and STM3241G-EVAL[3] for crypto support)
- STM32 F4 starter kits from IAR and Keil (order codes: STM3240G-SK/IAR and STM3240G-SK/KEI)

Note: 3. Contact your local ST sales office.

STM3240G-EVAL

STM32F4DISCOVERY

Features and benefits

Features	Benefits
168 MHz/210 DMIPS Cortex-M4 with single cycle DSP MAC and floating point unit	Boosted execution of control algorithms More features possible for your applications Ease of use Better code efficiency Faster time to market Elimination of scaling and saturation Easier support for meta-language tools
Designed for high performance and ultra fast data transfers ■ ART Accelerator ■ 32-bit, 7-layer AHB bus matrix with 7 masters and 8 slaves including 2 blocks of SRAM ■ Multi DMA controllers: 2 general purpose, 1 for USB HS, 1 for Ethernet ■ One SRAM block dedicated to the core	Performance equivalent to 0-wait execution from Flash Concurrent execution and data transfers Simplified resource allocation
Outstanding power efficiency ■ Ultra-low dynamic power ■ RTC <1 µA typ in V_{BAT} mode ■ 3.6 V down to 1.7 V[1] V_{DD} ■ Voltage regulator with power scaling capability	Extra flexibility to reduce power consumption for applications requiring both high processing and low power performance when running at low voltage or on a rechargeable battery
Maximum integration Up to 1 Mbyte of on-chip Flash memory, 192 Kbytes of SRAM, reset circuit, internal RCs, PLLs, WLCSP package available	More features in space constrained applications
Superior and innovative peripherals ■ Connectivity: camera interface, crypto/hash HW processor, Ethernet MAC10/100 with IEEE 1588 v2 support, 2 USB OTG (one with HS support), ■ Audio: dedicated audio PLL and 2 full duplex I²S ■ Up to 15 communication interfaces (including 6x USART, 3x SPI, 3x I²C, 2x CAN, SDIO) ■ Analog: 2x 12-bit DACs, 3x 12-bit ADC reaching 7.32 MSPS in interleaved mode ■ Up to 17 timers: 16 and 32 bits running up to 168 MHz	New possibilities to connect and communicate high speed data
	More precision thanks to high resolution
Extensive tools and software solutions Various IDE, starter kits, libraries, RTOS and stacks, either open source or provided by ST or 3rd parties, including the ARM CMSIS DSP library optimized for Cortex-M4 instructions	A wide choice within the STM32 ecosystem to develop your applications

Note: 1. 1.7 V available on all packages except the LQFP64

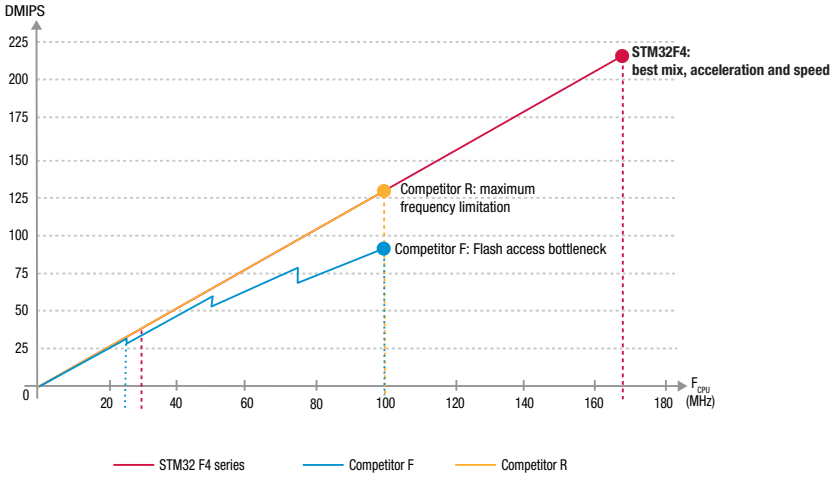
ART Accelerator™ performance result

Unleashing the full performance of the core beyond the embedded Flash intrinsic speed is an art.

Combined with ST's 90 nm technology, the ART Accelerator achieves a linear performance up to 168 MHz, offering 210 DMIPS and 363 Coremark performance executing from Flash.

The acceleration mechanism is made possible using a prefetch queue, a branch cache and a smart arbitration mechanism.

- MCUs using less advanced accelerators or slower embedded Flash memories will impact exectution performance as wait states occur.
- MCUs using faster Flash but no branch cache acceleration to achieve performance usually show higher power consumption as a result of more accesses to a power hungry Flash.



Device summary

Part number	Package	Flash size (Kbytes)	Internal RAM size (Kbytes)	Timer functions		ADC	DAC	I/Os (high current)	Serial interface	Supply voltage (Vcc) (V)	Supply current (Icc)		Temperature (°C)
				16-bit (IC/OC/ PWM)	Others						Lowest power mode (µA)	Run mode (µA/ MHz)	
STM32F405/415: 1x USB OTG (FS/HS[1]), crypto/hash processor[2]													
STM32F405RG	LQFP64 (10x10) WLCSP64	1024	192	12x16-bit (24/24/30)	2x32-bit timers (8/8/8), 2x WDG, RTC, 24-bit down counter, 2x16-bit basic timers	16x12-bit	2x12-bit	51(51)	3xSPI, 2xI²S, 2xI²C, 3xUSART (IrDa, ISO 7816), 3xUART, 1x USB OTG FS/HS, 2xCAN, SDIO	1.7[3]/1.8 to 3.6	2.5	230	-40 to +85 or -40 to +105
STM32F415RG[2]	LQFP64 (10x10) WLCSP64	1024	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	51(51)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F405VG	LQFP100 (14x14)	1024	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	82(82)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F415VG[2]	LQFP100 (14x14)	1024	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	82(82)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F405ZG	LQFP144 (20x20)	1024	192	12x16-bit (24/24/30)		24x12-bit	2x12-bit	114(114)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F415ZG[2]	LQFP144 (20x20)	1024	192	12x16-bit (24/24/30)		24x12-bit	2x12-bit	114(114)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F407/417: 2x USB OTG (FS + /HS[1]), camera IF, crypto/hash processor[2]													
STM32F407IE	UFBGA176 (10x10) LQFP176 (24x24)	512	192	12x16-bit (24/24/30)	2x32-bit timers (8/8/8), 2 x WDG, RTC, 24-bit down counter, 2x16-bit basic timers	24x12-bit	2x12-bit	140(140)	3xSPI, 2xI²S, 2xI²C, 3xUSART (IrDa, ISO 7816), 3xUART, 2x USB OTG FS/HS, 2xCAN, Ethernet MAC10/100, SDIO	1.7[3]/1.8 to 3.6	2.5	230	-40 to +85 or -40 to +105
STM32F417IE[2]	UFBGA176 (10x10) LQFP176 (24x24)	512	192	12x16-bit (24/24/30)		24x12-bit	2x12-bit	140(140)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F407IG	UFBGA176 (10x10) LQFP176 (24x24)	1024	192	12x16-bit (24/24/30)		24x12-bit	2x12-bit	140(140)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F417IG[2]	UFBGA176 (10x10) LQFP176 (24x24)	1024	192	12x16-bit (24/24/30)		24x12-bit	2x12-bit	140(140)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F407VE	LQFP100 (14x14)	512	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	82(82)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F417VE[2]	LQFP100 (14x14)	512	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	82(82)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F407VG	LQFP100 (14x14)	1024	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	82(82)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F417VG[2]	LQFP100 (14x14)	1024	192	12x16-bit (24/24/30)		16x12-bit	2x12-bit	82(82)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F407ZE	LQFP144 (20x20)	512	192	12x16-bit (24/24/30)		2x12-bit	2x12-bit	114(114)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F417ZE[2]	LQFP144 (20x20)	512	192	12x16-bit (24/24/30)		2x12-bit	2x12-bit	114(114)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F407ZG	LQFP144 (20x20)	1024	192	12x16-bit (24/24/30)		2x12-bit	2x12-bit	114(114)		1.7[3]/1.8 to 3.6	2.5	230	
STM32F417ZG[2]	LQFP144 (20x20)	1024	192	12x16-bit (24/24/30)		2x12-bit	2x12-bit	114(114)		1.7[3]/1.8 to 3.6	2.5	230	

Notes:
1. HS requires an external PHY connected to ULPI interface
2. Crypto/hash processor on STM32F417 and STM32F415
3. Available on all packages except LQFP64. 1.7V requires external reset circuitry.

Order code: BRSTM32F40911

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