

# BLF4G22-100; BLF4G22S-100

UHF power LDMOS transistor

Rev. 01 — 10 January 2006

Product data sheet

## 1. Product profile

### 1.1 General description

100 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

**Table 1: Typical performance**

$T_{case} = 25\text{ }^{\circ}\text{C}$ ; in a common source class-AB test circuit;  $I_{Dq} = 900\text{ mA}$ ; typical values

Mode of operation	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)	IMD3 (dBc)	ACPR (dBc)
2-carrier W-CDMA [1]	$f_1 = 2135$ ; $f_2 = 2145$	28	25 (AV)	13.5	26	-37	-41

[1] 10 MHz carrier spacing PAR 7 dB at 0.01 % probability on CCDF, 3GPP test model 1, 1 to 64 DPCH.

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features

- Typical 2-Carrier W-CDMA performance at a supply voltage of 28 V and an  $I_{Dq}$  of 900 mA:
  - ◆ Load power = 25 W (AV)
  - ◆ Gain = 13.5 dB (typ)
  - ◆ Efficiency = 26 % (typ)
  - ◆ ACPR = -41 dBc (typ)
  - ◆ IMD3 = -37 dBc (typ)
- Easy power control
- Integrated ESD protection
- Excellent ruggedness > 10 : 1 VSWR at 100 W CW
- High efficiency
- High peak power capability (> 150 W)
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use

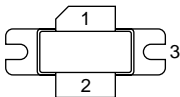
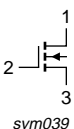
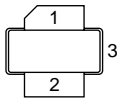
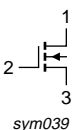
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## 1.3 Applications

- RF power amplifiers for W-CDMA base stations and multicarrier applications in the 2000 MHz to 2200 MHz frequency range.

## 2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
<b>BLF4G22-100 (SOT502A)</b>			
1	drain		 sym039
2	gate		
3	source		
<b>BLF4G22S-100 (SOT502B)</b>			
1	drain		 sym039
2	gate		
3	source		

[1] Connected to flange

## 3. Ordering information

Table 3: Ordering information

Type number	Package		Version
	Name	Description	
BLF4G22-100	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF4G22S-100	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

## 4. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+15	V
$I_D$	drain current		-	12	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$ ; $P_L = 25\text{ W}$ ; 2-carrier W-CDMA	-	0.76	0.85	K/W

## 6. Characteristics

**Table 6: Characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 180\text{ mA}$	2.5	3.1	3.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$ ; $I_D = 900\text{ mA}$	2.7	3.2	3.7	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$	-	-	3	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 6\text{ V}$ ; $V_{DS} = 10\text{ V}$	27	30	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 15\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	300	nA
$g_{fs}$	transfer conductance	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ A}$	-	9.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 6\text{ V}$ ; $I_D = 6\text{ A}$	-	0.09	-	$\Omega$
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 28\text{ V}$ ; $f = 1\text{ MHz}$	-	2.5	-	pF

## 7. Application information

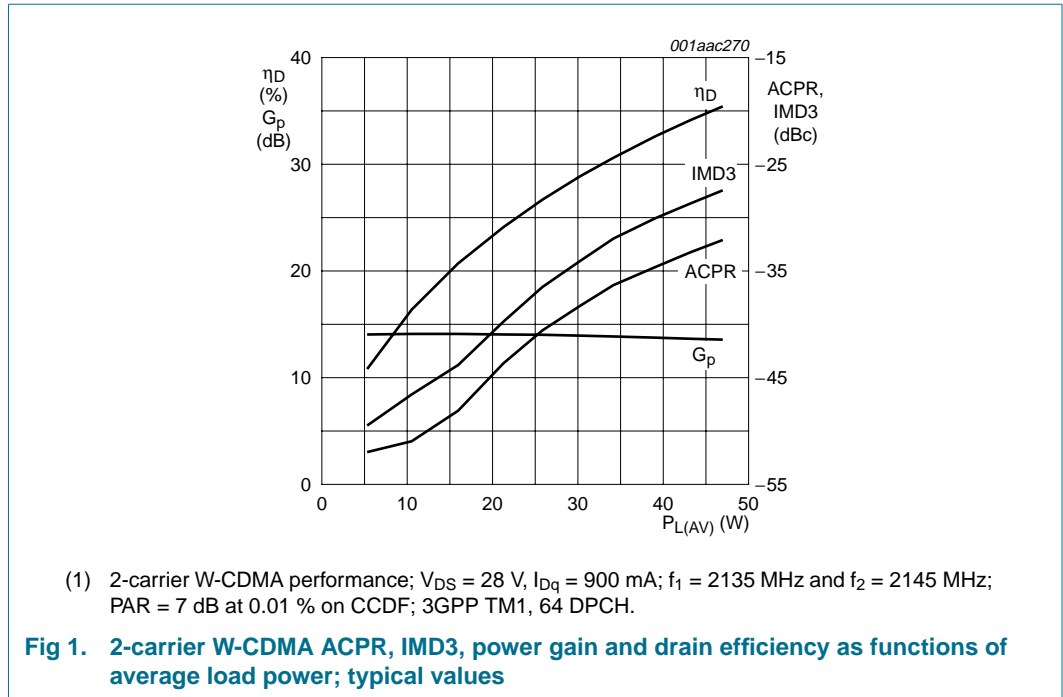
**Table 7: Application information**

Mode of operation: 2-Carrier W-CDMA, PAR 7 dB at 0.01 % probability on CCDF, 3GPP test model 1, 1-64 DPCH,  $f_1 = 2112.5\text{ MHz}$ ,  $f_2 = 2122.5\text{ MHz}$ ,  $f_3 = 2157.5\text{ MHz}$ ,  $f_4 = 2167.5\text{ MHz}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 25\text{ W}$	12.5	13.5	-	dB
IRL	input return loss	$P_{L(AV)} = 25\text{ W}$	9	15	-	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 25\text{ W}$	24	26	-	%
IMD3	third order intermodulation distortion	$P_{L(AV)} = 25\text{ W}$	-	-37	-35	dBc
ACPR	adjacent channel power ratio	$P_{L(AV)} = 25\text{ W}$	-	-41	-39	dBc

### 7.1 Ruggedness in class-AB operation

The BLF4G22-100/BLF4G22S-100 are capable of withstanding a load mismatch corresponding to VSWR > 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $P_L = 100\text{ W}$  (CW).



**Table 8: Typical impedance values**

$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 900\text{ mA}$ ;  $P_L = 25\text{ W (AV)}$ ;  $T_{case} = 25\text{ °C}$ .

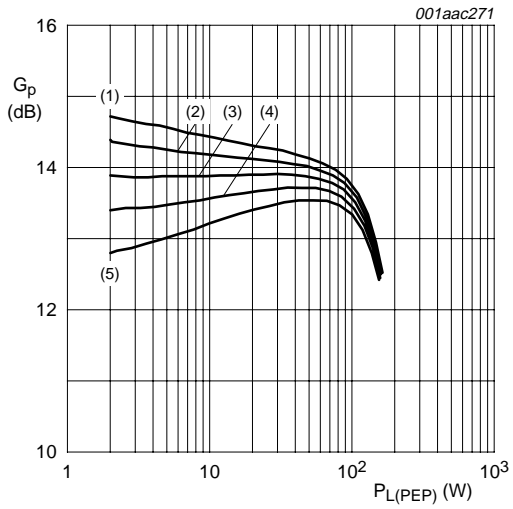
Frequency (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
2110	2.2 + j4.8	1.5 - j2.6
2140	2.2 + j4.6	1.5 - j2.4
2170	2.2 + j4.5	1.4 - j2.2

**Table 9: RF gain grouping**

Code [1]	Gain (dB) [2]	
	Min	Max
A	12.5	13.0
B	13.0	13.5
C	13.5	14.0
D	14.0	14.5
E	14.5	-

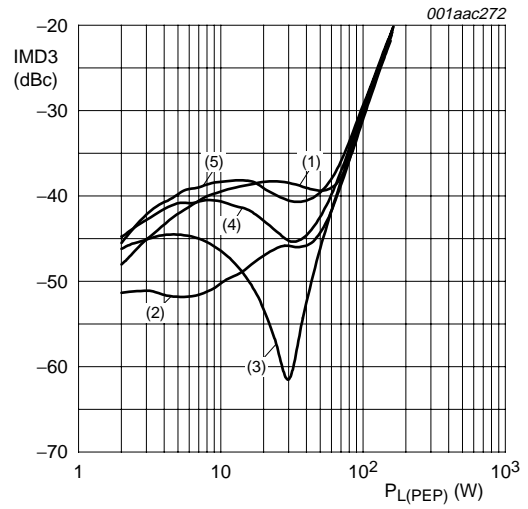
[1] 0.2 dB overlap is allowed for measurement reproducibility.

[2] For 2-carrier W-CDMA at  $f_1 = 2157\text{ MHz}$ ,  $f_2 = 2167.5\text{ MHz}$ .



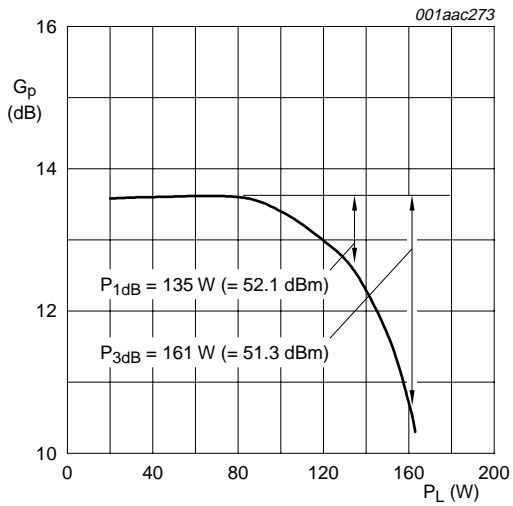
(1)  $I_{Dq} = 600 \text{ mA}$   
 (2)  $I_{Dq} = 750 \text{ mA}$   
 (3)  $I_{Dq} = 900 \text{ mA}$   
 (4)  $I_{Dq} = 1050 \text{ mA}$   
 (5)  $I_{Dq} = 1200 \text{ mA}$   
 Two-tone measurement;  
 $V_{DS} = 28 \text{ V}$ ;  $f_1 = 2140.0 \text{ MHz}$ ;  $f_2 = 2140.1 \text{ MHz}$

**Fig 2. Power gain as a function of peak envelope load power; typical values**



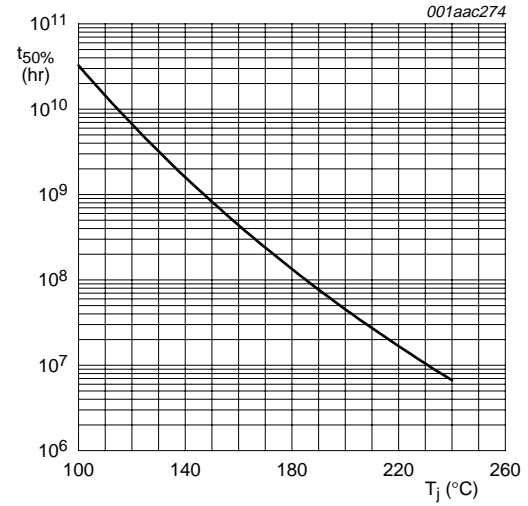
(1)  $I_{Dq} = 600 \text{ mA}$   
 (2)  $I_{Dq} = 750 \text{ mA}$   
 (3)  $I_{Dq} = 900 \text{ mA}$   
 (4)  $I_{Dq} = 1050 \text{ mA}$   
 (5)  $I_{Dq} = 1200 \text{ mA}$   
 Two-tone measurement;  
 $V_{DS} = 28 \text{ V}$ ;  $f_1 = 2140.0 \text{ MHz}$ ;  $f_2 = 2140.1 \text{ MHz}$

**Fig 3. Third order intermodulation distortion as a function of peak envelope power; typical values**



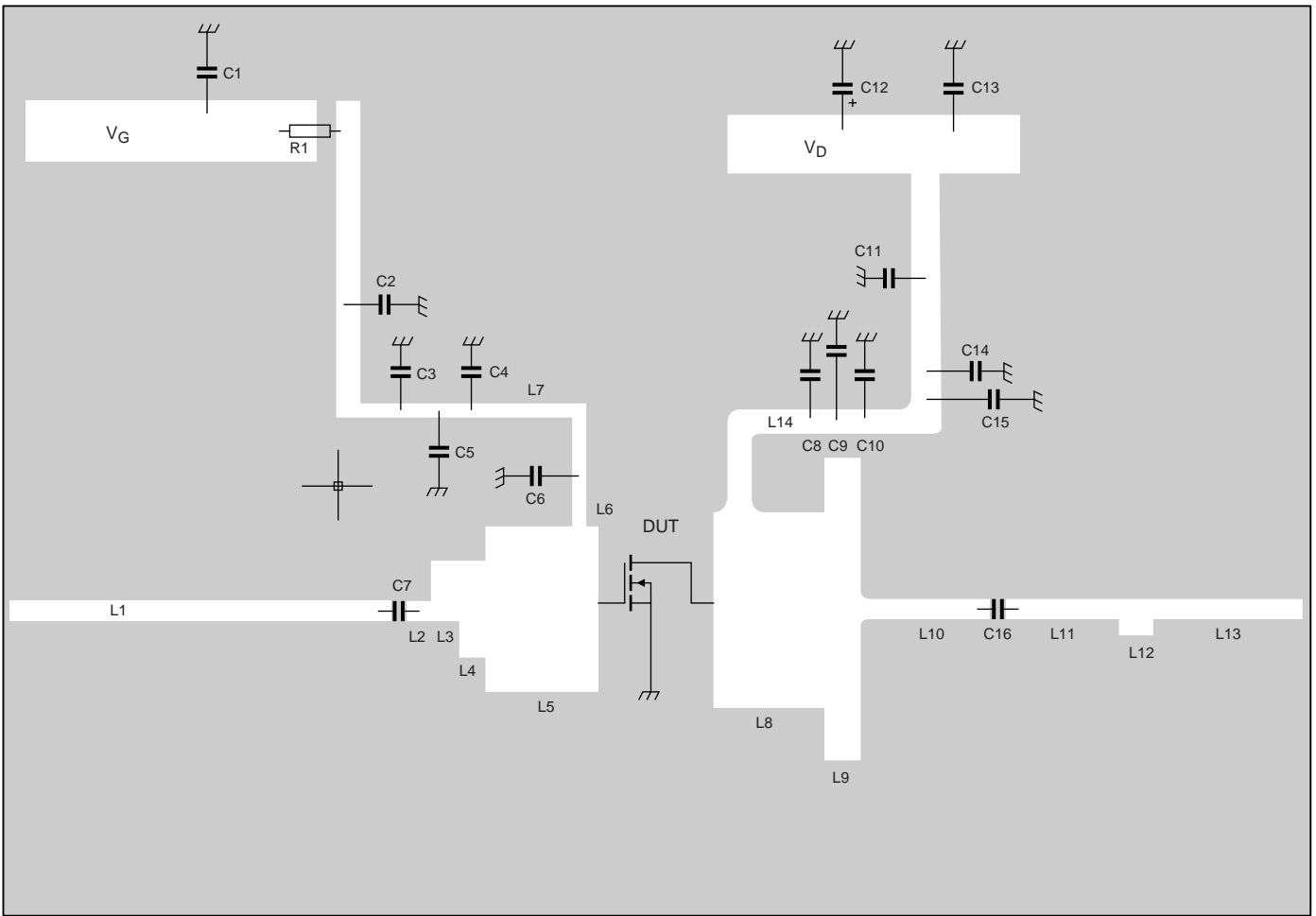
$t_{on} = 8 \mu\text{s}$   
 $t_{off} = 1 \text{ ms}$

**Fig 4. Pulsed peak power capability; typical values**



**Fig 5.  $t_{50\%}$  failures due to electromigration as a function of junction temperature**

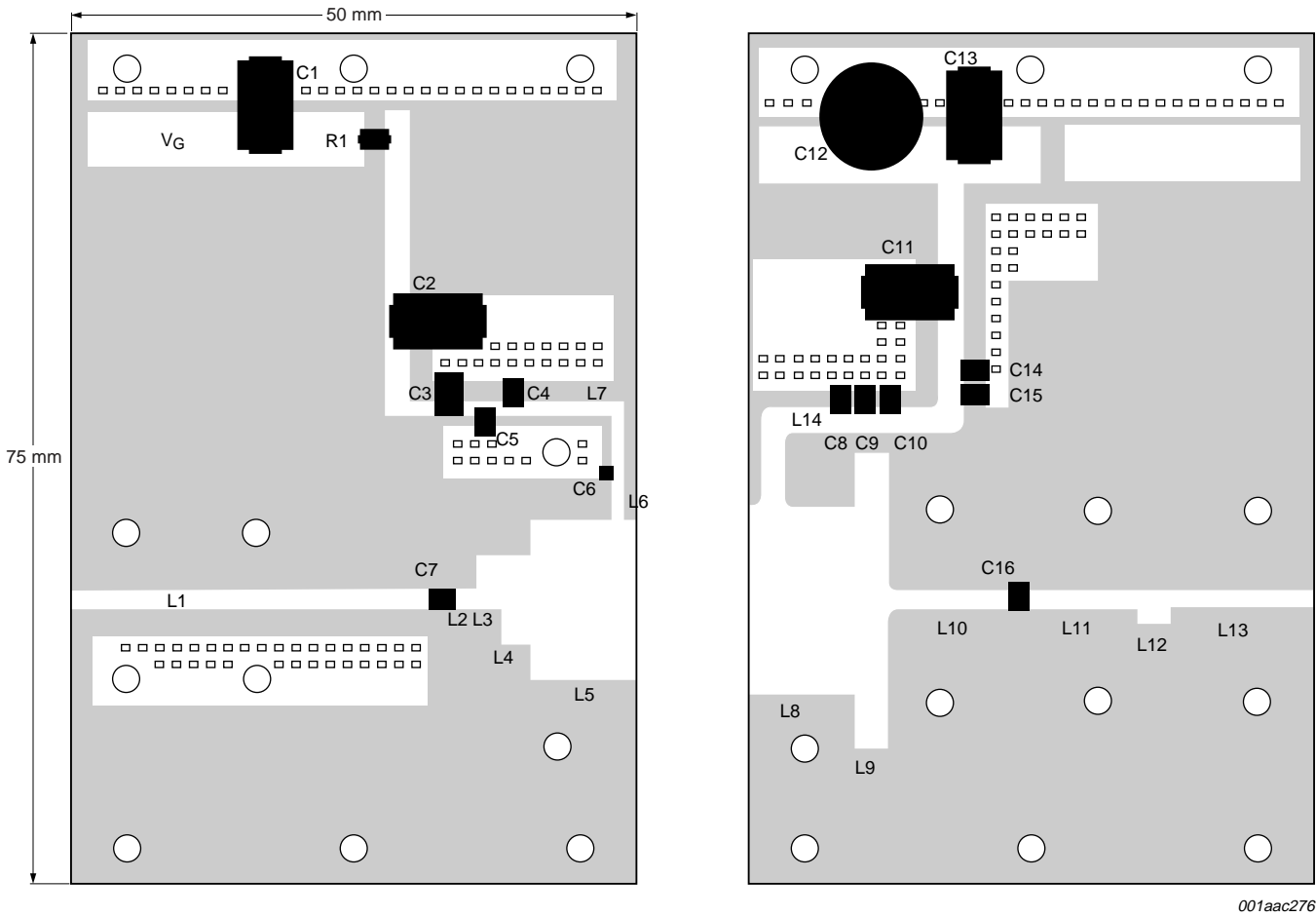
**8. Test information**



001aac275

See [Table 10](#) for list of components

**Fig 6. Test circuit for operation at 2.14 GHz**



The components are situated on double copper-clad Taconic RF35 Printed-Circuit Board (PCB) ( $\epsilon_r = 3.5$ ); thickness = 0.76 mm.

The other side is unetched and serves as a ground plane.

See [Table 10](#) for list of components.

**Fig 7. Component layout for 2.14 GHz test circuit**

Table 10: List of components (see Figure 6 and Figure 7 )

Component	Description	Value	Dimensions
C1, C2, C11	tantalum capacitor	10 $\mu$ F; 35 V	
C3	multilayer ceramic chip capacitor	4.7 $\mu$ F; 25 V	
C4, C10	multilayer ceramic chip capacitor	[1] 8.2 pF	
C5, C8, C14, C15	multilayer ceramic chip capacitor	1.5 $\mu$ F; 50 V	
C6	multilayer ceramic chip capacitor	[2] 0.6 pF	
C7	multilayer ceramic chip capacitor	[1] 4.7 pF	
C9	multilayer ceramic chip capacitor	220 nF; 50 V	
C12	electrolytic capacitor	220 $\mu$ F; 63 V	
C13	tantalum capacitor	4.7 $\mu$ F; 50 V	
C16	multilayer ceramic chip capacitor	[3] 7.5 pF	
L1	stripline	[4] $Z_0 = 50 \Omega$	(W $\times$ L) 32.3 mm $\times$ 1.7 mm
L2	stripline	[4] $Z_0 = 50 \Omega$	(W $\times$ L) 2.2 mm $\times$ 1.7 mm
L3	stripline	[4] $Z_0 = 24 \Omega$	(W $\times$ L) 2.3 mm $\times$ 4.8 mm
L4	stripline	[4] $Z_0 = 15 \Omega$	(W $\times$ L) 2.4 mm $\times$ 8 mm
L5	stripline	[4] $Z_0 = 9.5 \Omega$	(W $\times$ L) 9.3 mm $\times$ 14 mm
L6	stripline	[4] $Z_0 = 60 \Omega$	(W $\times$ L) 4 mm $\times$ 1.2 mm
L7	stripline	[4] $Z_0 = 60 \Omega$	(W $\times$ L) 14.5 mm $\times$ 1.2 mm
L8	stripline	[4] $Z_0 = 8.2 \Omega$	(W $\times$ L) 9.3 mm $\times$ 16.8 mm
L9	stripline	[4] $Z_0 = 5.5 \Omega$	(W $\times$ L) 3 mm $\times$ 25.8 mm
L10	stripline	[4] $Z_0 = 50 \Omega$	(W $\times$ L) 11 mm $\times$ 1.7 mm
L11	stripline	[4] $Z_0 = 50 \Omega$	(W $\times$ L) 9.5 mm $\times$ 1.7 mm
L12	stripline	[4] $Z_0 = 34 \Omega$	(W $\times$ L) 3 mm $\times$ 3 mm
L13	stripline	[4] $Z_0 = 50 \Omega$	(W $\times$ L) 12.7 mm $\times$ 1.7 mm
L14	stripline	[4] $Z_0 = 43 \Omega$	(W $\times$ L) 13.5 mm $\times$ 2.1 mm
R1	SMD resistor	4.7 $\Omega$ ; 0.1 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] American Technical Ceramics type 180R or capacitor of same quality.

[4] Striplines are on a double copper-clad Taconic RF35 PCB ( $\epsilon_r = 3.5$ ); thickness = 0.76 mm.



**9. Package outline**

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

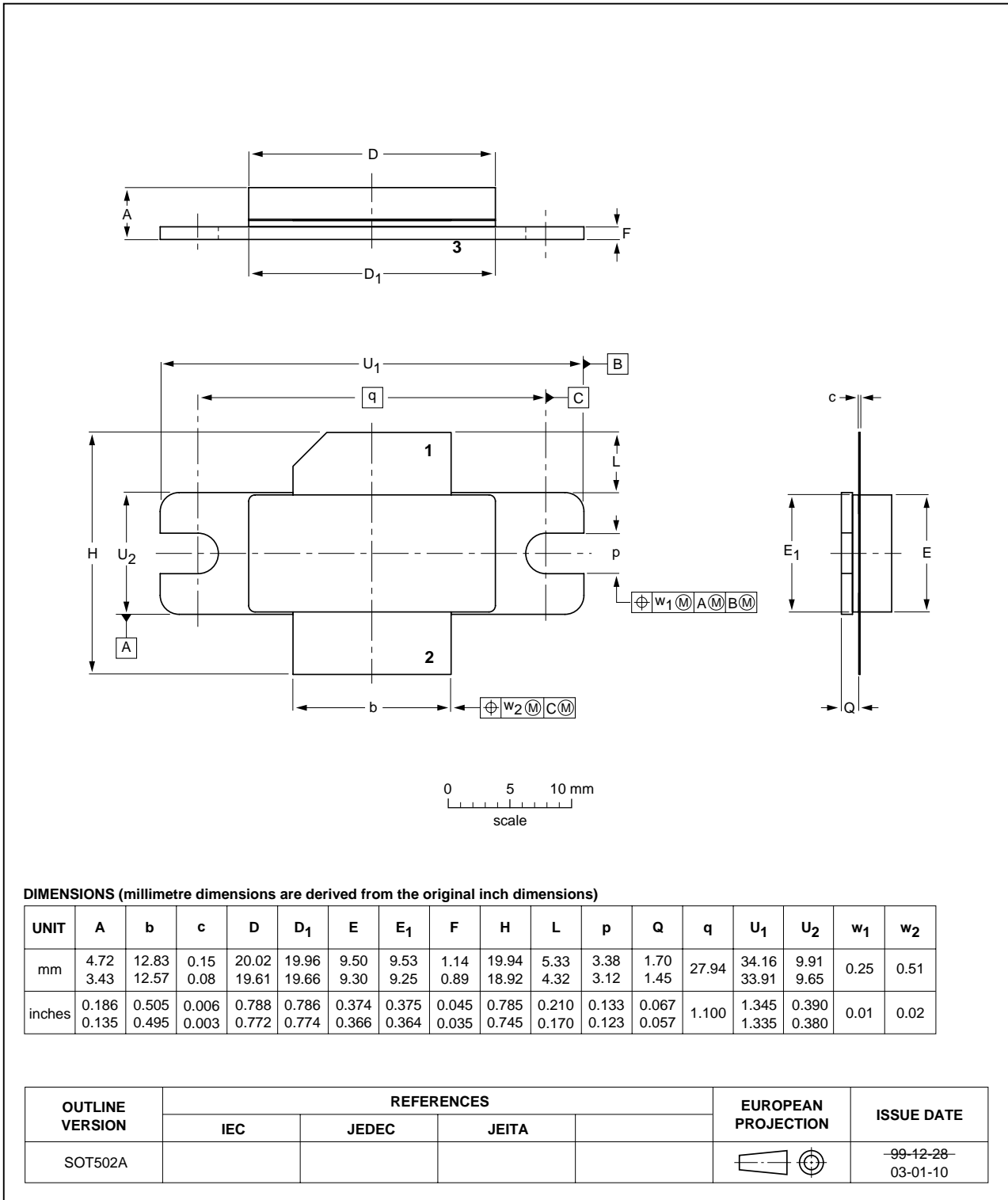


Fig 8. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

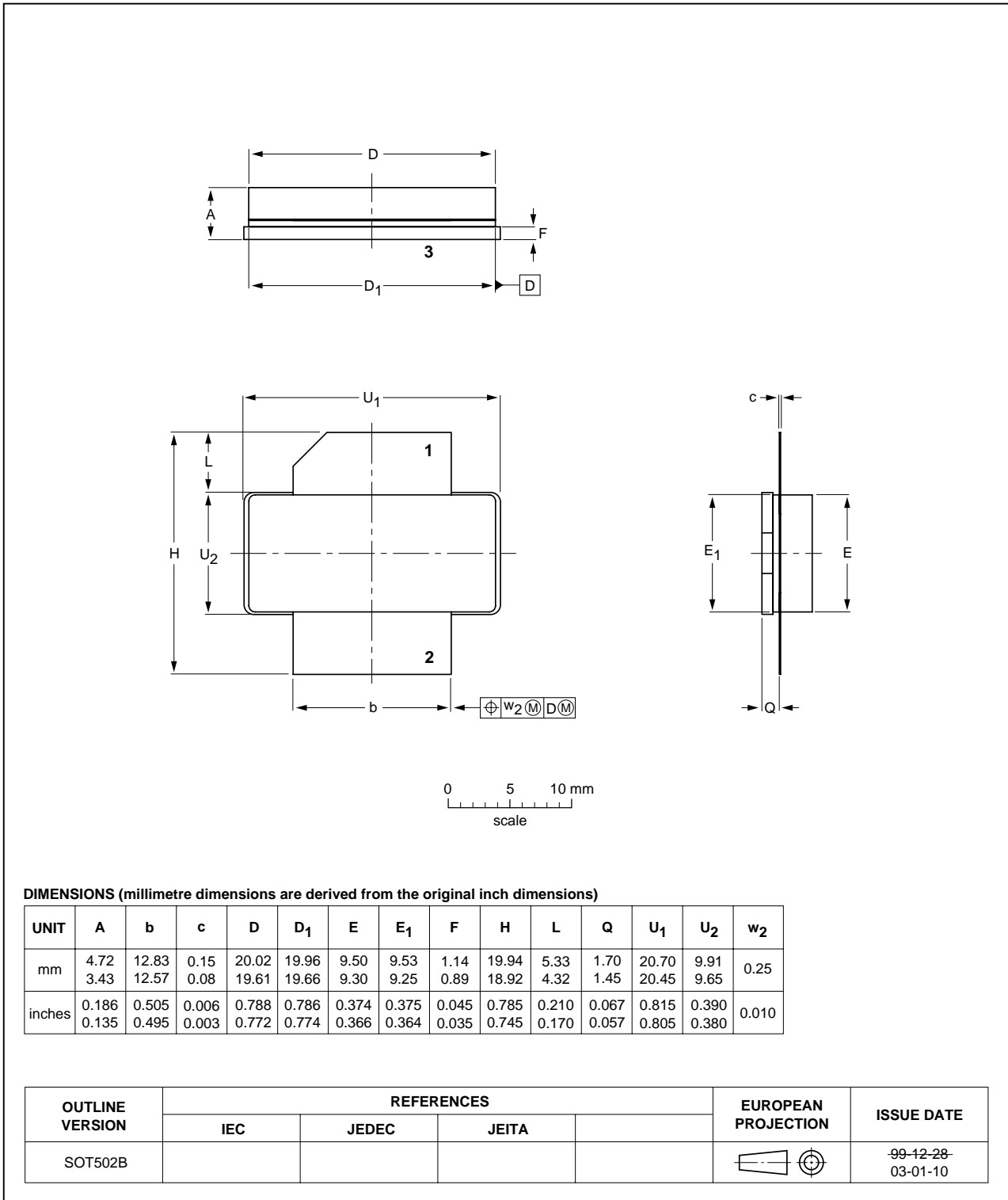


Fig 9. Package outline SOT502B

## 10. Abbreviations

**Table 11: Abbreviations**

Acronym	Description
3GPP	Third Generation Partnership Project
CW	Continuous Wave
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical Channels
$I_{Dq}$	quiescent drain current
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
PEP	Peak Envelope Power
RF	Radio Frequency
TM1	Test Model 1
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

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**Table 12: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BLF4G22-100_4G22 S-100_1	20060110	Product data sheet	-	9397 750 14338	-

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
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Date of release: 10 January 2006  
Document number: 9397 750 14338

Published in The Netherlands