eFuse Evaluation Board Manual

INTRODUCTION

This reference board allows the user to evaluate the SIP32433A, SIP32433B, SIP32434A, and SIP32434B single-channel eFuse load switches. It can also be used for AEC-Q100 qualified versions of these devices, which have part numbers starting with SIPQ instead of SIP.

The SIP32433A, SIP32433B, SIP32434A, and SIP32434B integrate multiple control and protection features, which provide increased controllability and reliability with simplified designs and minimal external components. They protect both power sources and downstream circuitry connected to the switch from overloads, short circuits, voltage surges, and excessive inrush currents.

The output current limit can be set by a single external resistor. V_{IN} overvoltage protection and undervoltage lockout threshold levels can be set with an external resistor network. V_{IN} inrush current requirements can be set with a single external soft start capacitor.

Upon switch-off due to latchable faults, the SIP32433A and SIP32434A will latch the power switch off and the PGD will remain low. The switch can restart by resetting the EN or V_{IN}. The SIP32433B and SIP32434B will auto retry if there is no OTP or OVP fault. The retry delay time is 32 times the soft start time set by the CSS.

Overcurrent, overtemperature, and short circuits are latchable faults, while overvoltage, undervoltage, and reverse current flow are non-latchable faults.

EVALUATION BOARD FEATURES

The SIP32433A, SIP32433B, SIP32434A, and SIP32434B eFuse evaluation board features include:

- 3 V to 23 V operation
- Programmable current limit range. 150 mA to 3.5 A for the SIP32533 and 300 mA to 6 A for the SIP32434
- Programmable soft start output voltage slew rate and auto retry time
- Input path current sense resistor for current probing
- Onboard MOSFET for output short test
- Programmable OVP threshold
- Reverse current blocking (SIP32433x only)

APPLICATIONS

The evaluation board can be used for:

- Servers and data storage
- Routers and switches
- Hot swap and hot plug devices
- Optical modules
- PCIe and memory
- Industrial controls and automation
- TVs and gaming systems

DESCRIPTION

This evaluation fits the evaluation of the eFuse products listed in Table 1.

TABLE 1 - EVALUATION BOARD ORDERING INFORMATION

PART NUMBER	FAULT OFF RESPONSE	$R_{DS(ON)}$ (mΩ)	MAX. I_{LIM} (A)	REVERSE BLOCKING	V_{IN} RANGE (V)	EN / UVLO SET (kΩ)	OVP SET (kΩ)	I_{LIM} SET
SIP32433AEVB	Latch	78	3.5	Yes	3.3 to 23	25 / 4.12	15 / 1	2433A
SIP32433BEVB	Auto-retry	78	3.5	Yes	3.3 to 23	25 /4.12	15 / 1	2433B
SIP32434AEVB	Latch	33	6	No	3.3 to 23	25 /4.12	15 / 1	2434A
SIP32434BEVB	Auto-retry	33	6	No	3.3 to 23	25 /4.12	15 / 1	2434B

Fig. 1 - SIP32433xEVB, SIP32434xEVB Evaluation Board Rev. A

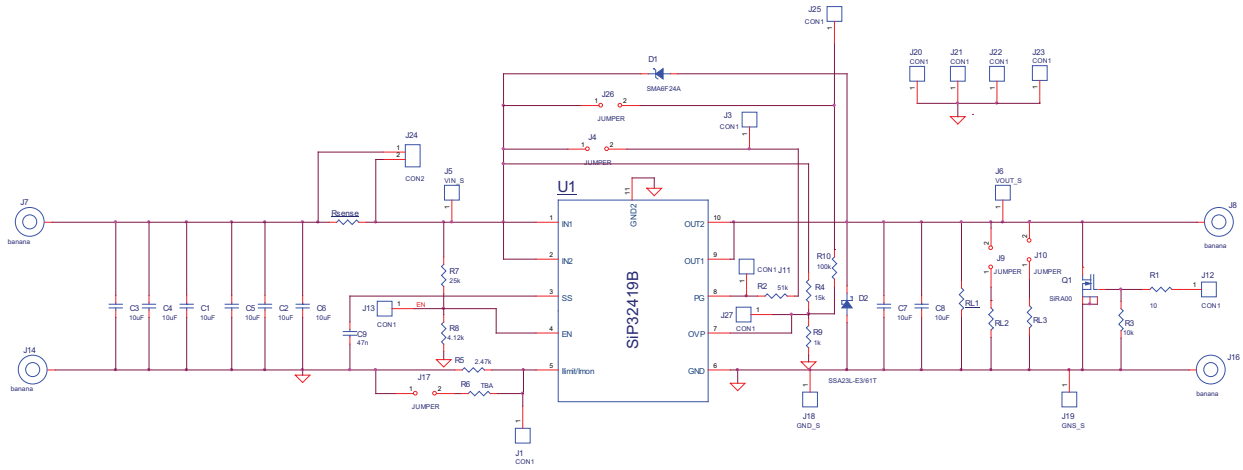

Fig. 2 - SIP3243xxEVB Schematic

SIP3243XXEVB PHYSICAL ACCESS

Table 2 lists the SIP3243xxEVB eFuse evaluation board's switch on / off control, power input, and output connectors. Table 3 lists the test points. Table 4 describes jumpers and the functions to be set. These jumpers are off at the normal board setting.

TABLE 2 - INPUT AND OUTPUT CONNECTOR DESCRIPTION

LABEL	NAME	DESCRIPTION
J13	EN	Active high enable and undervoltage input. Voltage divider resistors are 25 kΩ and 4.12 kΩ
J7	V_{IN}	Power input connector
J14	PGND	Ground connection for the power input
J16	PGND	Ground connection for the power output
J8	V_{OUT}	Power output connector

TABLE 3 - TEST POINTS DESCRIPTION		
LABEL	NAME	DESCRIPTION
J27	OVP	OVP pin probe point
J25	OVP	OVP pin probe through a 100 kΩ resistor
J18	GND	IC ground sense
J12	Gate	High enable gate of MOSFET that shorts the output to GND
J24	I_{SENSE}	Differential sense of input current over a shunt resistor
J6	V_{OUT_S}	Power output sense point
J19	GND	IC ground sense
J3	PG	PG pull-up voltage bias supply
J5	V_{IN_S}	Power input sense point

TABLE 4 - JUMPER DESCRIPTION AND DEFAULT SETTING		
LABEL	NAME	DESCRIPTION
J9	RL2	Connect load resistor
J10	RL3	Connect load resistor
J4	PG	Jumper that connects PG pull-up resistor to V_{IN}
J17	R_{LIM}	Jumper that connects R_6 as a parallel current limit setting resistor to R_5
J26	OVP	Jumper connects R_{10}, OVP voltage divider upper resistor to be paralleled with R_4

POWER INPUT AND OUTPUT TERMINALS

The power header terminals are designed to allow a power supply and load to be connected easily to the evaluation board (see Fig. 1). The input voltage range for this evaluation is from 3.3 V to 23 V.

D_2 is the Schottky diode placed next to the device output to clamp the negative voltage when abruptly switching off an inductive load. A TVS diode can be placed at the input capacitor location in case input transient protection is required.

INPUT AND OUTPUT CAPACITORS

The input capacitors (C_1 to C_6) and output capacitors (C_7, C_8) are mounted close to the device to ensure a stable voltage right before and after the eFuse load switch. The capacitances of these capacitors are 10 µF. The voltage rating for input and output capacitors is 50 V. The SIP32433A, SIP32433B, SIP32434A, and SIP32434B can operate normally up to 23 V. It is important to use capacitors rated at 35 V or higher for the input and output capacitors.

ENABLE AND UNDERVOLTAGE LOCKOUT TERMINAL

The header J13 is directly connected to the EN pin for the enable function of the device. The voltage rating of the EN pin is 28 V. The enable threshold voltage is 1.25 V and the disable threshold voltage is 1.05 V. A user-defined undervoltage protection can be implemented with a voltage divider (Fig. 3)

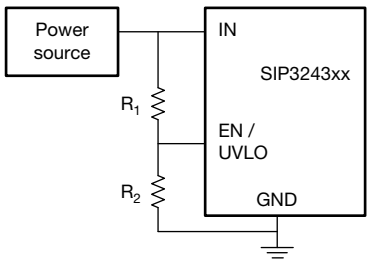

Fig. 3 - Settable Undervoltage Protection With Designs

PG, POWER GOOD OUTPUT

The SIP32433A, SIP32433B, SIP32434A, and SIP32434B devices have power good output to indicate their operation. PG is an open drain output pin. When there is no fault, and V_{OUT} reaches 95 % of V_{IN}, the PG is off. The header J11 is connected to the PG of the device. An external bias voltage can be applied on header J3. The voltage rating of the power good is 28 V maximum. The pull-high resistor connects it to the V_{IN} through the J4 jumper when using the V_{IN} as a PG high bias voltage source.

OVERCURRENT LIMIT SETTING

One of the key features of the devices is they provide overcurrent limit protection. The SIP32433A's and SIP32433B's current limit setting resistor R_{SET} can be calculated by the below formula.

$$R_{SET} = \frac{0.6\ V}{I_{LIM}} \times 10\ 300$$

The SIP32434A's and SIP32434B's RSET follows the formula below:

$$R_{SET} = \frac{0.6\ V}{I_{LIM}} \times 20\ 600$$

- R_{SET} is paralleled R_5 and R_6 on the board
- I_{LIM} is the target current limit setting

PROGRAMMABLE SOFT POWER UP

During soft start, the devices control the output voltage to follow the voltage ramp on the SS pin.

$$V_{OUT} = \frac{I_{INRUSH}\ (mA)}{C_{OUT}\ (\mu F)}$$

The output slew rate and its set capacitor, C_{SS}, can be calculated by the following formulas:

$$C_{SS} = \frac{I_{SS} \times 9}{SR}$$

Where:

- t_{SS} is the soft power up time
- I_{SS} is the built-in current to charge up the C_{SS}; the value is 4.5 µA
- C_{SS} is the soft power setting capacitor shown as C_9 on the board
- R_{SET} is the current limit resistor

HOT-PLUG TEST

Connect J3 to an external 5 V power source as the PG bias source.

Hot-plug the power supply between J7 and J14.

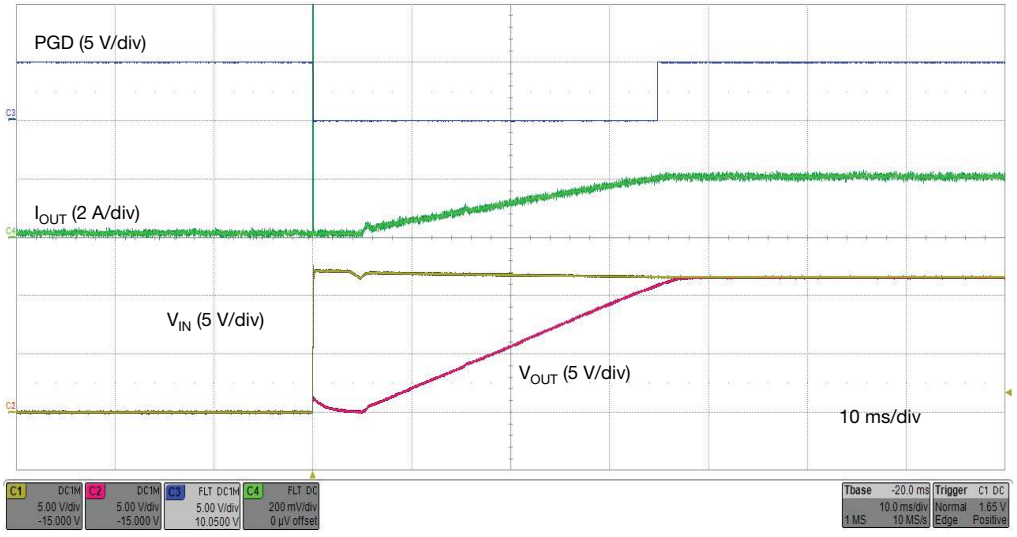

Fig. 4 - An Example of Inrush Current Captured on the SIP32433 Series eFuse Evaluation Board

CURRENT LIMIT TEST

Connect and turn on the power supply.

Slowly increase the load current. The switch turns off after 6 ms at the set current limit clamping level.

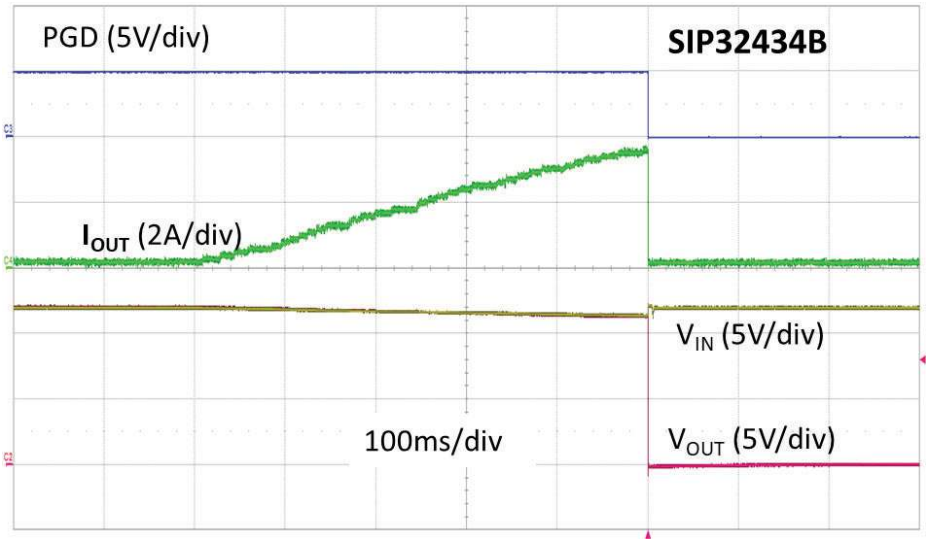

Fig. 5 - An Example of Overcurrent Protection Captured on the SIP32434 eFuse Evaluation Board

OUTPUT SHORT TEST

Short the output through the on-board MOSFET by pulling J12 high.

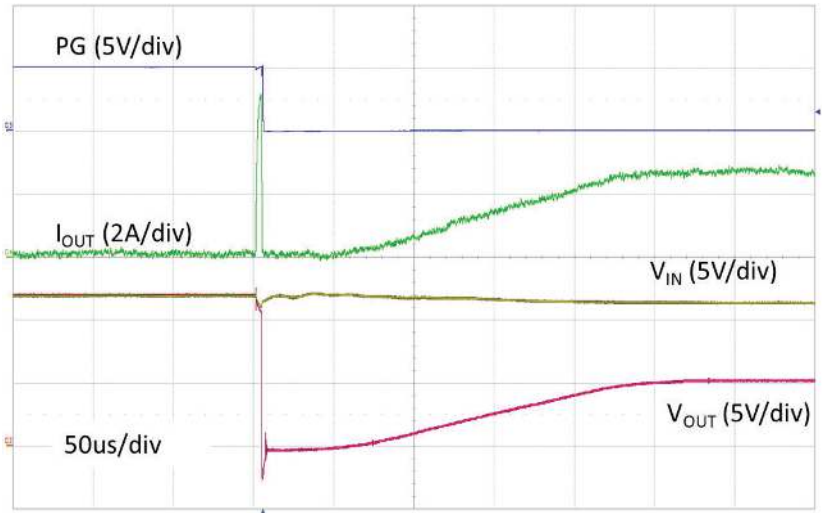

Fig. 6 - An Example of Output Short Protection Captured on the SIP32433 eFuse Evaluation Board

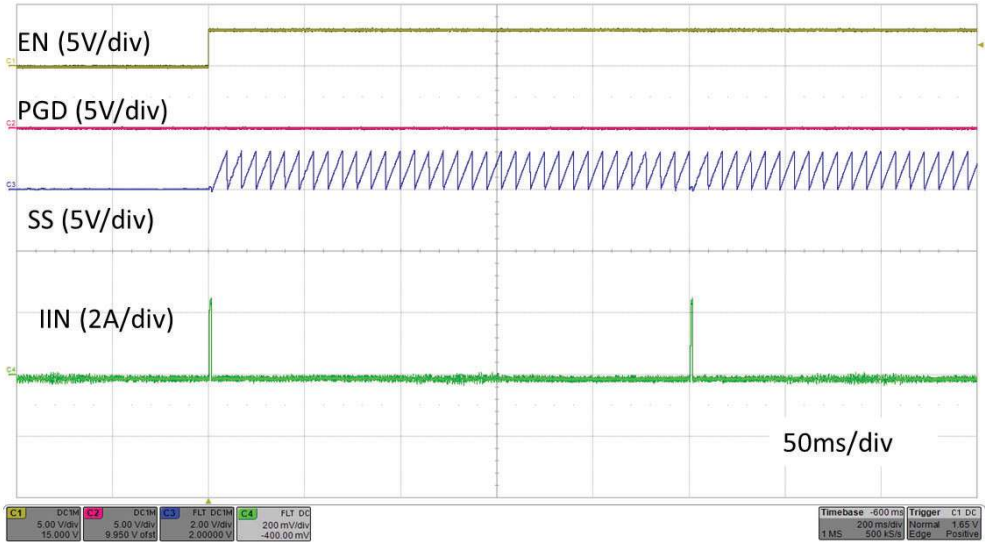

Fig. 7 - An Example of Auto Retry Into an Output Short Condition

EVALUATION BOARD LAYOUT AND PROPOSED LAYOUT GUIDELINES

Fig. 8 to Fig. 11 show component placement and PCB layouts.

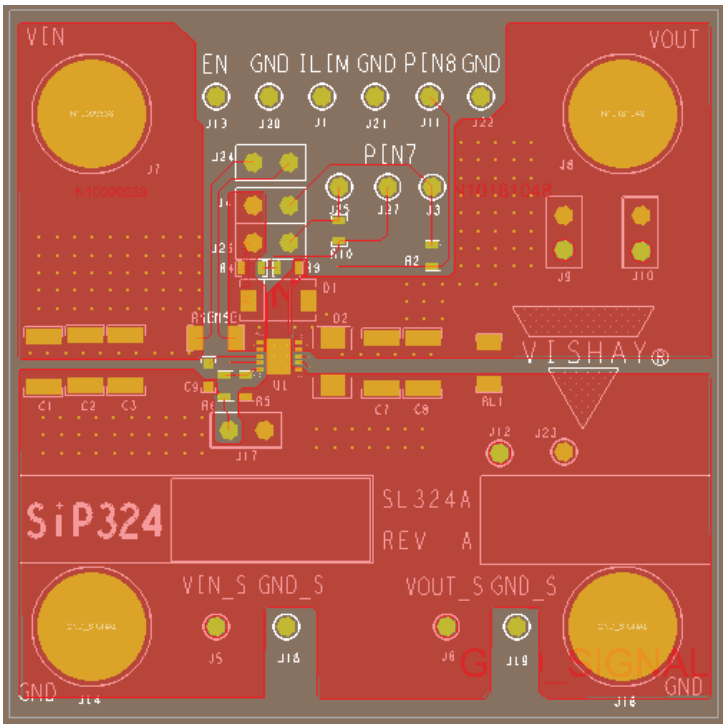

Fig. 8 - SIP3243xxEVB Board Top Layer

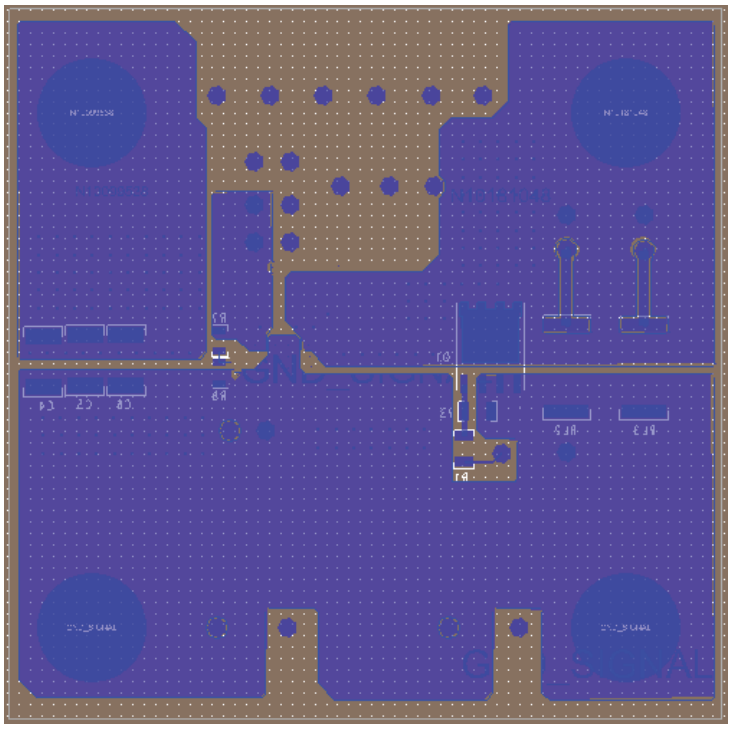

Fig. 9 - SIP3243xxEVB Board Bottom Layer

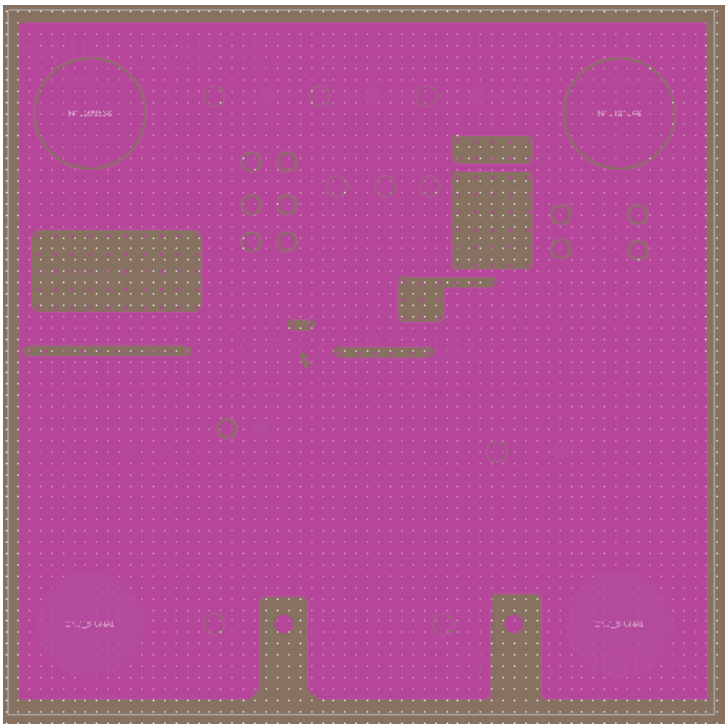

Fig. 10 - SIP3243xxEVB Board Inner 1 Layer

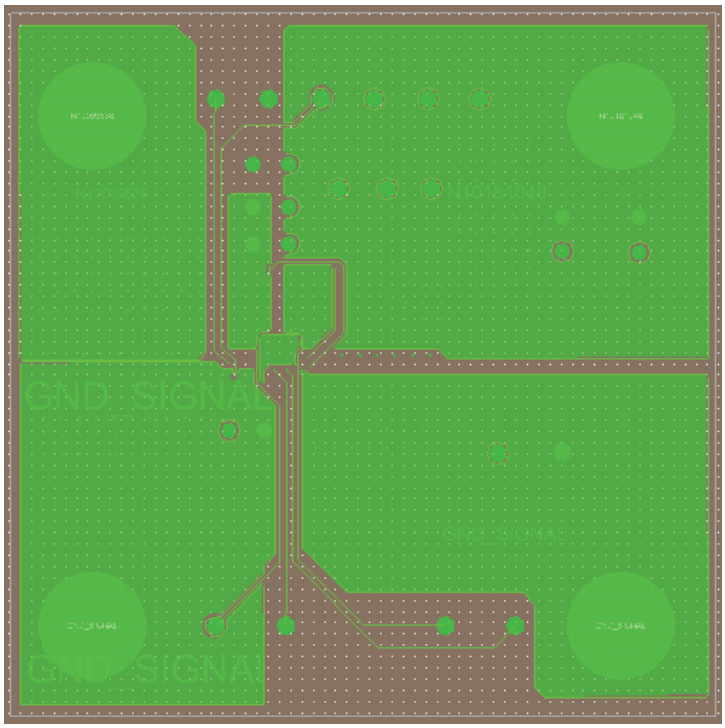

Fig. 11 - SIP3243xxEVB Board Inner 2 Layer

BILL OF MATERIALS

Table 3 lists the evaluation board bill of materials (BOM).

TABLE 3 - SIP3243XXEVB BILL OF MATERIALS

SYM. NAME	COMP. VALUE	QUANTITY	REFDES	MANUFACTURE PART NUMBER
BANANA	Banana	4	J7; J8; J14; J16	36-575-4-ND
C0603-TDK	47 nF	1	C9	399-17881-2-ND
C1210-TDK	10 uF, 50 V	8	C1; C2; C3; C4; C5; C6; C7; C8	445-14933-2-ND
DO-214	SSA23L	1	D2	SSA23L-E3/61TGITR-ND
DO-221AC	SMA6F24A	1	D1	DNP
JUMPER2	JUMPER	5	J4; J9; J10; J17; J26	TSW-102-07-L-S
JUMPER2	CON2	1	J24	TSW-102-07-L-S
MLP33-11A	IC	1	U1	SIP3243xx
MOSPOWERPAKSO8	SiRA00	1	Q1	SIRA00DP-T1-GE3TR-ND
R0603-VISHAY	51 kΩ	1	R2	541-5465-2-ND
R0603-VISHAY	DNP	1	R4	DNP
R0603-VISHAY	DNP	1	R8	DNP
R0603-VISHAY	12.4 kΩ	1	R5	A140147TR-ND
R0603-VISHAY	2.05 kΩ	1	R6	A140445TR-ND
R0603-VISHAY	DNP	1	R7	DNP
R0603-VISHAY	1 kΩ	1	R9	541-1.00KHTR-ND
R0603-VISHAY	DNP	1	R10	DNP
R0805-VISHAY	10 Ω	1	R1	CRCW080510R0FKEB
R0805-VISHAY	100 kΩ	1	R3	541-3950-2-ND
R1206-VISHAY	DNP	1	RL1	DNP
R1206-VISHAY	25 mΩ	1	R_{SENSE}	CSR1206FK25L0TR-ND
R2512-VISHAY	DNP	2	RL2; RL3	DNP
TP30	CON1	11	J1; J3; J11; J12; J13; J20; J21; J22; J23; J25; J27	36-5002-ND
TP30	V_{IN_S}	1	J5	
TP30	V_{OUT_S}	1	J6	
TP30	GND_S	1	J18	
TP30	GNS_S	1	J19	

LAYOUT GUIDELINES

The SIP32434A and SIP32434B are protection switches designed to maintain a constant output load current upon overcurrent faults. An optimized layout with efficient heat sinking is critical. It is recommended to put as much copper as possible on the devices' central exposed pad, which is connected to ground. Connect all ground planes with all possible thermal VIAs. The circuit setting components should be laid close to their connection pins. The components include a current limit setting resistor, soft start setting capacitor, and resistors connected to EN / UVLO and OVP pins.

Protection devices such as an input TVS or output Schottky diode must be located close to the pins to be protected, and routed with short traces to reduce inductance.

Below is a layout example.

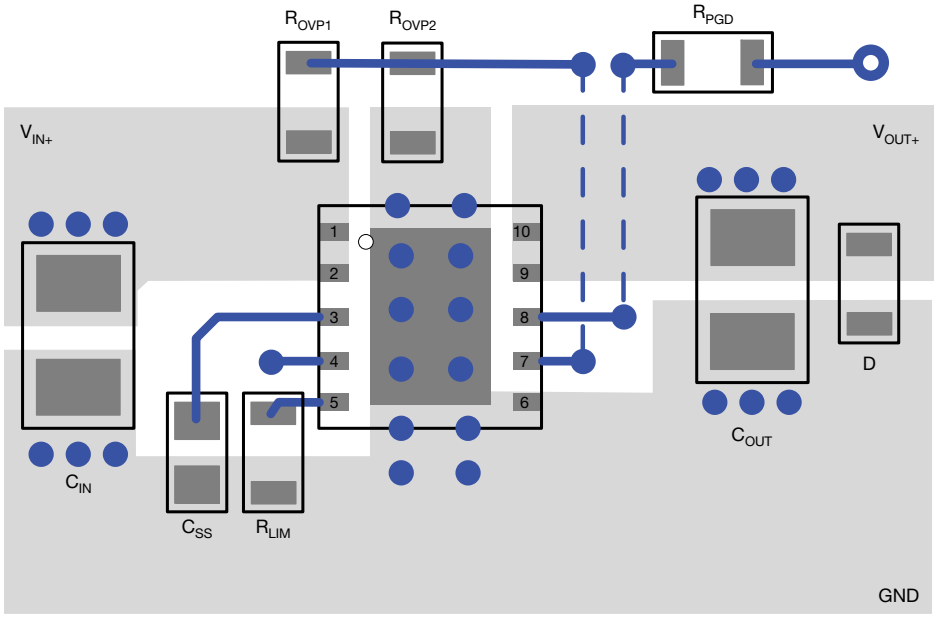

Fig. 12