Product Specification

PE45450

UltraCMOS® Power Limiter
9 kHz–6 GHz

Features

- Monolithic drop-in solution with no external bias components reducing design complexity
- Adjustable power limiting threshold from +25 dBm to +35 dBm
- Max power handling
  - +40 dBm CW (10W)
  - +47 dBm Pulsed (50W)
- Superior ESD rating and ESD protection
  - 8 kV HBM on all pins
  - 1 kV CDM on all pins
  - 600V MM on all pins
- Unbiased power limiting operation
- Fast response and recovery time of 1 ns
- Dual mode operation
  - Power limiting mode
  - Power reflecting mode

Product Description

The PE45450 is a HaRP™ technology-enhanced power limiter designed for use in high performance power limiting applications in test and measurement equipment, radar, military electronic counter measure receivers and wireless infrastructure transceivers and antennas.

Unlike traditional PIN diode solutions, the PE45450 achieves an adjustable input 1 dB compression point or limiting threshold via a low current control voltage (V_{CTRL}), eliminating the need for external bias components, such as DC blocking capacitors, RF choke inductors, and bias resistors.

It delivers low insertion loss and high linearity under non-limiting input power levels and extremely fast response and recovery time in a limiting event. It also offers superior ESD rating and ESD protection for subsequent circuitry.

The PE45450 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

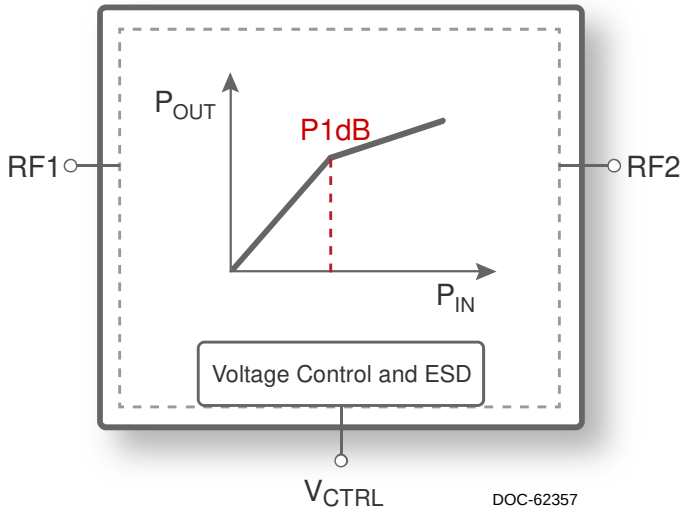


Figure 2. Package Type
12-lead 3x3 mm QFN

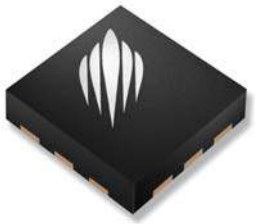
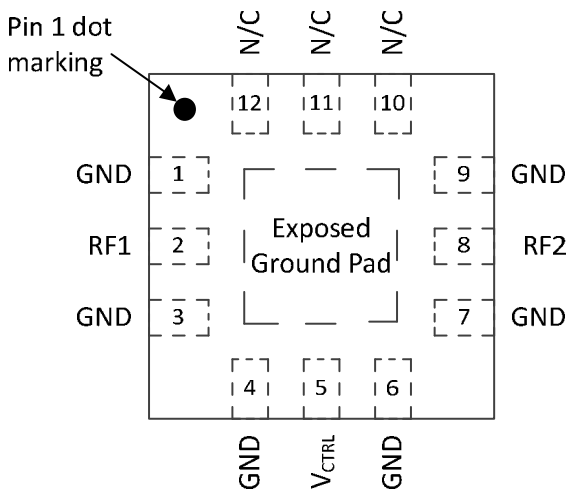


Table 1. Electrical Specifications @ +25°C (Z_S = Z_L = 50Ω), unless otherwise noted

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		9 kHz		6 GHz	As shown
Power limiting mode					
Insertion loss[1]	9 kHz–3 GHz 3–6 GHz		0.45 0.80	0.70 1.05	dB dB
Return loss[1]	9 kHz–3 GHz 3–6 GHz		13 17		dB dB
P1dB / limiting threshold	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –1.5V @ 915 MHz V_{CTRL} = –0.5V @ 915 MHz		35 32 25		dBm dBm dBm
Leakage power[2]	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –1.5V @ 915 MHz V_{CTRL} = –0.5V @ 915 MHz		33.5 33 31.5	35.5 35 33.5	dBm dBm dBm
Leakage power slope	V_{CTRL} = –1.0V @ 915 MHz		0.4		dB/dB
Unbiased leakage power[2]	V_{CTRL} = 0V @ 915 MHz		25	27	dBm
Input IP2	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –2.5V @ 6 GHz		115 110		dBm dBm
Input IP3	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –2.5V @ 6 GHz		70 60		dBm dBm
Response / recovery time	1 GHz		1		ns
Power reflecting mode[3]					
Leakage power[2]	V_{CTRL} = +2.5V @ 915 MHz		2	8	dBm
Switching time[4]	State change to 10% RF		400		µs

Notes: 1. External matching is required to achieve the performance.
2. Measured with +40 dBm CW applied at input.
3. This mode requires the control voltage to toggle between +2.5V and –2.5V. At +2.5V, the limiter equivalent circuit is a low impedance to ground, reflecting most of the incident power back to the source.
4. State change is V_{CTRL} toggle from –2.5V to +2.5V.

Figure 3. Pin Configuration (Top View)*



Note: * Pins 10–12 can be ground if deemed necessary by the customer.

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1, 3, 4, 6, 7, 9	GND	Ground
2	RF1*	RF port 1
5	V_{CTRL}	Control voltage
8	RF2*	RF port 2
10–12	N/C	No connect
Pad	GND	Exposed pad: Ground for proper operation

Note: * RF pins 2 and 8 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE45450 in the 12-lead 3x3 mm QFN package is MSL1.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Control voltage Power limiting mode Power reflecting mode	V_{CTRL}	 –2.5 –2.5		 –0.5 +2.5	 V V
RF input power, CW[1]	$P_{MAX,CW}$			40	dBm
RF input power, pulsed[2]	$P_{MAX,PULSED}$			47	dBm
RF input power, unbiased[2,3]	$P_{MAX,UNB}$			47	dBm
Operating temperature range	T_{OP}	–55	+25	+85	°C
Operating junction temperature[1]	T_J			+290	°C

Notes: 1. CW, 100% duty cycle, in 10 min, 50Ω
2. Pulsed, 0.1% duty cycle of 1 µs pulse width in 10 min, 50Ω
3. V_{CTRL} = 0V or V_{CTRL} pin left not connected

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Control voltage Power limiting mode Power reflecting mode	V_{CTRL}	–3.3	3.6	V
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM[1], all pins	$V_{ESD,HBM}$		8000	V
ESD voltage MM[2], all pins	$V_{ESD,MM}$		600	V
ESD voltage CDM[3], all pins	$V_{ESD,CDM}$		1000	V

Notes: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)
2. Machine Model (JEDEC JESD22-A115)
3. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

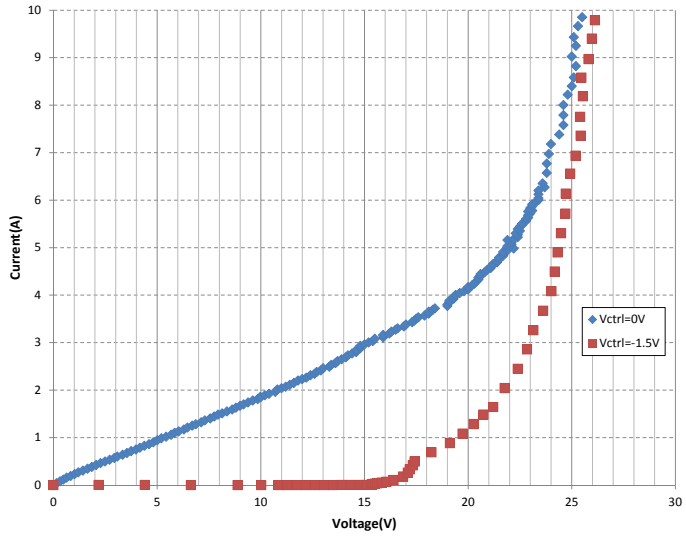
ESD Protection Capability

The PE45450 can be used as an ESD protection device to protect sensitive circuit elements against ESD surges. Besides superior ESD rating of 8 kV HBM, the PE45450 has excellent voltage clamping capability. During an ESD event, the PE45450 maintains very low voltage across the device to ensure that the circuit element it is protecting survives.

Table 5. Transmission Line Pulse Data vs. HBM

V_{CTRL}	HBM (V)	Max Current (A)	Voltage (V)
0	1000	0.7	3.7
–1.5	1000	0.7	18
0	2000	1.3	7
–1.5	2000	1.3	20
0	3000	2.0	10.8
–1.5	3000	2.0	21.5

Figure 4. Transmission Line Pulse Curve



Dual Mode Operation

Power Limiting Mode

The PE45450 performs as a linear power limiter with adjustable P1dB / limiting threshold. The P1dB / limiting threshold can be adjusted by changing the control voltage between –2.5V and –0.5V. If unbiased, or if V_{CTRL} = 0V, the PE45450 still offers power limiting protection.

Power Reflecting Mode

Power reflecting mode requires a power detector to sample the RF input power and a microcontroller to toggle the limiter control voltage between +2.5V and –2.5V based on the system protection requirements. At +2.5V, the limiter impedance to ground is less than 1Ω and most of the incident power will be reflected back to the source. At –2.5V, the device operates as in power limiting mode.

Thermal Data

When limiting high power RF signals, the junction temperature of the power limiter can rise significantly.

Special consideration needs to be made in the design of the PCB to properly dissipate the heat away from the part and maintain the 290°C peak junction temperature.

It is recommended to use best design practices for high power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Special care also needs to be made to alleviate solder voiding under the part.

Table 6. Theta JC

Parameter	Min	Typ	Max	Unit
Theta JC		20		°C/W

Typical Performance Data @ +25°C, 915 MHz ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 5. Insertion Loss vs. Temperature

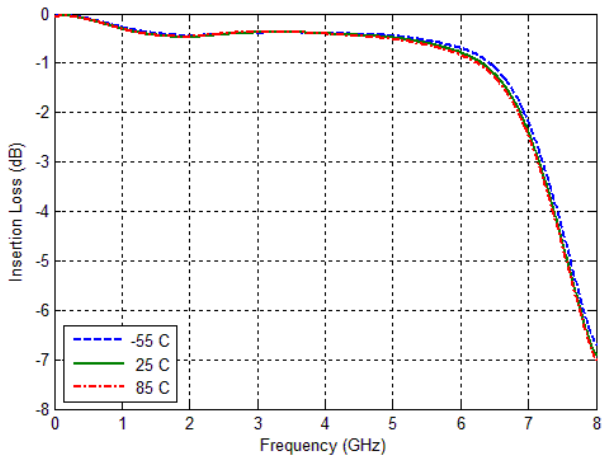


Figure 6. Input Return Loss vs. Temperature

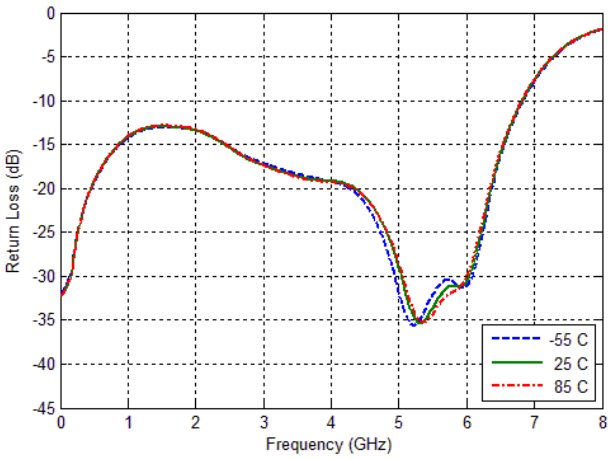
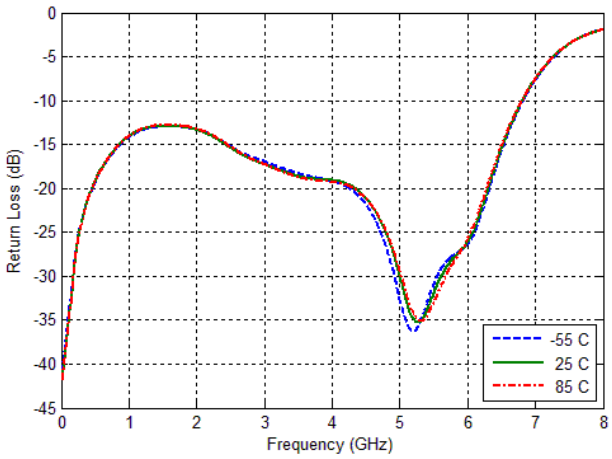


Figure 7. Output Return Loss vs. Temperature



Typical Performance Data @ +25°C, 915 MHz ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 8. P_{OUT} vs. P_{IN} Over V_{CTRL}

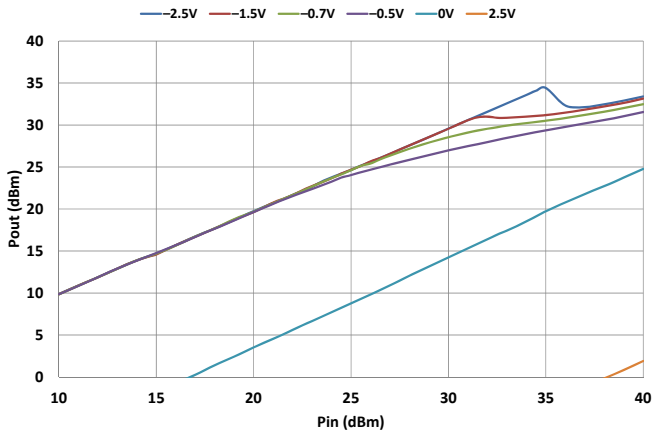


Figure 9. P_{OUT} vs. P_{IN} Over Frequency @ V_{CTRL} = –0.7V

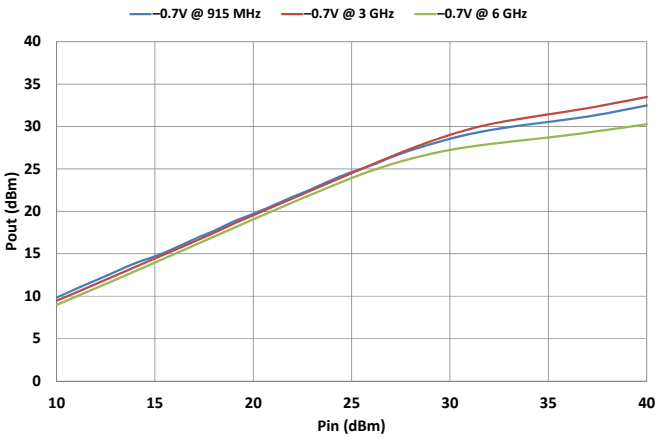


Figure 10. P1dB vs. V_{CTRL} Over Temperature

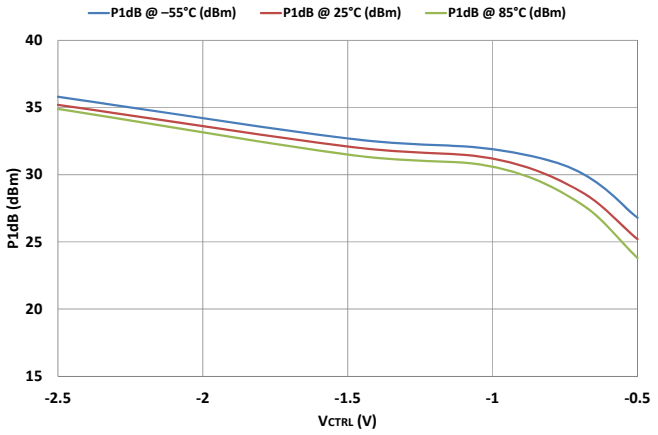
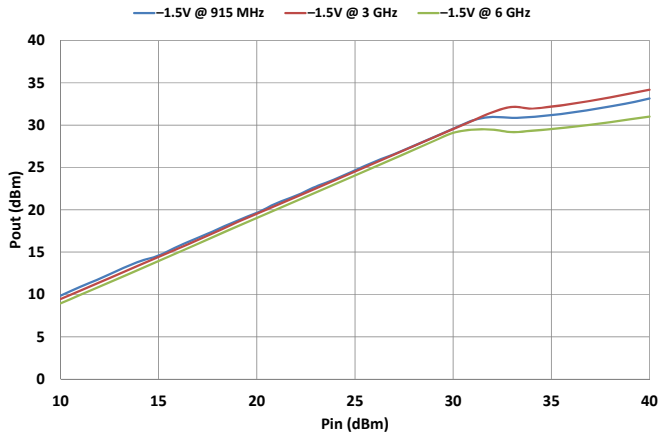


Figure 11. P_{OUT} vs. P_{IN} Over Frequency @ V_{CTRL} = –1.5V



Typical Performance Data @ +25°C, 915 MHz ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Figure 12. IIP3 / IIP2 vs. V_{CTRL} Over Temperature

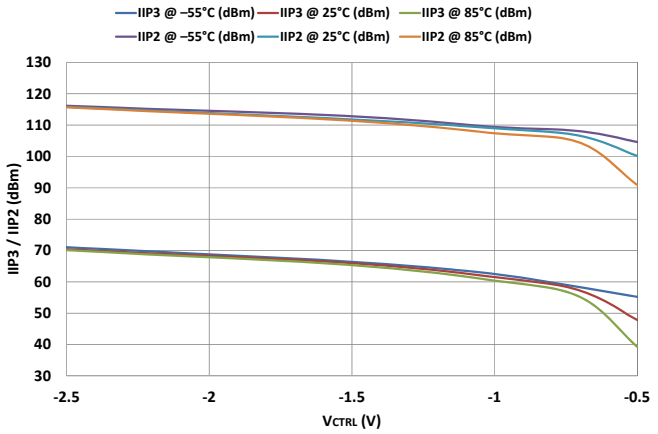


Figure 13. IIP3 / IIP2 vs. P_{IN} Over V_{CTRL}

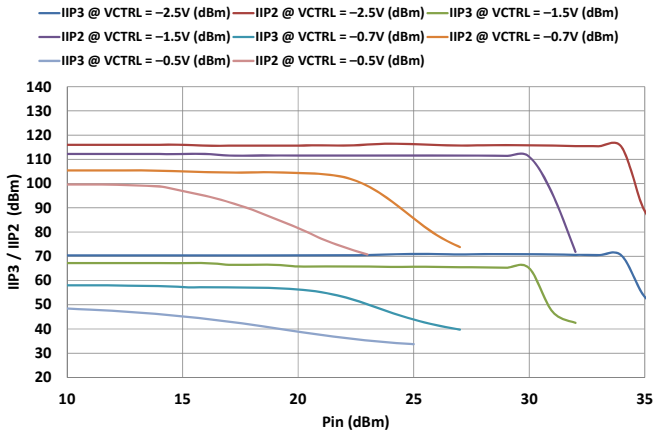


Figure 14. Leakage Power @ P_{MAX} vs. V_{CTRL} Over Temperature

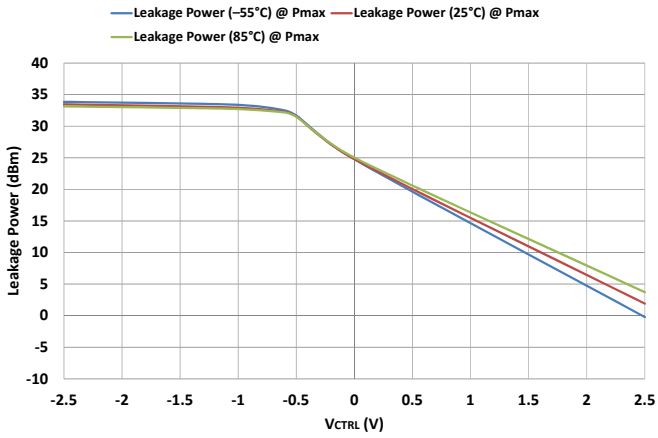
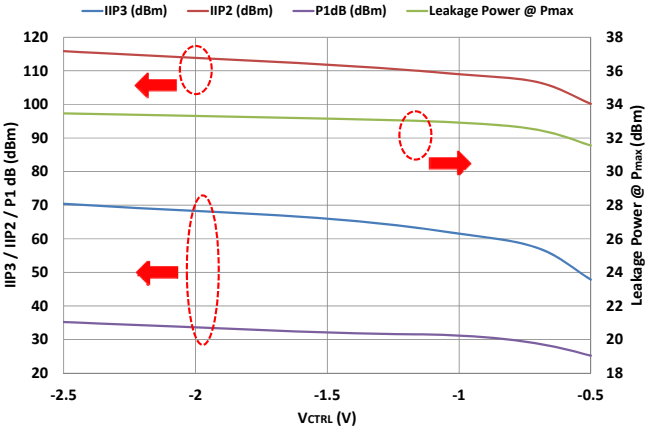


Figure 15. P1dB, IIP3, IIP2, Leakage Power @ P_{MAX} vs. V_{CTRL}

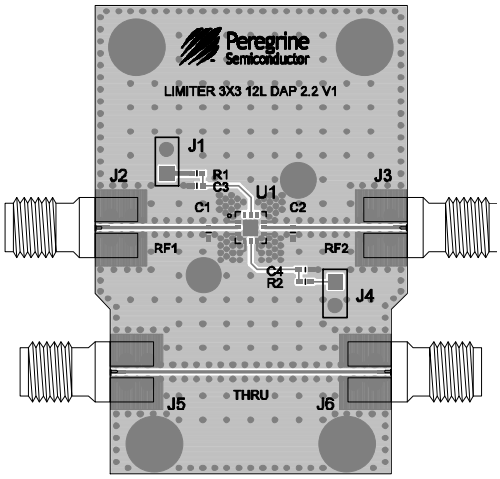


Evaluation Kit

The power limiter EVK board was designed to ease customer evaluation of Peregrine's PE45450. The bi-directional RF input and output are connected to RF1 and RF2 port through a 50Ω transmission line via SMA connectors J2 and J3. A through 50Ω transmission line is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. The 2-pin connector J4 is connected to the external bias V_{CTRL}.

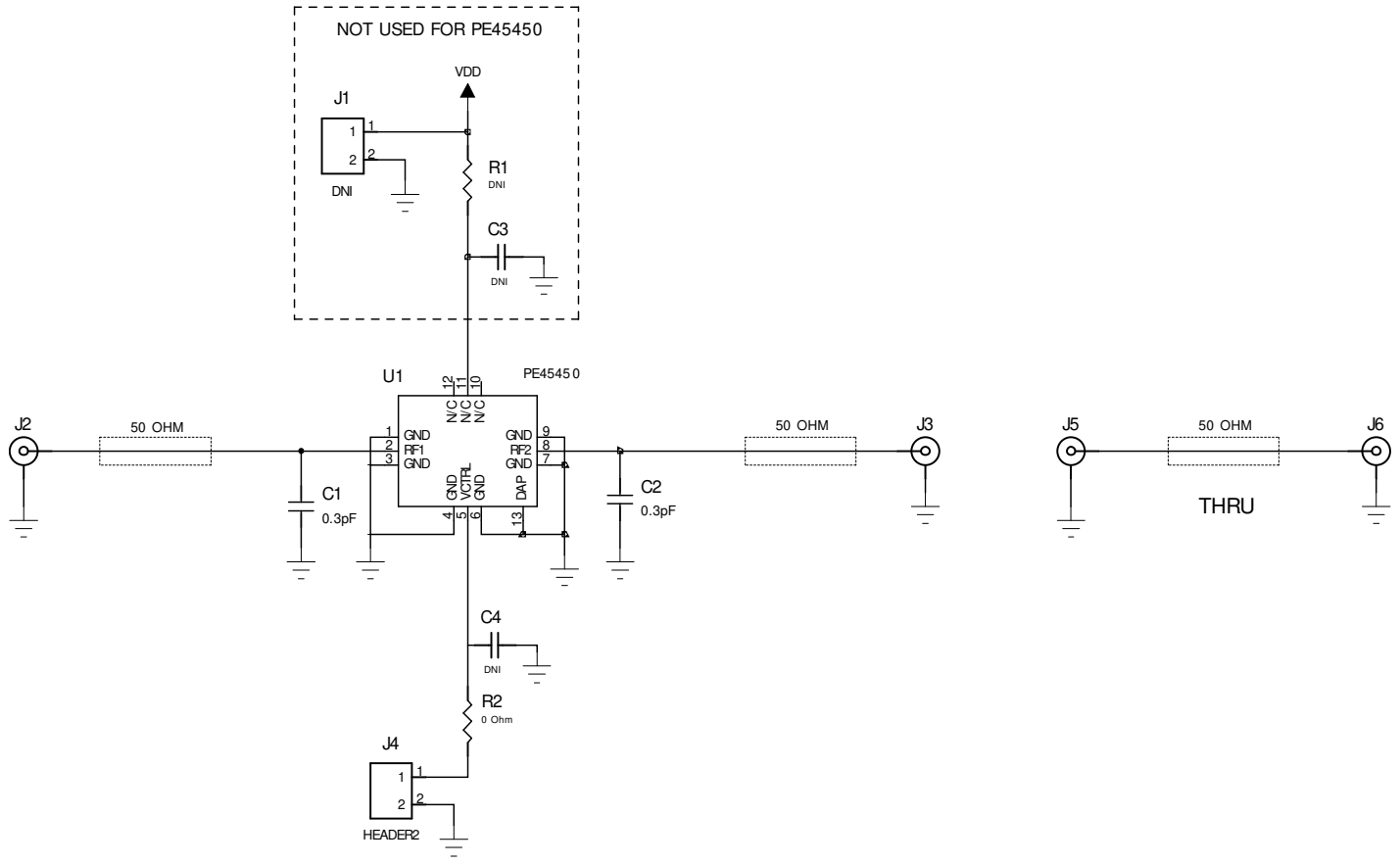
The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers RO4350B material with a 6.6 mil RF core and Er = 3.66. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 13.5 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

Figure 16. Evaluation Board Layout



PRT-51452

Figure 17. Evaluation Board Schematic



Caution: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

DOC-44327

Figure 18. Package Drawing

12-lead 3x3 mm QFN

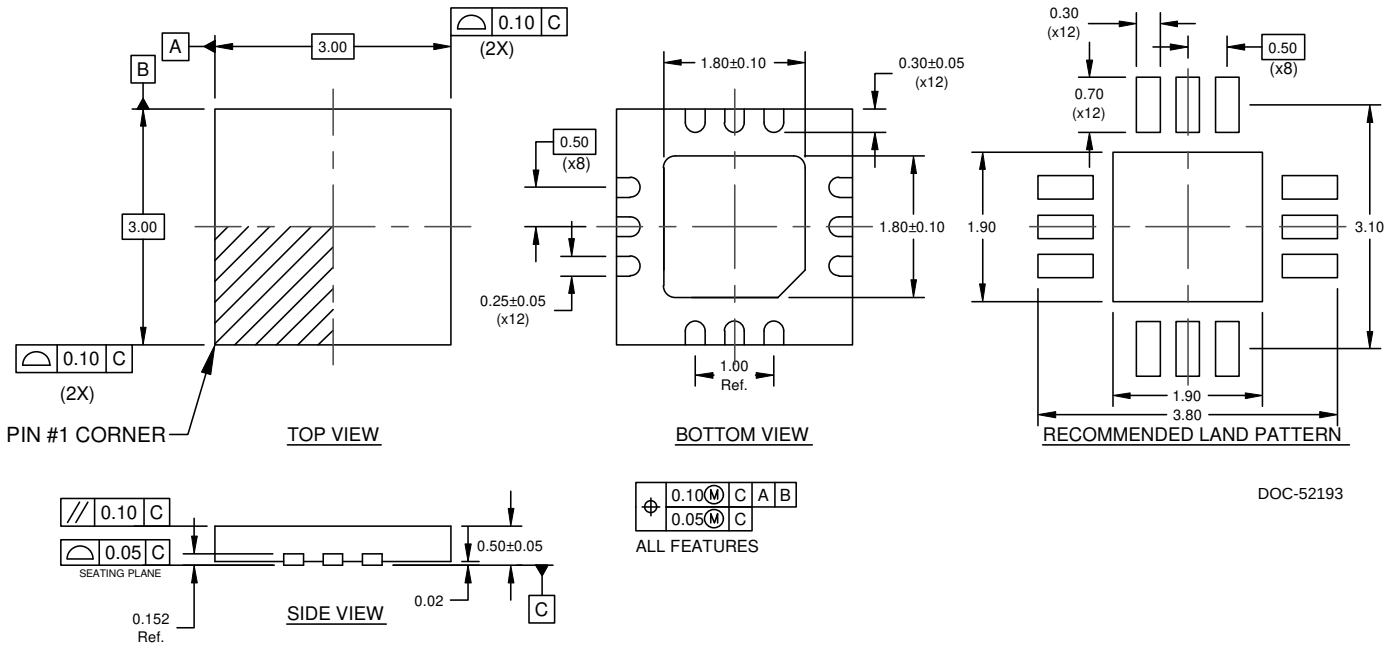


Figure 19. Top Marking Specifications

DOC-51207

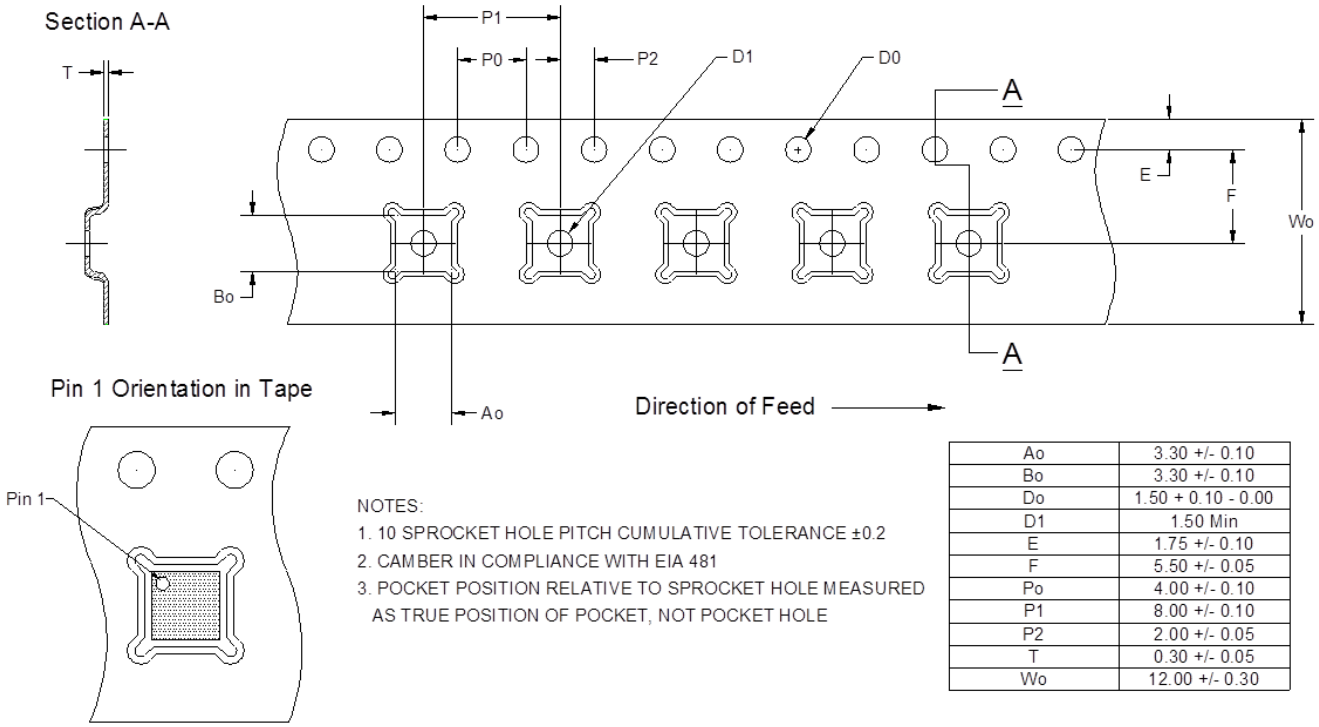
● = Pin 1 designator

45450 = Five digit part number

YYWW = Date Code, last two digits of the year and work week

ZZZZZZ = Maximum six characters of the assembly lot code

Figure 20. Tape and Reel Drawing



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Ao	3.30 +/- 0.10
Bo	3.30 +/- 0.10
Do	1.50 + 0.10 - 0.00
D1	1.50 Min
E	1.75 +/- 0.10
F	5.50 +/- 0.05
Po	4.00 +/- 0.10
P1	8.00 +/- 0.10
P2	2.00 +/- 0.05
T	0.30 +/- 0.05
Wo	12.00 +/- 0.30

Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
PE45450A-X	PE45450 Power limiter	Green 12-lead 3x3 mm QFN	500 units / T&R
EK45450-02	PE45450 Evaluation kit	Evaluation kit	1 / box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. ***Preliminary Specification:*** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).
The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com.