

MC10E416, MC100E416

5V ECL Quint Differential Line Receiver

Description

The MC10E416/100E416 is a 5-bit differential line receiving device. The 2.0 GHz of bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below V_{CC} .

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

Features

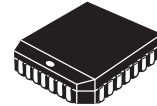
- Differential D and Q; V_{BB} available
 - 600 ps Max. Propagation Delay
 - High Frequency Outputs
 - 2 Stages of Gain
 - PECL Mode Operating Range: $V_{CC} = 4.2$ V to 5.7 V with $V_{EE} = 0$ V
 - NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -4.2$ V to -5.7 V
 - Internal Input 50 k Ω Pulldown Resistors
 - ESD Protection: Human Body Model; > 2 kV, Machine Model; > 200 V
 - Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
 - Moisture Sensitivity Level:
 - Pb = 1;
 - Pb-Free = 3
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
 - Transistor Count = 201 devices
 - Pb-Free Packages are Available*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



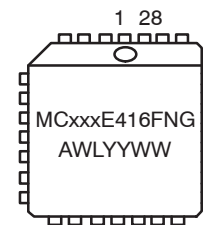
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PLCC-28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



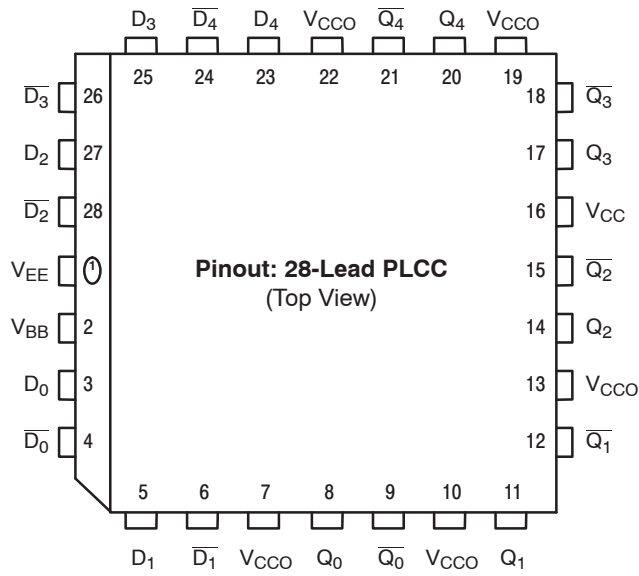
| | |
|-----|---------------------|
| xxx | = 10 or 100 |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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* All V_{CC} and V_{CCO} pins are tied together on the die.
Warning: All V_{CC} , V_{CCO} , and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 28-Lead Pinout Assignment

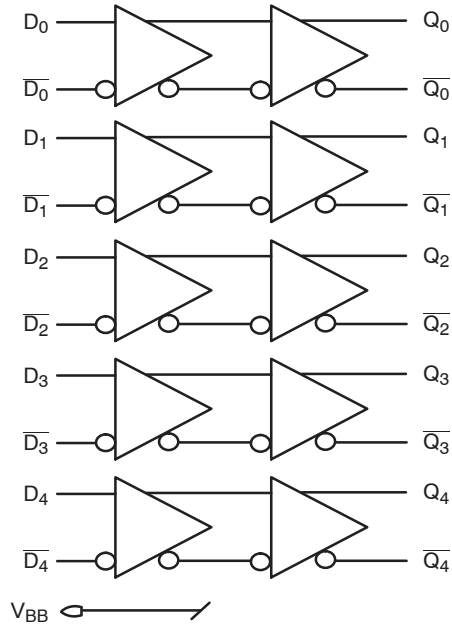


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|------------------------------|-------------------------------|
| D[0:4], \overline{D} [0:4] | ECL Differential Data Inputs |
| Q[0:4], \overline{Q} [0:4] | ECL Differential Data Outputs |
| V_{BB} | Reference Voltage Output |
| V_{CC} , V_{CCO} | Positive Supply |
| V_{EE} | Negative Supply |

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Table 2. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|-----------------------|-------------------|-------------|-----------------------------|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 8 | V |
| V_I | PECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ | $V_I \leq V_{CC}$ | 6 | V |
| | NECL Mode Input Voltage | $V_{CC} = 0\text{ V}$ | $V_I \geq V_{EE}$ | -6 | V |
| I_{out} | Output Current | Continuous Surge | | 50 | mA |
| | | | | 100 | mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | 0 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | PLCC-28 | 63.5 | $^{\circ}\text{C}/\text{W}$ |
| | | 500 lfpm | PLCC-28 | 43.5 | $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | PLCC-28 | 22 to 26 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder | Pb Pb-Free | | 265 | $^{\circ}\text{C}$ |
| | | | | 265 | $^{\circ}\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 3. 10E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$, $V_{EE} = 0.0\text{ V}$ (Note 1)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 135 | 162 | | 135 | 162 | | 135 | 162 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 3980 | 4070 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.73 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.7 | | 5.0 | 2.7 | | 5.0 | 2.7 | | 5.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 4. 10E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 4)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 135 | 162 | | 135 | 162 | | 135 | 162 | mA |
| V_{OH} | Output HIGH Voltage (Note 5) | -1020 | -930 | -840 | -980 | -895 | -810 | -910 | -815 | -720 | mV |
| V_{OL} | Output LOW Voltage (Note 5) | -1950 | -1790 | -1630 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1170 | -1005 | -840 | -1130 | -970 | -810 | -1060 | -890 | -720 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1950 | -1715 | -1480 | -1950 | -1715 | -1480 | -1950 | -1698 | -1445 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.27 | -1.35 | | -1.25 | -1.31 | | -1.19 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) | -2.3 | | 0.0 | -2.3 | | 0.0 | -2.3 | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.065 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
5. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
6. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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Table 5. 100E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 7)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 135 | 162 | | 135 | 162 | | 155 | 186 | mA |
| V_{OH} | Output HIGH Voltage (Note 8) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| V_{OL} | Output LOW Voltage (Note 8) | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 2.7 | | 5.0 | 2.7 | | 5.0 | 2.7 | | 5.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

8. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

9. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 6. 100E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 10)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 135 | 162 | | 135 | 162 | | 155 | 186 | mA |
| V_{OH} | Output HIGH Voltage (Note 11) | -1025 | -950 | -880 | -1025 | -950 | -880 | -1025 | -950 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 11) | -1810 | -1705 | -1620 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | -1025 | -880 | -1165 | -1025 | -880 | -1165 | -1025 | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12) | -2.3 | | 0.0 | -2.3 | | 0.0 | -2.3 | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

11. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

12. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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Table 7. AC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 13)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|---|-----|----------|------|------|----------|------|------|----------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{MAX} | Maximum Toggle Frequency | | | | | > 2.0 | | | | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output | | | | | | | | | | ps |
| | d(Diff) | 250 | 350 | 500 | 250 | 350 | 500 | 250 | 350 | 500 | |
| | D(SE) | 200 | 350 | 550 | 200 | 350 | 550 | 200 | 350 | 550 | |
| t_{SKEW} | Within-Device Skew (Note 14) | | 50 | | | 50 | | | 50 | | ps |
| t_{SKEW} | Duty Cycle Skew (Note 15) $t_{PLH}-t_{PHL}$ | | ± 10 | | | ± 10 | | | ± 10 | | ps |
| t_{JITTER} | Random Clock Jitter (RMS) | | < 1 | | | < 1 | | | < 1 | | ps |
| $V_{PP(AC)}$ | Input Voltage Swing (Differential Configuration) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t_r t_f | Rise/Fall Time (20 - 80%) | 100 | 200 | 350 | 100 | 200 | 350 | 100 | 200 | 350 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. 10 Series: V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.

100 Series: V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

14. Within-device skew is defined as identical transitions on similar paths through a device.

15. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

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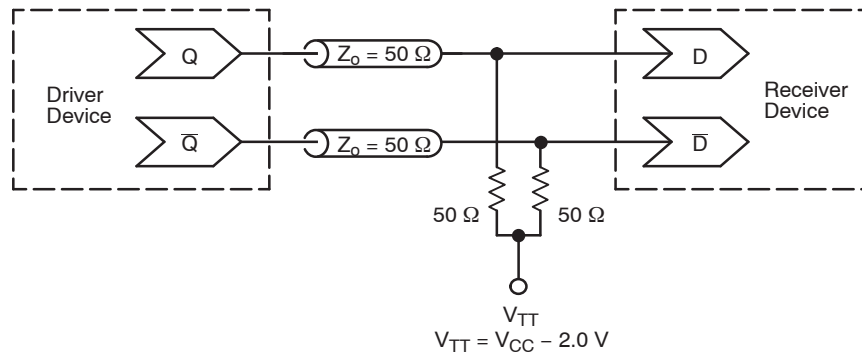


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|----------------------|-----------------------|
| MC10E416FN | PLCC-28 | 37 Units / Rail |
| MC10E416FNG | PLCC-28 (Pb-Free) | 37 Units / Rail |
| MC10E416FNR2 | PLCC-28 | 500 / Tape & Reel |
| MC10E416FNR2G | PLCC-28 (Pb-Free) | 500 / Tape & Reel |
| MC100E416FN | PLCC-28 | 37 Units / Rail |
| MC100E416FNG | PLCC-28 (Pb-Free) | 37 Units / Rail |
| MC100E416FNR2 | PLCC-28 | 500 / Tape & Reel |
| MC100E416FNR2G | PLCC-28 (Pb-Free) | 500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

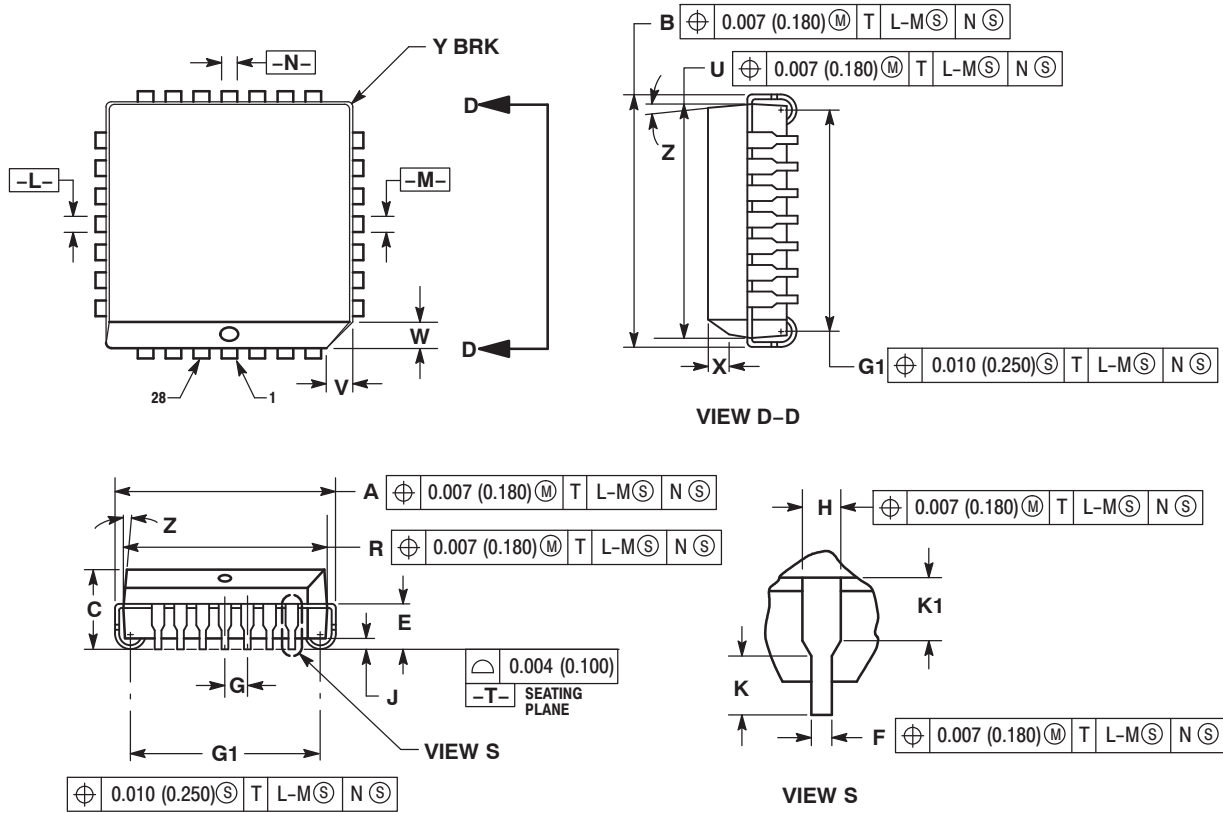
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E




NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE BOTTOM MAY BE SMALLER THAN THE PACKAGE TOP BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2° 10° | | 2° 10° | |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

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