



## Dual, 12-Bit, 125MSPS DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- 125MSPS UPDATE RATE
- SINGLE SUPPLY: +3.3V or +5V
- HIGH SFDR: 70dB at  $f_{OUT} = 20\text{MHz}$
- LOW GLITCH: 2pVs
- LOW POWER: 310mW
- INTERNAL REFERENCE
- POWER-DOWN MODE: 23mW

### DESCRIPTION

The DAC2902 is a monolithic, 12-bit, dual-channel, high-speed Digital-to-Analog Converter (DAC), and is optimized to provide high dynamic performance while dissipating only 310mW.

Operating with high update rates of up to 125MSPS, the DAC2902 offers exceptional dynamic performance, and enables the generation of very-high output frequencies suitable for “Direct IF” applications. The DAC2902 has been optimized for communications applications in which separate I and Q data are processed while maintaining tight gain and offset matching.

Each DAC has a high-impedance differential-current output, suitable for single-ended or differential analog-output configurations.

### APPLICATIONS

- COMMUNICATIONS:  
Base Stations, WLL, WLAN  
Baseband I/Q Modulation
- MEDICAL/TEST INSTRUMENTATION
- ARBITRARY WAVEFORM GENERATORS (ARB)
- DIRECT DIGITAL SYNTHESIS (DDS)

The DAC2902 combines high dynamic performance with a high throughput rate to create a cost-effective solution for a wide variety of waveform-synthesis applications:

- Pin compatibility between family members provides 10-bit (DAC2900), 12-bit (DAC2902), and 14-bit (DAC2904) resolution.
- Pin compatible to the AD9765 dual DAC.
- Gain matching is typically 0.5% of full-scale, and offset matching is specified at 0.02% max.
- The DAC2902 utilizes an advanced CMOS process; the segmented architecture minimizes output-glitch energy, and maximizes the dynamic performance.
- All digital inputs are +3.3V and +5V logic compatible. The DAC2902 has an internal reference circuit, and allows use of an external reference.
- The DAC2902 is available in a TQFP-48 package, and is specified over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



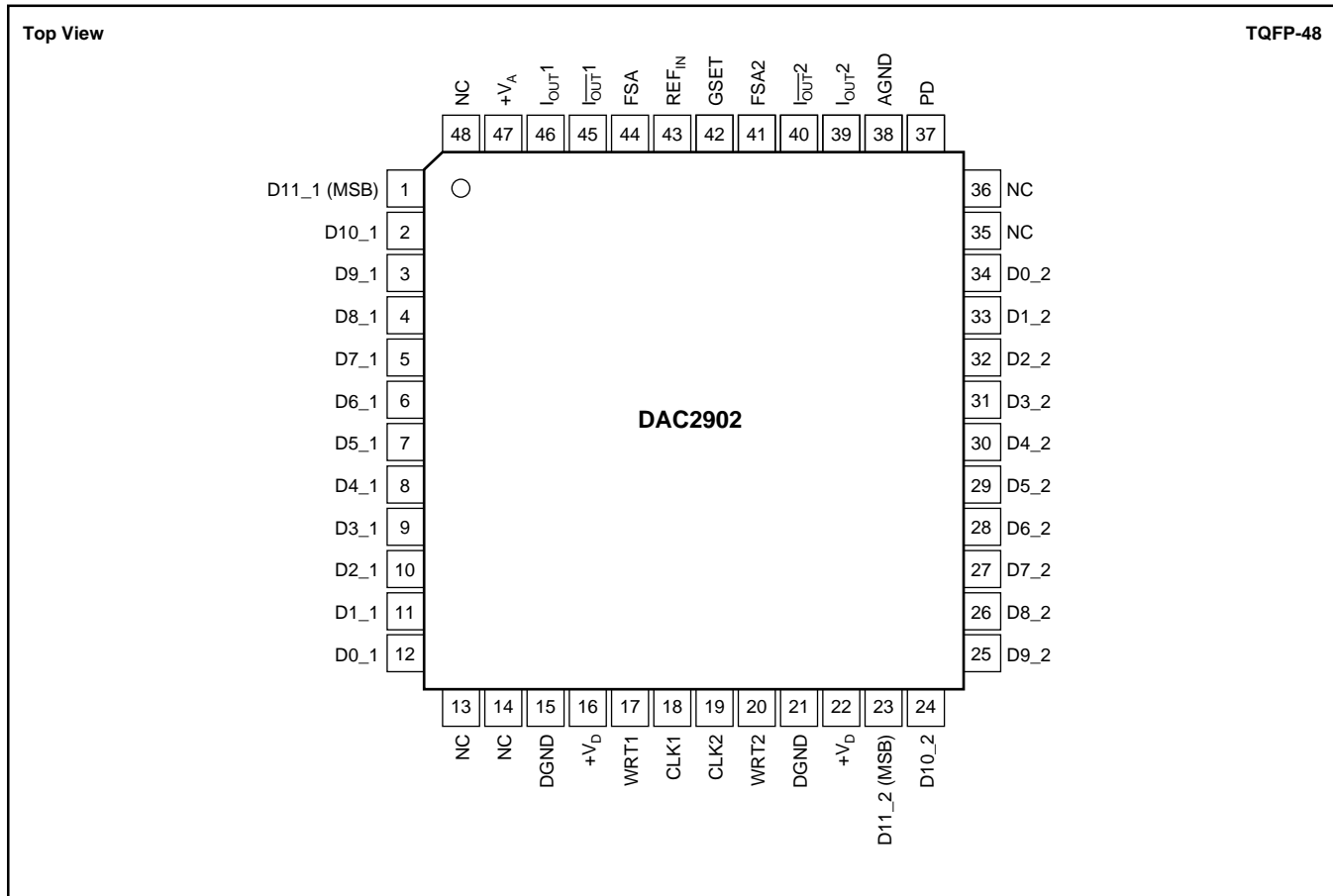
# ELECTRICAL CHARACTERISTICS (Cont.)

T<sub>MIN</sub> to T<sub>MAX</sub>, +V<sub>A</sub> = +5V, +V<sub>D</sub> = +3.3V, differential transformer coupled output, 50 $\Omega$  doubly terminated, unless otherwise noted. Independent Gain Mode.

PARAMETER	CONDITIONS	DAC2902Y			UNITS
		MIN	TYP	MAX	
<b>DYNAMIC PERFORMANCE (Cont.)</b>					
Signal-to-Noise Ratio (SNR)	0dBFS Output		68		dBc
f <sub>OUT</sub> = 5.02MHz, f <sub>CLOCK</sub> = 50MHz					
Signal-to-Noise and Distortion (SINAD)	0dBFS Output		67		dBc
f <sub>OUT</sub> = 5.02MHz, f <sub>CLOCK</sub> = 50MHz					
Channel Isolation					
f <sub>OUT</sub> = 1MHz, f <sub>CLOCK</sub> = 52MSPS			85		dBc
f <sub>OUT</sub> = 20MHz, f <sub>CLOCK</sub> = 125MSPS			77		dBc
Output Settling Time <sup>(2)</sup>	to 0.1%		30		ns
Output Rise Time <sup>(2)</sup>	10% to 90%		2		ns
Output Fall Time <sup>(2)</sup>	10% to 90%		2		ns
Glitch Impulse			2		pV-s
<b>DC ACCURACY</b>					
Full-Scale Output Range <sup>(3)</sup> (FSR)	All Bits HIGH, I <sub>OUT</sub>	2		20	mA
Output Compliance Range		-1.0		+1.25	V
Gain Error—Full-Scale	With Internal Reference	-5	±1	+5	%FSR
Gain Error	With External Reference	-2.5	±1	+2.5	%FSR
Gain Matching	With Internal Reference	-2.0	0.5	+2.0	%FSR
Gain Drift	With Internal Reference		±50		ppmFSR/°C
Offset Error	With Internal Reference	-0.02		+0.02	%FSR
Offset Drift	With Internal Reference		±0.2		ppmFSR/°C
Power-Supply Rejection, +V <sub>A</sub>	+5V, ±10%	-0.2		+0.2	%FSR/V
Power-Supply Rejection, +V <sub>D</sub>	+3.3V, ±10%	-0.025		+0.025	%FSR/V
Output Noise	I <sub>OUT</sub> = 20mA, R <sub>LOAD</sub> = 50 $\Omega$		50		pA/√Hz
	I <sub>OUT</sub> = 2mA		30		pA/√Hz
Output Resistance			200		k $\Omega$
Output Capacitance	I <sub>OUT</sub> , I <sub>OUT</sub> to Ground		6		pF
<b>REFERENCE/CONTROL AMP</b>					
Reference Voltage		+1.18	+1.25	+1.31	V
Reference Voltage Drift			±50		ppmFSR/°C
Reference Output Current			100		nA
Reference Multiplying Bandwidth			0.3		MHz
Input Compliance Range		+0.5		+1.25	V
<b>DIGITAL INPUTS</b>					
Logic Coding			Straight Binary		
Logic High Voltage, V <sub>IH</sub>	+V <sub>D</sub> = +5V	3.5	5		V
Logic Low Voltage, V <sub>IL</sub>	+V <sub>D</sub> = +5V		0	1.2	V
Logic High Voltage, V <sub>IH</sub>	+V <sub>D</sub> = 3.3V	2	3		V
Logic Low Voltage, V <sub>IL</sub>	+V <sub>D</sub> = 3.3V		0	0.8	V
Logic High Current: I <sub>IH</sub> <sup>(4)</sup>	+V <sub>D</sub> = 3.3V		±10		$\mu$ A
Logic Low Current	+V <sub>D</sub> = 3.3V		±10		$\mu$ A
Input Capacitance			5		pF
<b>POWER SUPPLY</b>					
Supply Voltages					
+V <sub>A</sub>		+3.0	+5	+5.5	V
+V <sub>D</sub>		+3.0	+3.3	+5.5	V
Supply Current					
I <sub>VA</sub> <sup>(5)</sup>	V <sub>A</sub> = +5V, I <sub>OUT</sub> = 20mA		59	64	mA
I <sub>VA</sub> <sup>(5)</sup>	Power-Down Mode		1.7	3	mA
I <sub>VD</sub> <sup>(5)</sup>			4.2	7	mA
I <sub>VD</sub> <sup>(6)</sup>			15.5	18	mA
Power Dissipation <sup>(5)</sup>	V <sub>A</sub> = +5V, V <sub>D</sub> = 3.3V, I <sub>OUT</sub> = 20mA		310	345	mW
Power Dissipation <sup>(6)</sup>	V <sub>A</sub> = +5V, V <sub>D</sub> = 3.3V, I <sub>OUT</sub> = 20mA		345	380	mW
Power Dissipation <sup>(5)</sup>	V <sub>A</sub> = +5V, V <sub>D</sub> = 3.3V, I <sub>OUT</sub> = 2mA		130		mW
Power Dissipation	Power-Down Mode		23	38	mW
Thermal Resistance, TQFP-48					
$\theta_{JA}$			60		°C/W
$\theta_{JC}$			13		°C/W
<b>TEMPERATURE RANGE</b>					
Specified	Ambient	-40		+85	°C
Operating	Ambient	-40		+85	°C

NOTES: (1) At output I<sub>OUT</sub>, while driving a virtual ground. (2) Measured single-ended into 50 $\Omega$  load. (3) Nominal full-scale output current is 32 • I<sub>REF</sub>; see Application section for details. (4) Typically 45 $\mu$ A for the PD pin, which has an internal pull-down resistor. (5) Measured at f<sub>CLOCK</sub> = 25MSPS and f<sub>OUT</sub> = 1MHz. (6) Measured at f<sub>CLOCK</sub> = 100MSPS and f<sub>OUT</sub> = 40MHz.

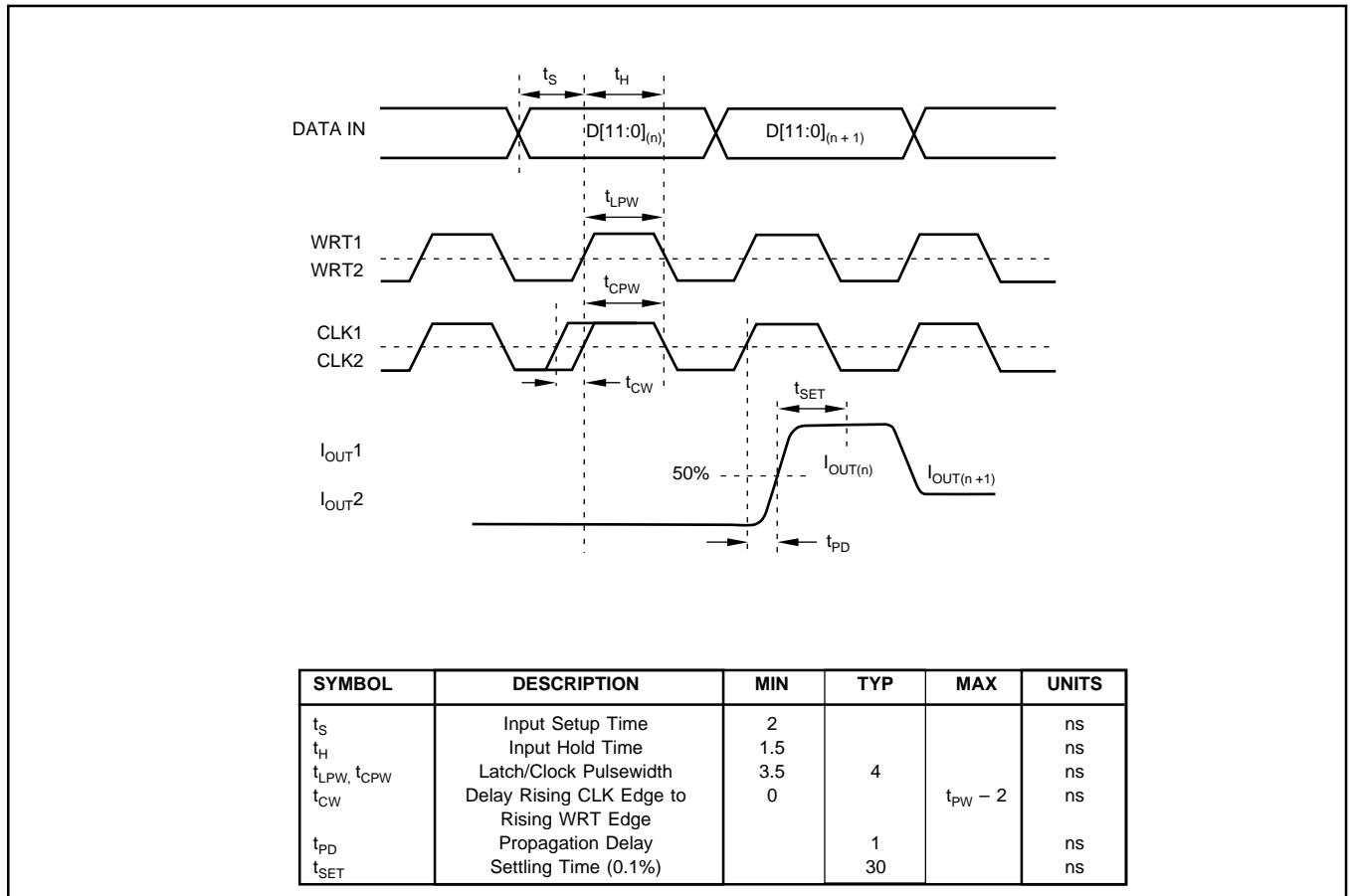
## PIN CONFIGURATION



## PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1-12	D[11:0]_1	Data Port DAC1, Data Bit 11 (MSB) to Bit 0 (LSB).
13, 14	NC	No Connection
15	DGND	Digital Ground
16	+V <sub>D</sub>	Digital Supply, +3.0V to +5.5V
17	WRT1	DAC1 Input Latches Write Signal
18	CLK1	Clock Input DAC1
19	CLK2	Clock Input DAC2
20	WRT2	DAC2 Input Latches Write Signal
21	DGND	Digital Ground
22	+V <sub>D</sub>	Digital Supply, +3.0V to +5.5V
23-34	D[11:0]_2	Data Port DAC2, Data Bit 11 (MSB) to Bit 0 (LSB).
35, 36	NC	No Connection
37	PD	Power-Down Function Control Input; "H" = DAC in power-down mode; "L" = DAC in normal operation (Internal pull-down for default "L").
38	AGND	Analog Ground
39	I <sub>OUT2</sub>	Current Output DAC2. Full-scale with all bits of data port 2 HIGH.
40	I <sub>OUT2</sub>	Complementary Current Output DAC2. Full-scale with all bits of data port 2 LOW.
41	FSA2	Full-Scale Adjust, DAC2. Connect External R <sub>SET</sub> Resistor
42	GSET	Gain-Setting Mode (H = 1 Resistor, L = 2 Resistor)
43	REF <sub>IN</sub>	Internal Reference Voltage output; External Reference Voltage input. Bypass with 0.1µF to AGND for internal reference operation.
44	FSA1	Full-Scale Adjust, DAC1. Connect External R <sub>SET</sub> Resistor
45	I <sub>OUT1</sub>	Complementary Current Output DAC1. Full-scale with all bits of data port 1 LOW.
46	I <sub>OUT1</sub>	Current Output DAC1. Full-scale with all bits of data port 1 HIGH.
47	+V <sub>A</sub>	Analog Supply, +3.0V to +5.5V
48	NC	No Connection

## TIMING DIAGRAM



## DIGITAL INPUTS AND TIMING

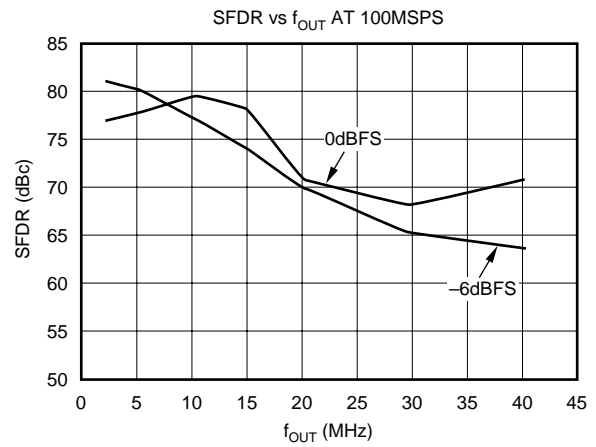
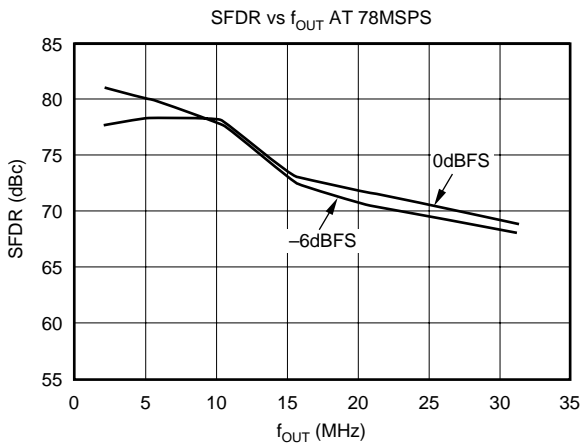
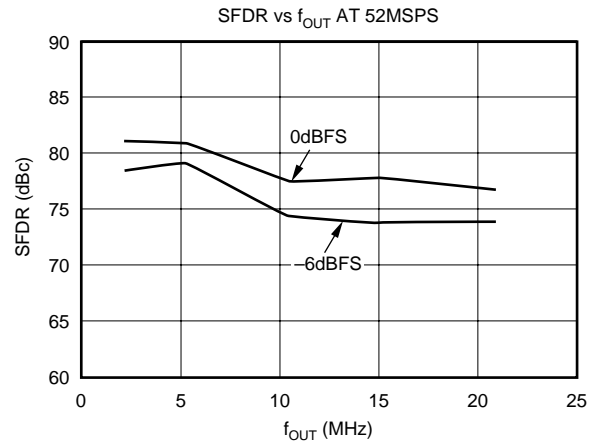
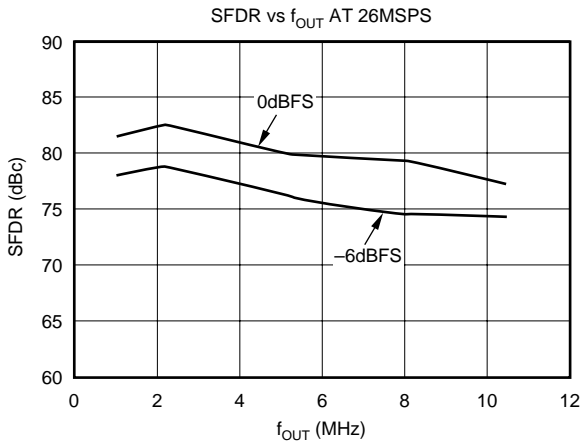
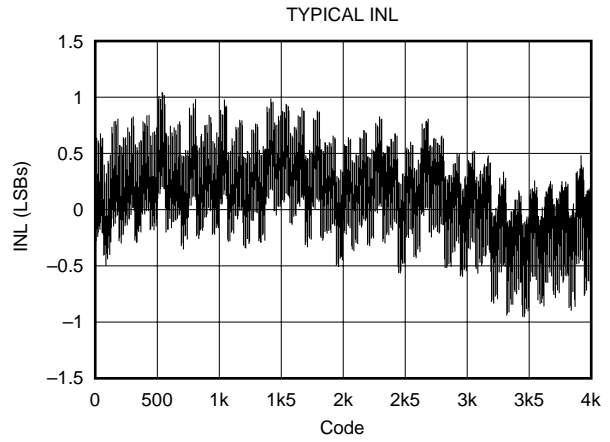
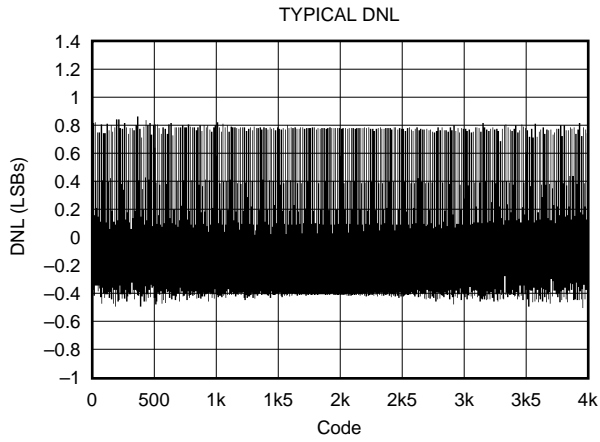
The data input ports of the DAC2902 accept a standard positive coding with data bit D11 being the most significant bit (MSB). The converter outputs support a clock rate of up to 125MSPS. The best performance will typically be achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Also, the set-up and hold times may be chosen within their specified limits.

All digital inputs of the DAC2902 are CMOS compatible. The logic thresholds depend on the applied digital supply voltages, such that they are set to approximately half the supply voltage;  $V^{th} = +V_D/2$  ( $\pm 20\%$  tolerance). The DAC2902 is designed to operate with a digital supply ( $+V_D$ ) of +3.0V to +5.5V.

The two converter channels within the DAC2902 consist of two independent, 12-bit, parallel data ports. Each DAC-channel is controlled by its own set of write (WRT1, WRT2) and clock (CLK1, CLK2) inputs. Here, the WRT lines control the channel input latches and the CLK lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRT line. This data is presented to the DAC latch on the following falling edge of the WRT signal. On the next rising edge of the CLK line, the DAC is updated with the new data and the analog output signal will change accordingly. The double latch architecture of the DAC2902 results in a defined sequence for the WRT and CLK signals, expressed by parameter ' $t_{CW}$ '. A correct timing is observed when the rising edge of CLK occurs at the same time, or before, the rising edge of the WRT signal. This condition can simply be met by connecting the WRT and CLK lines together. Note that all specifications were measured with the WRT and CLK lines connected together.

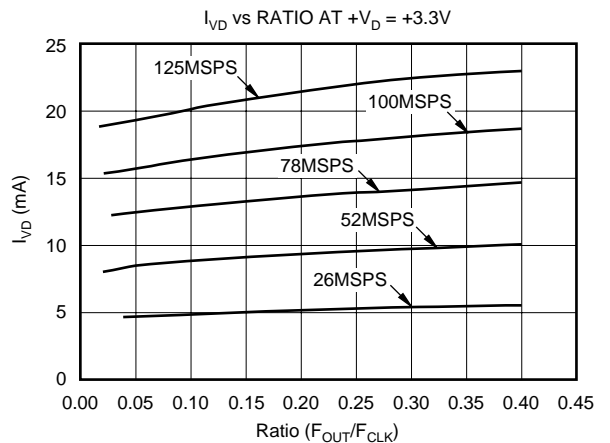
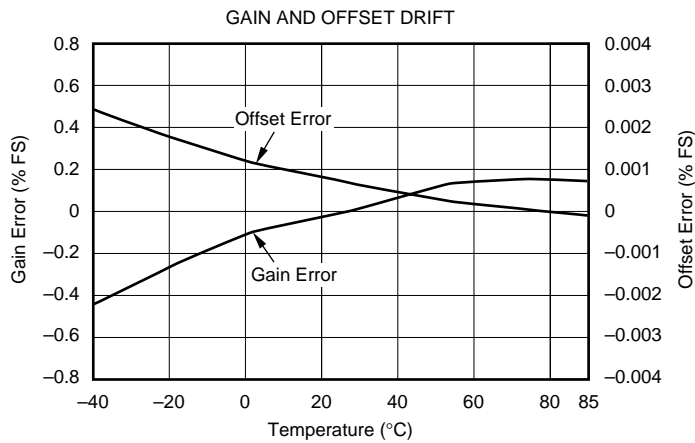
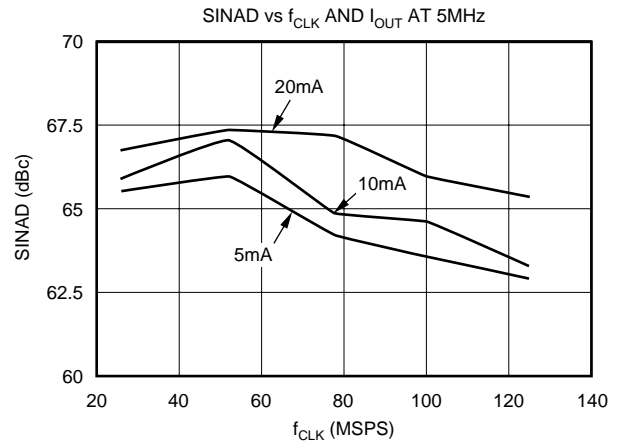
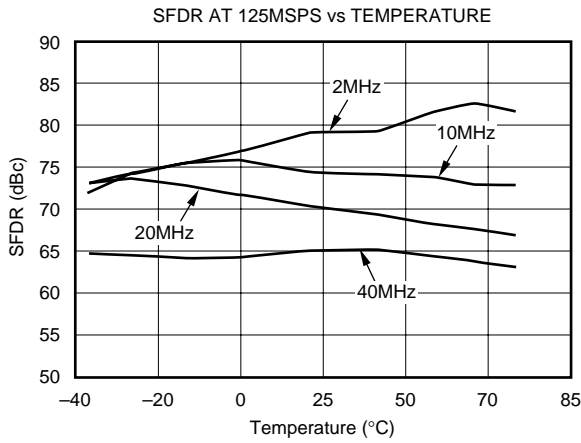
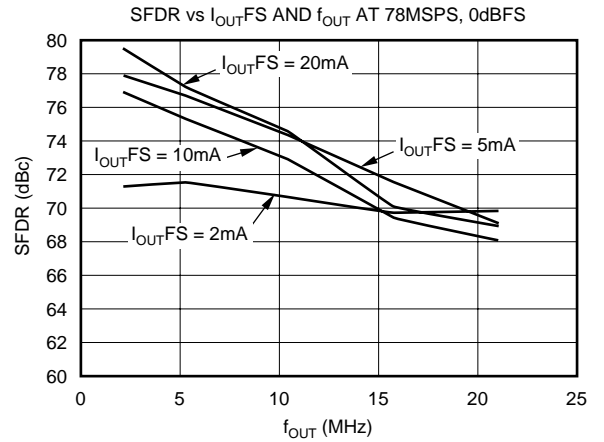
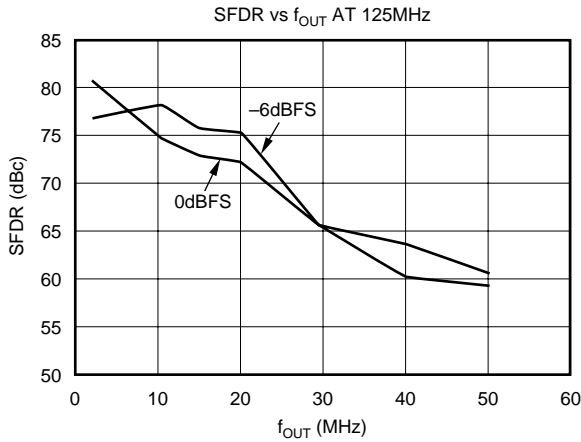
# TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $+V_D = +3.3\text{V}$ ,  $+V_A = +5\text{V}$ , differential transformer coupled,  $I_{\text{OUT}} = 20\text{mA}$ ,  $50\Omega$  double terminated load, SFDR up to Nyquist, unless otherwise noted.



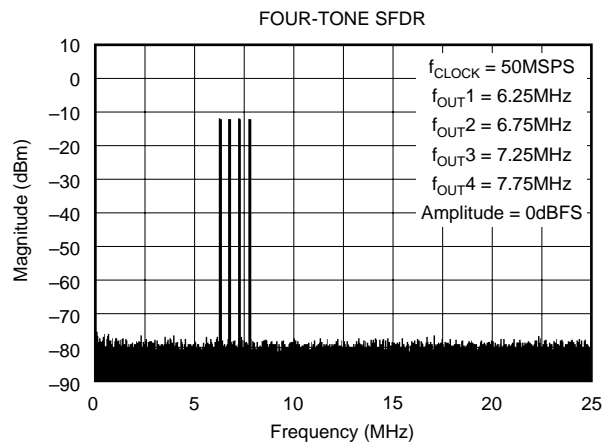
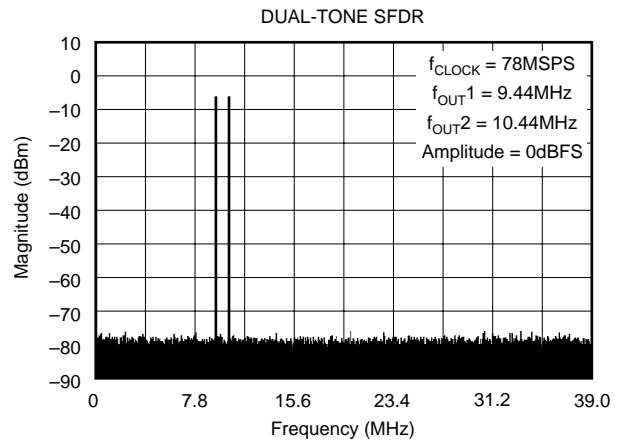
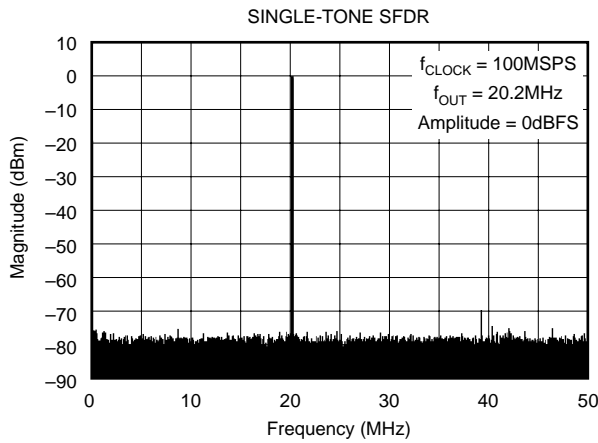
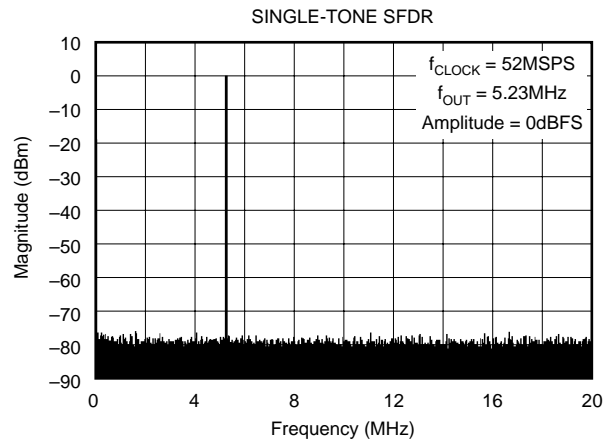
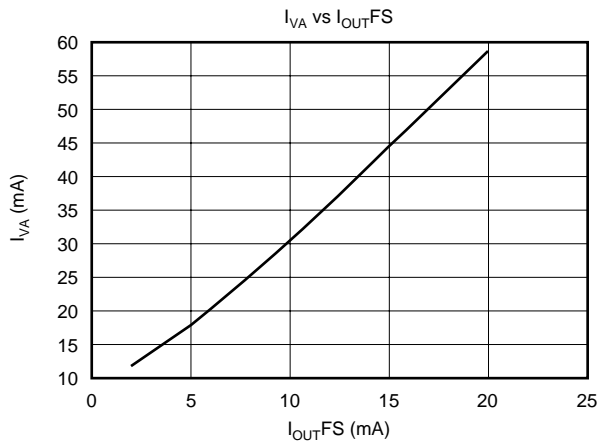
# TYPICAL CHARACTERISTICS (Cont.)

$T_A = 25^\circ\text{C}$ ,  $+V_D = +3.3\text{V}$ ,  $+V_A = +5\text{V}$ , differential transformer coupled,  $I_{\text{OUT}} = 20\text{mA}$ , 50 $\Omega$  double terminated load, SFDR up to Nyquist, unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

$T_A = 25^\circ\text{C}$ ,  $+V_D = +3.3\text{V}$ ,  $+V_A = +5\text{V}$ , differential transformer coupled,  $I_{\text{OUT}} = 20\text{mA}$ , 50 $\Omega$  double terminated load, SFDR up to Nyquist, unless otherwise noted.





# APPLICATION INFORMATION

## THEORY OF OPERATION

The architecture of the DAC2902 uses the current steering technique to enable fast switching and a high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20mA, as shown in Figure 1. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node,  $I_{OUT}$  or  $\overline{I_{OUT}}$ . The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy, improves the dynamic performance (SFDR), and DNL. The current outputs maintain a very high output impedance of greater than 200k $\Omega$ .

The full-scale output current is determined by the ratio of the internal reference voltage (approx. +1.25V) and an external resistor,  $R_{SET}$ . The resulting  $I_{REF}$  is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2mA to 20mA, depending on the value of  $R_{SET}$ .

The DAC2902 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises the current source array with its associated switches, and the reference circuitry.

## DAC TRANSFER FUNCTION

Each of the DACs in the DAC2902 has a complementary current output,  $I_{OUT1}$  and  $\overline{I_{OUT2}}$ . The full-scale output current,  $I_{OUTFS}$ , is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT} + \overline{I_{OUT}} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT} = I_{OUTFS} \cdot (\text{Code}/4096) \quad (2)$$

$$\overline{I_{OUT}} = I_{OUTFS} \cdot (4095 - \text{Code}) \quad (3)$$

where 'Code' is the decimal representation of the DAC data input word. Additionally,  $I_{OUTFS}$  is a function of the reference current  $I_{REF}$ , which is determined by the reference voltage and the external setting resistor,  $R_{SET}$ .

$$I_{OUTFS} = 32 \cdot I_{REF} = 32 \cdot V_{REF}/R_{SET} \quad (4)$$

In most cases the complementary outputs will drive resistive loads or a terminated transformer. A signal voltage will develop at each output according to:

$$V_{OUT} = I_{OUT} \cdot R_{LOAD} \quad (5)$$

$$V_{\overline{OUT}} = \overline{I_{OUT}} \cdot R_{LOAD} \quad (6)$$

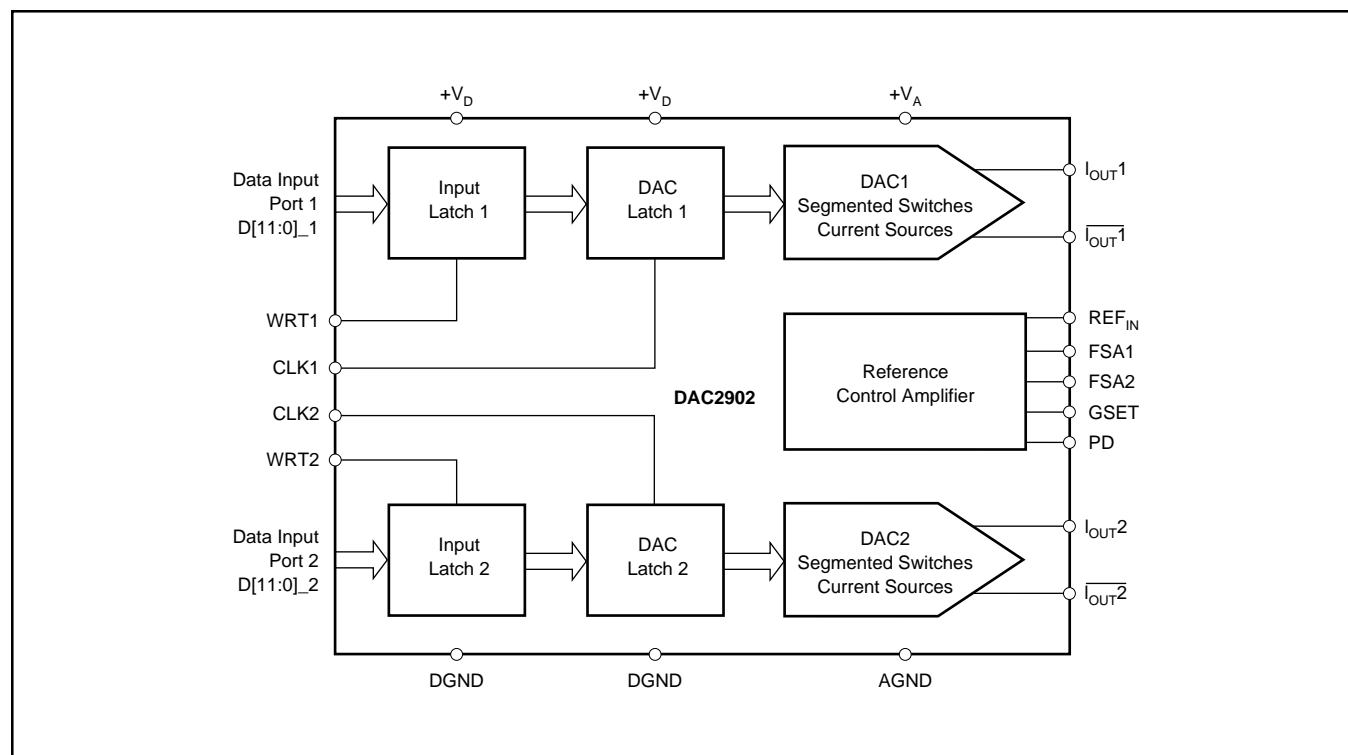


FIGURE 1. Block Diagram of the DAC2902.

The value of the load resistance is limited by the output compliance specification of the DAC2902. To maintain specified linearity performance, the voltage for  $I_{OUT}$  and  $I_{\overline{OUT}}$  should not exceed the maximum allowable compliance range.

The two single-ended output voltages can be combined to find the total differential output swing:

$$V_{OUTDIFF} = V_{OUT} - V_{\overline{OUT}} = \frac{(2 \cdot \text{Code} - 4095)}{4096} \cdot I_{OUTFS} \cdot R_{LOAD} \quad (7)$$

## ANALOG OUTPUTS

The DAC2902 provides two complementary current outputs,  $I_{OUT}$  and  $I_{\overline{OUT}}$ . The simplified circuit of the analog output stage representing the differential topology is shown in Figure 2. The output impedance of  $I_{OUT}$  and  $I_{\overline{OUT}}$  results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

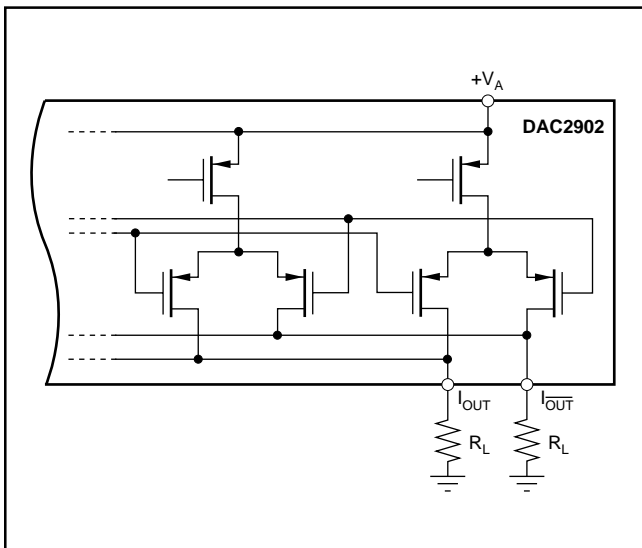


FIGURE 2. Equivalent Analog Output.

The signal voltage swing that may develop at the two outputs,  $I_{OUT}$  and  $I_{\overline{OUT}}$ , is limited by a negative and positive compliance. The negative limit of  $-1V$  is given by the breakdown voltage of the CMOS process, and exceeding it will compromise the reliability of the DAC2902, or even cause permanent damage. With the full-scale output set to 20mA, the positive compliance equals 1.25V, operating with an analog supply of  $+V_A = 5V$ . Note that the compliance range decreases to about 1V for a selected output current of  $I_{OUTFS} = 2mA$ . Care should be taken that the configuration of DAC2902 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5Vp-p. This is the case for a 50Ω doubly-terminated load and a 20mA full-scale output current. A variety of loads can

be adapted to the output of the DAC2902 by selecting a suitable transformer while maintaining optimum voltage levels at  $I_{OUT}$  and  $I_{\overline{OUT}}$ . Furthermore, using the differential output configuration in combination with a transformer will be instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20mA. A lower full-scale range down to 2mA may be considered for applications that require a low power consumption, but can tolerate a slightly reduced performance level.

## OUTPUT CONFIGURATIONS

The current outputs of the DAC2902 allow for a variety of configurations, some of which are illustrated in Table I. As mentioned previously, utilizing the converter's differential outputs will yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps will be suitable for a DC-coupled configuration.

INPUT CODE (D11 - D0)	$I_{OUT}$	$I_{\overline{OUT}}$
1111 1111 1111	20mA	0mA
1000 0000 0000	10mA	10mA
0000 0000 0000	0mA	20mA

TABLE I. Input Coding Versus Analog Output Current.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground will convert the output current into a ground-referenced voltage signal. To improve on the DC linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

## DIFFERENTIAL WITH TRANSFORMER

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance (see Figure 3). The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements. The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio), the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs. The model shown, ADTT1-1 (by Mini-Circuits), has a 1:1 ratio and may be used to interface the DAC2902 to a 50Ω load. This results in a 25Ω load for each of the outputs,  $I_{OUT}$  and  $I_{\overline{OUT}}$ . The output signals are ac coupled and inherently isolated because of its magnetic coupling.

As shown in Figure 3, the transformer's center tap is connected to ground. This forces the voltage swing on  $I_{OUT}$  and  $I_{\overline{OUT}}$  to be centered at 0V. In this case the two resistors,  $R_L$ , may be replaced with one,  $R_{DIFF}$ , or omitted altogether. This approach should only be used if all components are close to each other, and if the VSWR is not important. A complete power transfer from the DAC output to the load can be realized, but the output compliance range should be observed. Alternatively, if the center tap is not connected, the signal swing will be centered at  $R_L \cdot I_{OUTFS}/2$ . However, in this case, the two resistors ( $R_L$ ) must be used to enable the necessary DC-current flow for both outputs.

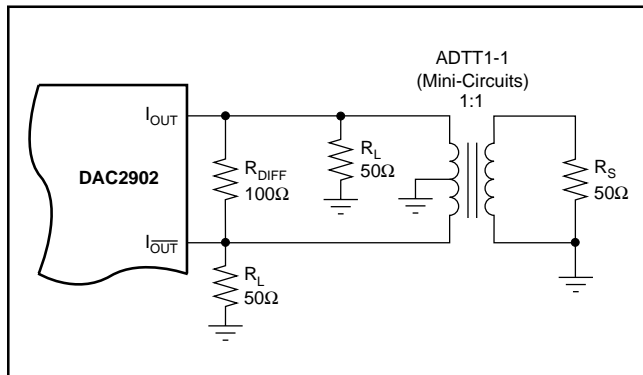


FIGURE 3. Differential Output Configuration Using an RF Transformer.

#### DIFFERENTIAL CONFIGURATION USING AN OP AMP

If the application requires a DC-coupled output, a difference amplifier may be considered, as shown in Figure 4. Four external resistors are needed to configure the voltage-feedback op amp OPA680 as a difference amplifier performing the differential to single-ended conversion. Under the shown configuration, the DAC2902 generates a differential output signal of 0.5Vp-p at the load resistors,  $R_L$ . The resistor values shown were selected to result in a symmetric 25 $\Omega$  loading for each of the current outputs since the input impedance of the difference amplifier is in parallel to resistors  $R_L$ , and should be considered.

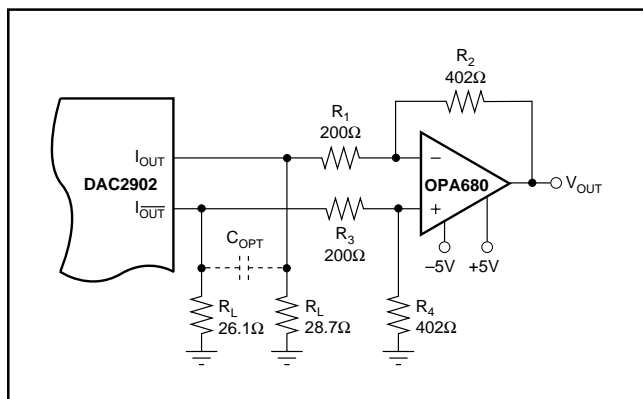


FIGURE 4. Difference Amplifier Provides Differential to Single-Ended Conversion and DC-Coupling.

The OPA680 is configured for a gain of two. Therefore, operating the DAC2902 with a 20mA full-scale output will produce a voltage output of  $\pm 1V$ . This requires the amplifier to operate off of a dual power supply ( $\pm 5V$ ). The tolerance of the resistors typically sets the limit for the achievable common-mode rejection. An improvement can be obtained by fine tuning resistor  $R_4$ .

This configuration typically delivers a lower level of ac performance than the previously discussed transformer solution because the amplifier introduces another source of distortion. Suitable amplifiers should be selected based on their slew-rate, harmonic distortion, and output swing capabilities. High-speed amplifiers like the OPA680 or OPA687 may be considered. The ac performance of this circuit may be improved by adding a small capacitor ( $C_{DIFF}$ ) between the outputs  $I_{OUT}$  and  $I_{\overline{OUT}}$ , as shown in Figure 4). This will introduce a real pole to create a low-pass filter in order to slew-limit the DAC's fast output signal steps, that otherwise could drive the amplifier into slew-limitations or into an overload condition; both would cause excessive distortion. The difference amplifier can easily be modified to add a level shift for applications requiring the single-ended output voltage to be unipolar, i.e., swing between 0V and +2V.

#### DUAL TRANSIMPEDANCE OUTPUT CONFIGURATION

The circuit example of Figure 5 shows the signal output currents connected into the summing junctions of the dual voltage-feedback op amp OPA2680 that is set up as a transimpedance stage, or 'I-to-V converter'. With this circuit, the DAC's output will be kept at a virtual ground, minimizing the effects of output impedance variations, which results in the best DC linearity (INL). As mentioned previously, care should be taken not to drive the amplifier into slew-rate limitations, and produce unwanted distortion.

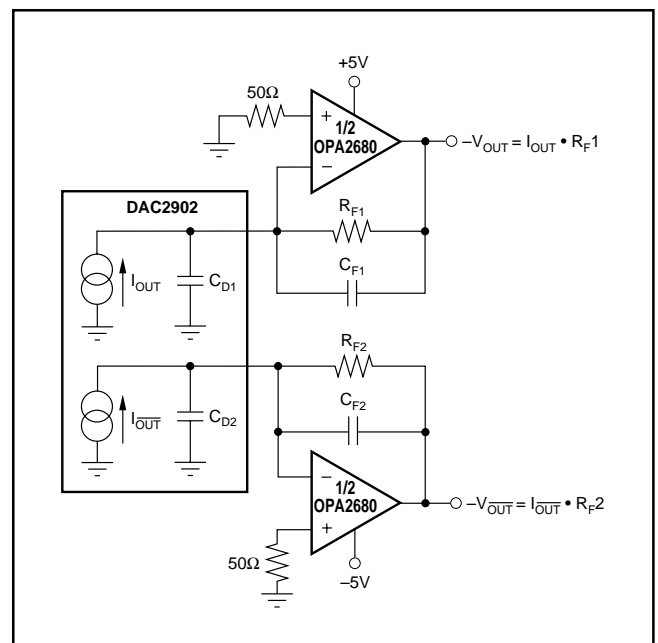


FIGURE 5. Dual, Voltage-Feedback Amplifier OPA2680 Forms Differential Transimpedance Amplifier.

The DC gain for this circuit is equal to feedback resistor  $R_F$ . At high frequencies, the DAC output impedance ( $C_{D1}$ ,  $C_{D2}$ ) will produce a 0 in the noise gain for the OPA2680 that may cause peaking in the closed-loop frequency response.  $C_F$  is added across  $R_F$  to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

(8)

with  $GBP$  = Gain Bandwidth Product of OPA,

which will give a corner frequency  $f_{-3dB}$  of approximately:

(9)

The full-scale output voltage is simply defined by the product of  $I_{OUTFS} \cdot R_F$ , and has a negative unipolar excursion. To improve on the ac performance of this circuit, adjustment of  $R_F$  and/or  $I_{OUTFS}$  should be considered. Further extensions of this application example may include adding a differential filter at the OPA2680's output followed by a transformer, in order to convert to a single-ended signal.

### SINGLE-ENDED CONFIGURATION

Using a single-load resistor connected to the one of the DAC outputs, a simple current-to-voltage conversion can be accomplished. The circuit in Figure 6 shows a  $50\Omega$  resistor connected to  $I_{OUT}$ , providing the termination of the further connected  $50\Omega$  cable. Therefore, with a nominal output current of 20mA, the DAC produces a total signal swing of 0V to 0.5V into the  $25\Omega$  load.

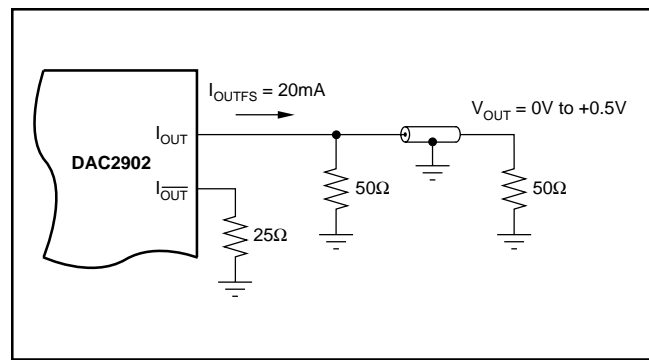


FIGURE 6. Driving a Doubly Terminated  $50\Omega$  Cable Directly.

Different load resistor values may be selected as long as the output compliance range is not exceeded. Additionally, the output current,  $I_{OUTFS}$ , and the load resistor, may be mutually adjusted to provide the desired output signal swing and performance.

### INTERFACING ANALOG QUADRATURE MODULATORS

One of the main applications for the dual-channel DAC is baseband I- and Q-channel transmission for digital communications. In this application, the DAC is followed by an analog quadrature modulator, modulating an IF carrier with the baseband data, as shown in Figure 7. Often, the input stages of these quadrature modulators consist of npn-type transistors that require a DC bias (base) voltage of  $> 0.8V$ . The wide output compliance range ( $-10V$  to  $+1.25V$ ) allows for a direct DC-coupling between the DAC2902 and the quadrature modulator.

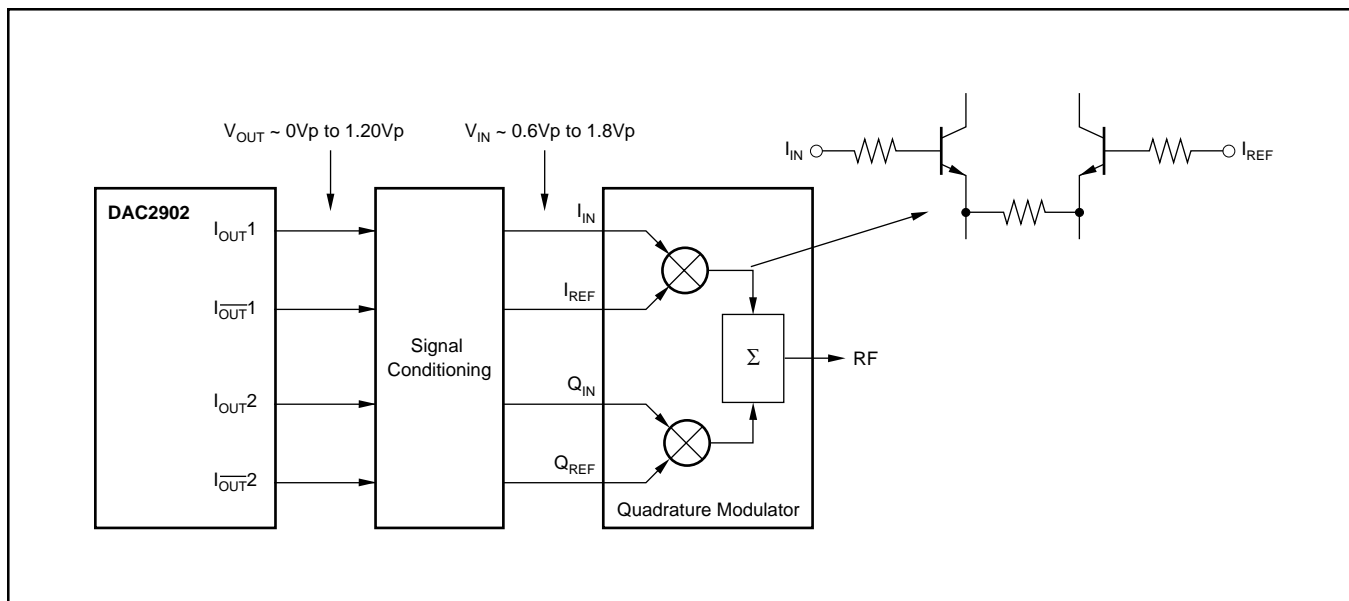


FIGURE 7. Generic Interface to a Quadrature Modulator. Signal Conditioning (Level-Shifting) May Be Required to Ensure Correct DC Common-Mode Levels At the Input of the Quadrature Modulator.

Figure 8 shows an example of a DC-coupled interface with DC level-shifting, using a precision resistor network. An ac-coupled interface, as shown in Figure 9, has the advantage that the common-mode levels at the input of the modulator can be set independently of those at the output of the DAC. Furthermore, no voltage loss is obtained in this setup.

### INTERNAL REFERENCE OPERATION

The DAC2902 has an on-chip reference circuit that comprises a 1.25V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current,  $I_{OUTFS}$ , of the DAC2902 is determined by the reference voltage,  $V_{REF}$ , and the value of resistor  $R_{SET}$ .  $I_{OUTFS}$  can be calculated by:

$$I_{OUTFS} = 32 \cdot I_{REF} = 32 \cdot V_{REF} / R_{SET} \quad (10)$$

The external resistor  $R_{SET}$  connects to the FSA pin (Full-Scale Adjust), see Figure 10. The reference control amplifier operates as a V-to-I converter producing a reference current,  $I_{REF}$ , which is determined by the ratio of  $V_{REF}$  and  $R_{SET}$  (as shown in Equation 10). The full-scale output current,  $I_{OUTFS}$ , results from multiplying  $I_{REF}$  by a fixed factor of 32.

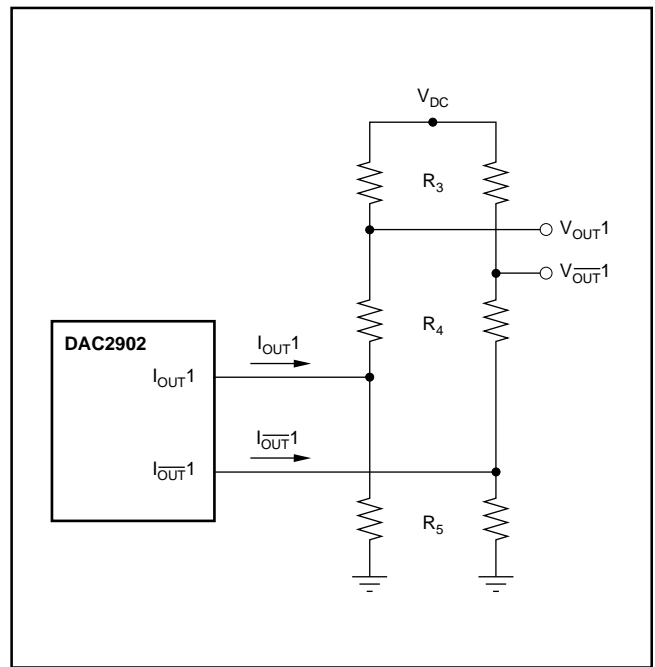


FIGURE 8. DC-Coupled Interface to Quadrature Modulator Applying Level Shifting.

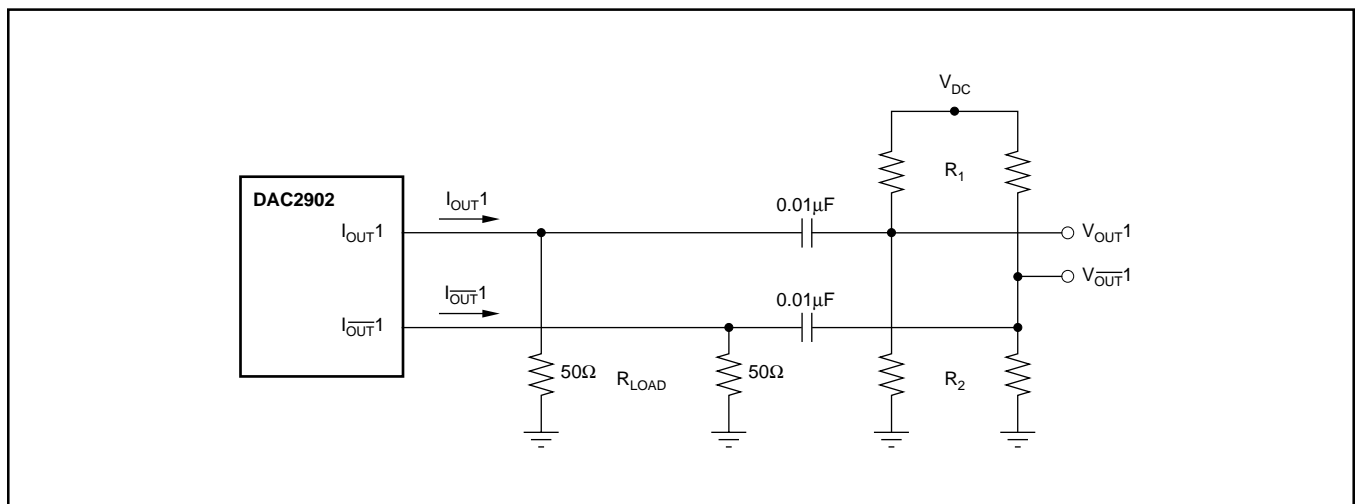


FIGURE 9. AC-Coupled Interface to Quadrature Modulator Applying Level Shifting.

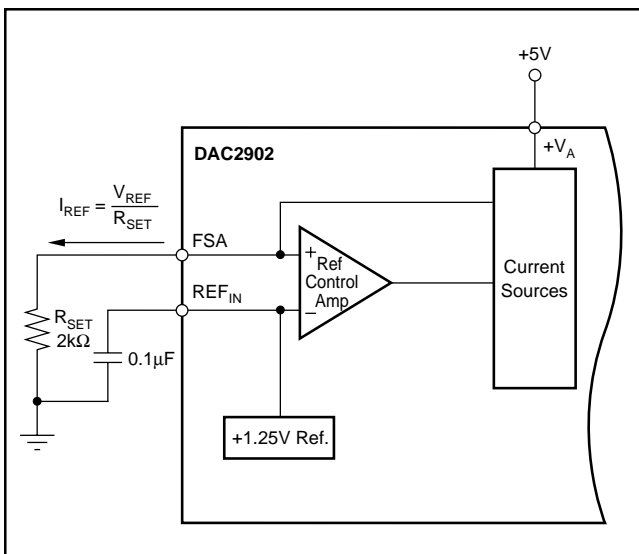


FIGURE 10. Internal Reference Configuration.

Using the internal reference, a 2kΩ resistor value results in a full-scale output of approximately 20mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20mA down to 2mA. Operating the DAC2902 at lower than 20mA output currents may be desirable for reasons of reducing the total power consumption, optimizing the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the REF<sub>IN</sub> pin with a ceramic chip capacitor of 0.1μF or more. The control amplifier is internally compensated, and its small signal bandwidth is approximately 0.3MHz.

### GAIN SETTING OPTIONS

The full-scale output current on the DAC2902 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be LOW (i.e. connected to AGND). In this mode, two external resistors are required—

one R<sub>SET</sub> connected to the FSA1 pin (pin 44) and the other to the FSA2 pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin HIGH (i.e. connected to +V<sub>A</sub>), the DAC2902 will switch into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R<sub>SET</sub> resistor connected to the FSA1 pin. The resistor at the FSA2 pin may be removed, however this is not required since this pin is not functional in this mode and the resistor has no effect to the gain equation. The formula for deriving the correct R<sub>SET</sub> remains unchanged, e.g. R<sub>SET</sub> = 2kΩ will result in a 20mA output for both DACs.

### EXTERNAL REFERENCE OPERATION

The internal reference can be disabled by simply applying an external reference voltage into the REF<sub>IN</sub> pin, which in this case functions as an input, as shown in Figure 11. The use of an external reference may be considered for applications that require higher accuracy and drift performance, or to add the ability of dynamic gain control.

While a 0.1μF capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, REF<sub>IN</sub>, has a high input impedance (1MΩ) and can easily be driven by various sources. Note that the voltage range of the external reference should stay within the compliance range of the reference input (0.5V to 1.25V).

### POWER-DOWN MODE

The DAC2902 features a power-down function that can be used to reduce the total supply current to less than 6mA. Applying a logic HIGH to the PD pin will initiate the power-down mode, while a logic LOW enables normal operation. When left unconnected, an internal active pull-down circuit will enable the normal operation of the converter.

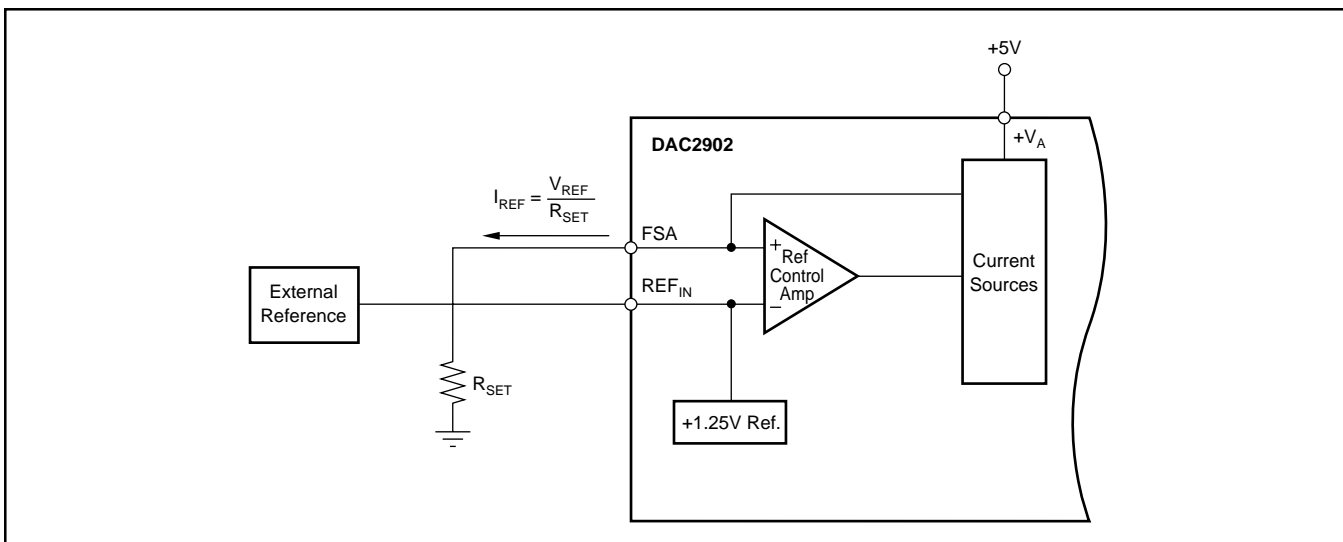


FIGURE 11. External Reference Configuration.

## GROUNDING, DECOUPLING, AND LAYOUT INFORMATION

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PCBs are recommended for best performance since they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

The DAC2902 uses separate pins for its analog and digital supply and ground connections. The placement of the decoupling capacitor should be such that the analog supply ( $+V_A$ ) is bypassed to the analog ground (AGND), and the digital supply bypassed to the digital ground (DGND). In most cases 0.1 $\mu$ F ceramic chip capacitors at each supply pin are adequate to provide a low impedance decoupling path. Keep in mind that their effectiveness largely depends on the proximity to the individual supply and ground pins. Therefore, they should be located as close as physically possible to those device leads. Whenever possible, the capacitors should be located immediately under each pair of supply/ground pins on the reverse side of the pc board. This layout approach will minimize the parasitic inductance of component leads and PCB runs.

Further supply decoupling with surface-mount tantalum capacitors (1 $\mu$ F to 4.7 $\mu$ F) may be added as needed in proximity of the converter.

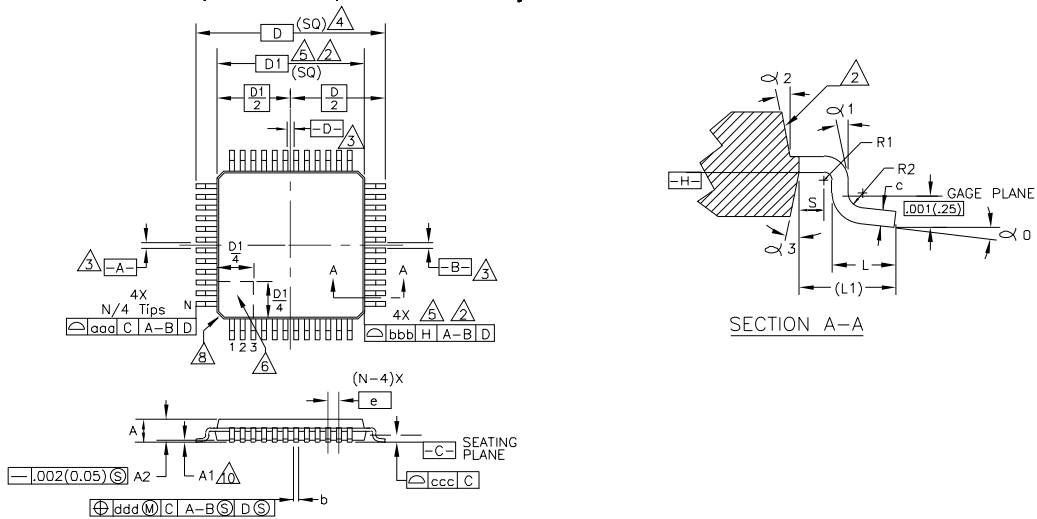
Low noise is required for all supply and ground connections to the DAC2902. It is recommended to use a multilayer PCB utilizing separate power and ground planes. Mixed signal designs require particular attention to the routing of the different supply currents and signal traces. Generally, analog supply and ground planes should only extend into analog signal areas, such as the DAC output signal and the reference signal. Digital supply and ground planes must be confined to areas covering digital circuitry, including the digital input lines connecting to the converter, as well as the clock signal. The analog and digital ground planes should be joined together at one point underneath the DAC. This can be realized with a short track of approximately 1/8" (3mm).

The power to the DAC2902 should be provided through the use of wide PCB runs or planes. Wide runs will present a lower trace impedance, further optimizing the supply decoupling. The analog and digital supplies for the converter should only be connected together at the supply connector of the pc board. In the case of only one supply voltage being available to power the DAC, ferrite beads along with bypass capacitors may be used to create an LC filter. This will generate a low-noise analog supply voltage that can then be connected to the  $+V_A$  supply pin of the DAC2902.

While designing the layout, it is important to keep the analog signal traces separated from any digital line, in order to prevent noise coupling onto the analog signal path.

# PACKAGE DRAWINGS

Package Number 355 - 48-Lead TQFP, 1.0 mm Thick, 7.0 x 7.0 mm Body



DIM	INCHES		MILLIMETERS		NOTE	DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	--	.047	--	1.20		aaa	.008	NOM.	0.20	NOM.	
A1	.002	.006	0.05	0.15	10	bbb	.008	NOM.	0.20	NOM.	
A2	.037	.041	0.95	1.05		ccc	.003	NOM.	0.08	NOM.	
b	.007	.011	0.17	0.27	7,9	ddd	.003	NOM.	0.08	NOM.	
c	.004	.008	0.09	0.20	9	$\alpha 0$	0°	7°	0°	7°	
D	.354	BASIC	9.00	BASIC	4	$\alpha 1$	0°	--	0°	--	
D1	.276	BASIC	7.00	BASIC	2,5	$\alpha 2$	11°	13°	11°	13°	
e	.020	BASIC	0.50	BASIC		$\alpha 3$	11°	13°	11°	13°	
L	.018	.030	0.45	0.75							
L1	.039	REF	1.00	REF							
N	48		48		12						
R1	.003	--	0.08	--							
R2	.003	.008	0.08	0.20							
S	.008	--	0.20	--							

NOTES:  
 1. ALL DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.  
 2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS .006 in.(0.15mm).  
 3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-].  
 4. TO BE DETERMINED AT SEATING PLANE [-C-].  
 5. DIMENSION D1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .001 in.(0.25mm) PER SIDE. D1 IS THE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.  
 6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.  
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION

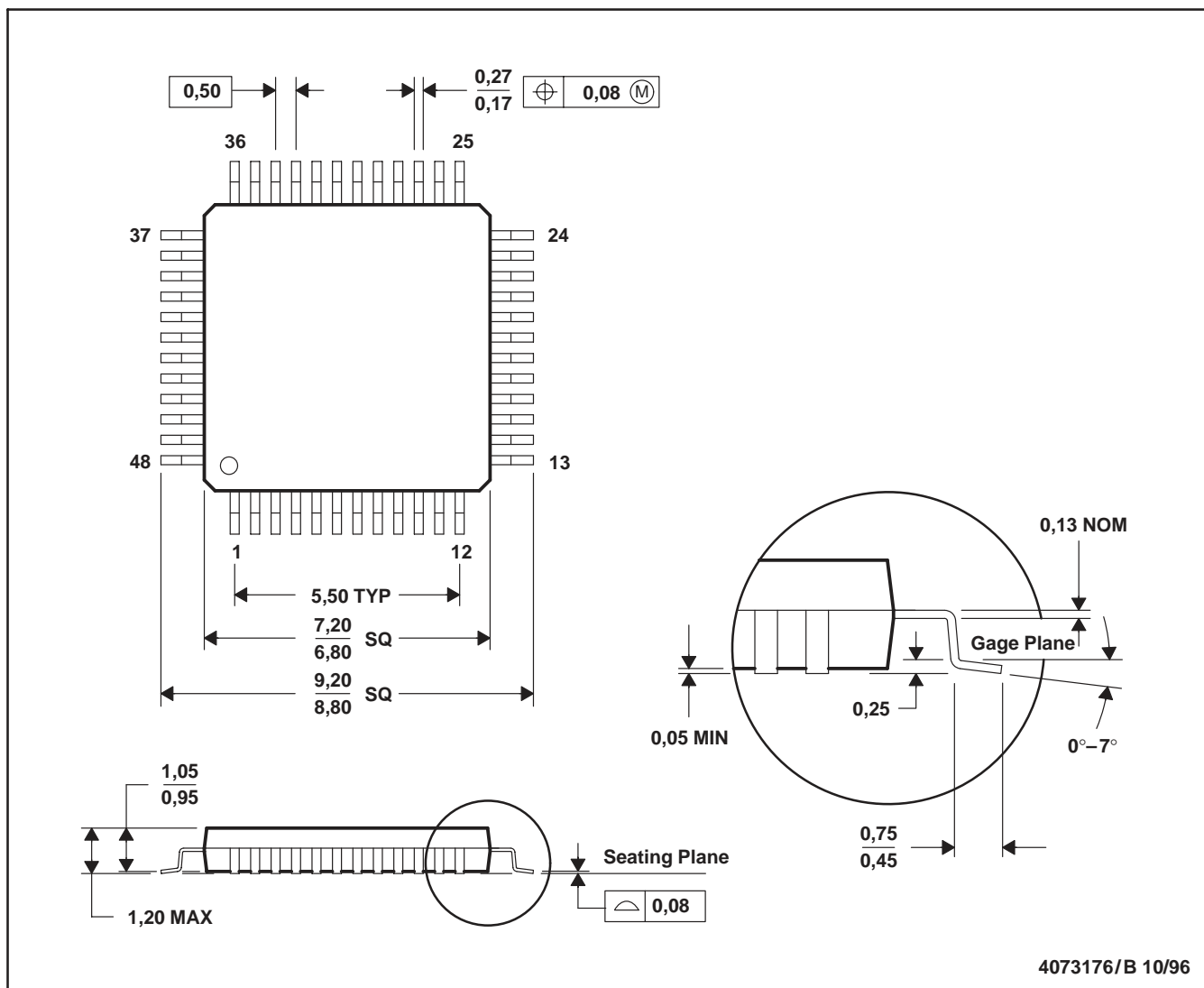
SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIM. BY MORE THAN .003 in.(0.08mm). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS .003 in.(0.07mm) FOR .016 in.(0.4mm) AND .020 in.(0.5mm) PITCH PACKAGES.  
 8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.  
 9. DIMENSION b AND c APPLY TO THE FLAT SECTION OF LEAD BETWEEN .004 in.(0.10mm) AND .002 in.(0.25mm) FROM THE LEAD TIP.  
 10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.  
 11. CONTROLLING DIMENSION IS MILLIMETER.  
 12. N IS THE NUMBER OF LEADS.

PACKAGE NUMBER: ZZ355      REV.: A  
 JEDEC NUMBER:      MS-026-ABC



PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated