FAIRCHILD
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March 1998

100331
Low Power Triple D Flip-Flop

General Description

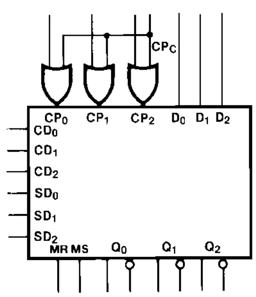
The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code:

Logic Symbol

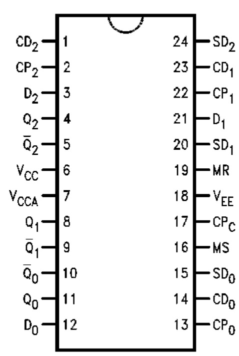


DS010262-1

Pin Names	Description
CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0-Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

Connection Diagrams

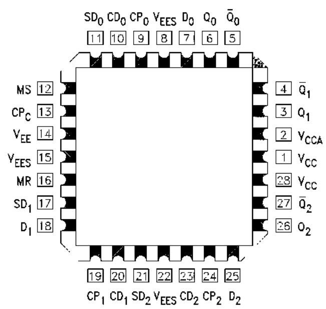
24-Pin DIP/SOIC



DS010262-2

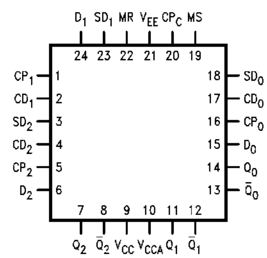
Connection Diagrams (Continued)

28-Pin PCC



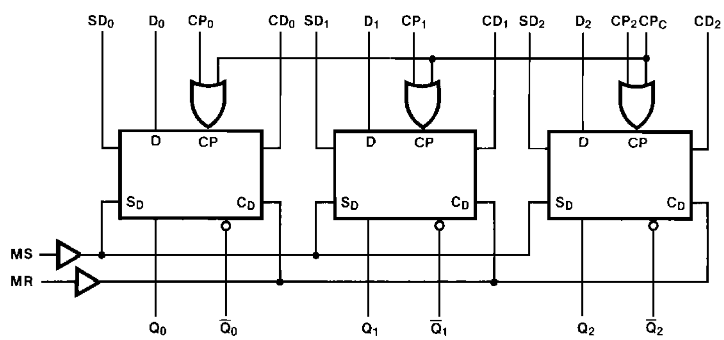
DS010262-4

24-Pin Quad Cerpak



DS010262-3

Logic Diagram



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Truth Tables

Synchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t + 1)$
L	⟋	L	L	L	L
H	⟋	L	L	L	H
L	L	⟋	L	L	L
H	L	⟋	L	L	H
X	L	L	L	L	Qn(t)
X	H	X	L	L	Qn(t)
X	X	H	L	L	Qn(t)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
⟋ = LOW to HIGH Transition

Asynchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t + 1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to	
Ground Pin (V_{EE})	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current	
(DC Output HIGH)	−50 mA
ESD (Note 2)	≤ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version
DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or V_{IL} (Max)	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−122		−65	mA	Inputs Open	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2, 3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	*Figures 1, 3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	*Figures 1, 3*	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.70	0.70	1.70	0.70	1.80	ns	CP_n, CP_C =L	*Figures 1, 4*
t_{PLH} t_{PHL}		0.70	2.00	0.70	2.00	0.70	2.00	ns	CP_n, CP_C = H	*Figures 1, 4*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.60	1.10	2.60	1.10	2.60	ns	CP_n, CP_C = L	*Figures 1, 4*
t_{PLH} t_{PHL}		1.10	2.80	1.10	2.80	1.10	2.80	ns	CP_n, CP_C = H	*Figures 1, 4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1, 3, 4*	

DIP AC Electrical Characteristics (Continued)

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_S	Setup Time								*Figure 5*
	D_n	0.40		0.40		0.40			
	CD_n, SD_n (Release Time)	1.30		1.30		1.30		ns	*Figure 4*
	MS, MR (Release Time)	2.30		2.30		2.30			
t_H	Hold Time D_n	0.5		0.5		0.7		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3, 4*

SOIC, PCC and Cerpak AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 2, 3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	*Figures 1, 3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.50	0.70	1.50	0.70	1.60	ns	CP_n, CP_C =L	*Figures 1, 4*
t_{PLH} t_{PHL}		0.80	1.80	0.70	1.80	0.70	1.80		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.10	2.60	1.10	2.60	1.10	2.60		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1, 3, 4*	
t_S	Setup Time								*Figure 5*	
	D_n	0.30		0.30		0.30				
	CD_n, SD_n (Release Time)	1.20		1.20		1.20		ns	*Figure 4*	
	MS, MR (Release Time)	2.20		2.20		2.20				
t_H	Hold Time D_n	0.5		0.5		0.7		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3, 4*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.40	0.75	1.40	0.80	1.50	ns	*Figures 1, 3* PCC Only	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	1.40	0.75	1.40	0.80	1.50	ns		

SOIC, PCC and Cerpak AC Electrical Characteristics (Continued)

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay CD$_n$, SD$_n$ to Output	0.70	1.50	0.70	1.50	0.80	1.60	ns	CP$_n$, CP$_C$ =L PCC Only	*Figures 1, 4*
t_{PLH} t_{PHL}		0.80	1.70	0.80	1.70	0.80	1.80		CP$_n$, CP$_C$ = H PCC Only	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.00	1.10	2.00	1.20	2.10	ns	CP$_n$, CP$_C$ = L PCC Only	
t_{PLH} t_{PHL}		1.20	2.10	1.20	2.10	1.30	2.20		CP$_n$, CP$_C$ = H PCC Only	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Common Clock to Output Path		100		100		100	ps	PCC Only (Note 4)	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation CP$_n$ to Output Path		235		235		235	ps	PCC Only (Note 4)	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Common Clock to Output Path		120		120		120	ps	PCC Only (Note 4)	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation CP$_n$ to Output Path		275		275		275	ps	PCC Only (Note 4)	
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Common Clock to Output Path		125		125		125	ps	PCC Only (Note 4)	
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation CP$_n$ to Output Path		265		265		265	ps	PCC Only (Note 4)	
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Common Clock to Output Path		90		90		90	ps	PCC Only (Note 4)	
t_{ps}	Maximum Skew Pin (Signal) Transition Variation CP$_n$ to Output Path		90		90		90	ps	PCC Only (Note 4)	

Note 4: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Industrial Version

PCC DC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = –40°C to +85°C (Note 5)

Symbol	Parameter	T_C = –40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	–1085	–870	–1025	–870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	–1830	–1575	–1830	–1620	mV	or V_{IL} (Min)	50Ω to –2.0V
V_{OHC}	Output HIGH Voltage	–1095		–1035		mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage		–1565		–1610	mV	or V_{IL} (Max)	50Ω to –2.0V
V_{IH}	Input HIGH Voltage	–1170	–870	–1165	–870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1830	–1480	–1830	1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		0.5		μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		300		240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	–122	–60	–122	–65	mA	Inputs Open	

Note 5: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = –40°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		400		400		MHz	*Figures 2, 3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	*Figures 1, 3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.60	1.50	0.70	1.50	0.70	1.60	ns	CP_n, CP_C = L	*Figures 1, 4*
t_{PLH} t_{PHL}		0.70	1.80	0.70	1.80	0.70	1.80		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.10	2.60	1.10	2.60	1.10	2.60		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.35	1.10	0.35	1.10	ns	*Figures 1, 3, 4*	
t_S	Setup Time								*Figure 5*	
	D_n	1.00		0.30		0.30				
	CD_n, SD_n (Release Time)	1.50		1.20		1.20		ns	*Figure 4*	
	MS, MR (Release Time)	2.50		2.20		2.20				
t_H	Hold Time D_n	0.7		0.5		0.7		ns	*Figure 5*	
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3, 4*	

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	(Notes 6, 7, 8)
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	(Notes 6, 7, 8)
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for all Inputs		(Notes 6, 7, 8, 9)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for all Inputs		(Notes 6, 7, 8, 9)
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 6, 7, 8)
I_{IH}	Input HIGH Current		240	µA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		(Notes 6, 7, 8)
			340	µA	−55°C			
I_{EE}	Power Supply Current	−130	−50	mA	−55°C to +125°C	Inputs Open		(Notes 6, 7, 8)

Note 6: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 7: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2, 3, 7 and 8.

Note 8: Sampled tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7 and 8.

Note 9: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions		Notes
		Min	Max	Min	Max	Min	Max				
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 2, 3*		(Note 13)
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	*Figures 1, 3*		(Notes 10, 11, 12)
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	*Figures 1, 3*		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	CP_n, CP_C = L	*Figures 1, 4*	
t_{PLH} t_{PHL}		0.50	2.40	0.60	2.10	0.50	2.50		CP_n, CP_C = H		
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	0.70	2.70	0.80	2.60	0.80	2.90	ns	CP_n, CP_C = L		
t_{PLH} t_{PHL}		0.70	2.90	0.80	2.80	0.80	3.10		CP_n, CP_C = H		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20	1.40	ns	*Figures 1, 3, 4*		
t_s	Setup Time D_n	1.00		0.80		0.90			*Figure 5*		(Note 13)
	CD_n, SD_n (Release Time) MS, MR (Release Time)	1.50 2.50		1.30 2.30		1.60 2.50		ns	*Figure 4*		
t_h	Hold Time D_n	1.50		1.30		1.60		ns	*Figure 5*		
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3, 4*		

Note 10: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 11: Screen tested 100% on each device at +25°C. Temperature only, Subgroup A9.

Note 12: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 and A11.

Note 13: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuits

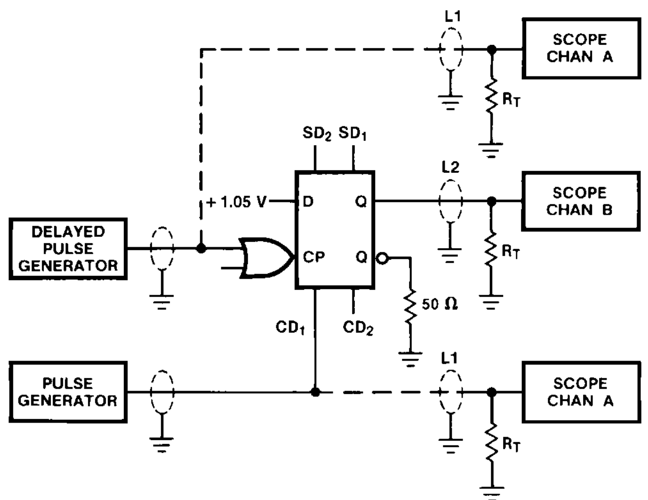
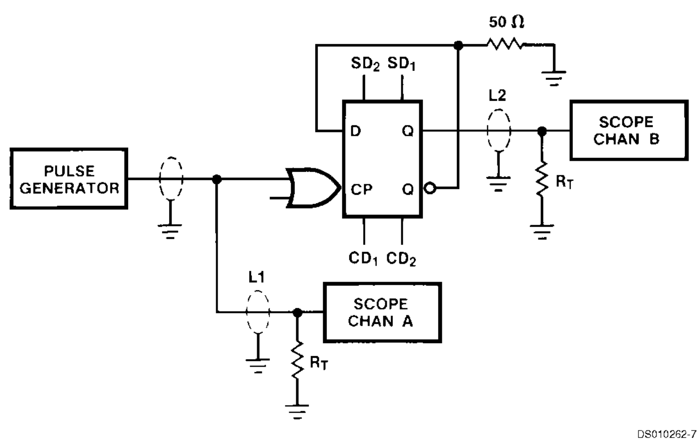


FIGURE 1. AC Test Circuit



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = Equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms

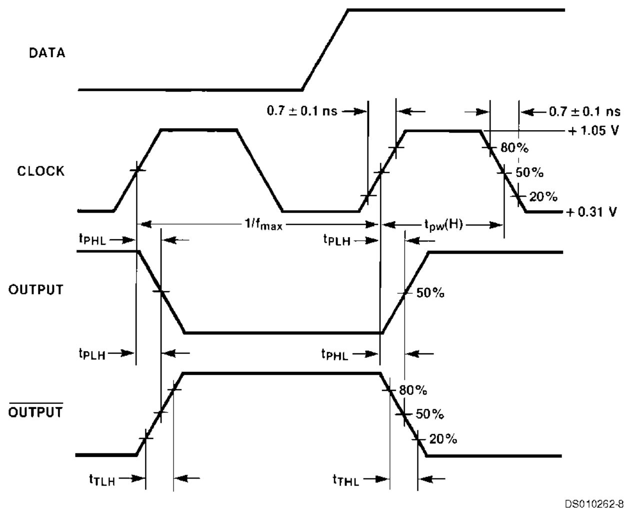


FIGURE 3. Propagation Delay (Clock) and Transition Times

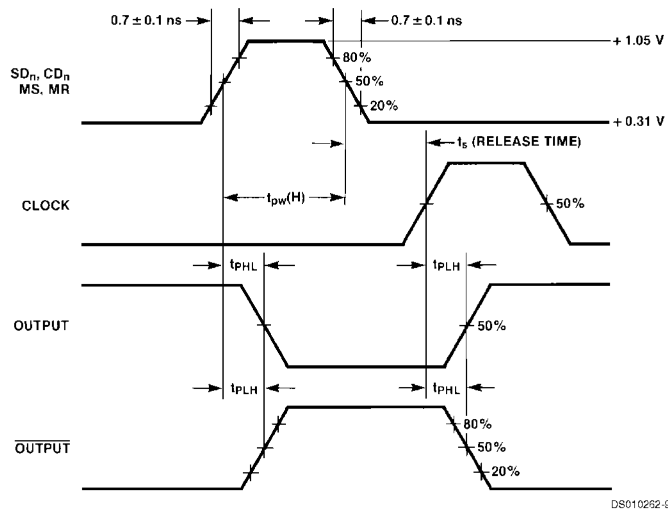


FIGURE 4. Propagation Delay (Resets)

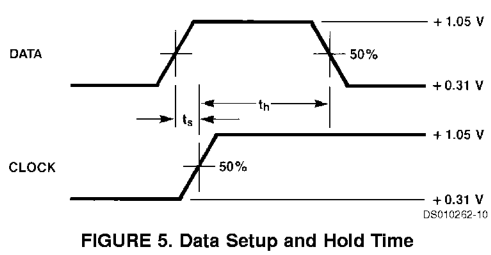


FIGURE 5. Data Setup and Hold Time

Note 14: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 15: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

100331 D C QB

Device Type (Basic) — 100331

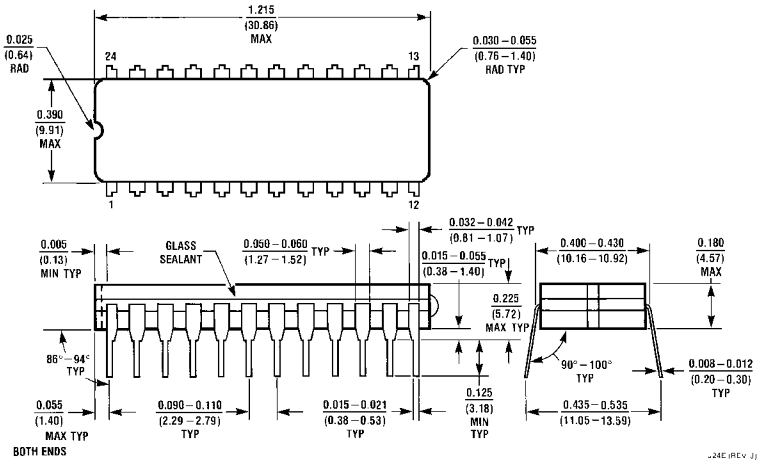
Package Code — D
- D = Ceramic DIP
- F = Quad Cerpak
- Q = Plastic Leaded Chip Carrier (PCC)
- P = Plastic DIP
- S = Small Outline (SOIC)

Temperature Range — C
- C = Commercial (0°C to +85°C)
- I = Industrial (−40°C to +85°C) (PCC Only)
- M = Military (−55°C to +125°C)

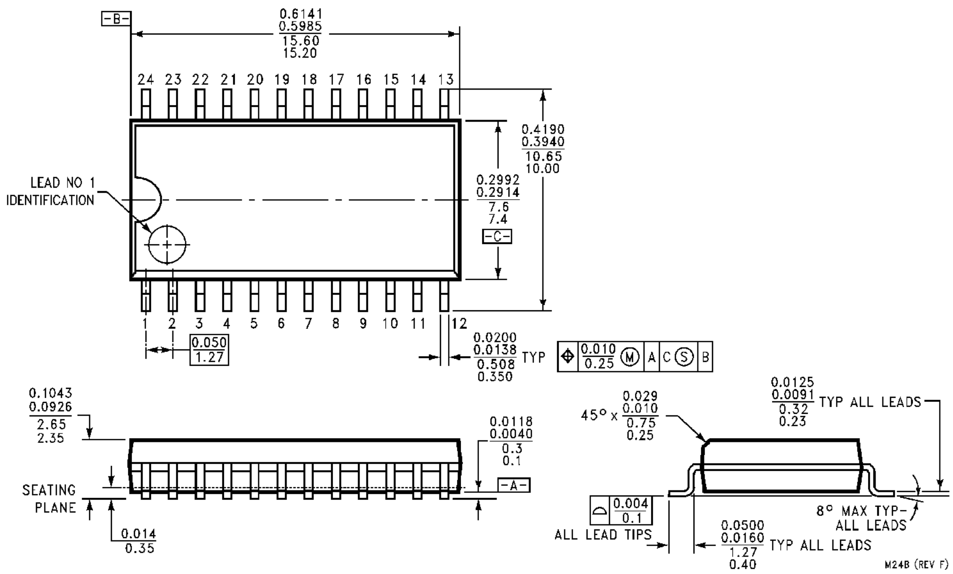
Special Variation — QB
- QB = Military grade device with environmental and burn-in processing.

DS010262-11

Physical Dimensions inches (millimeters) unless otherwise noted

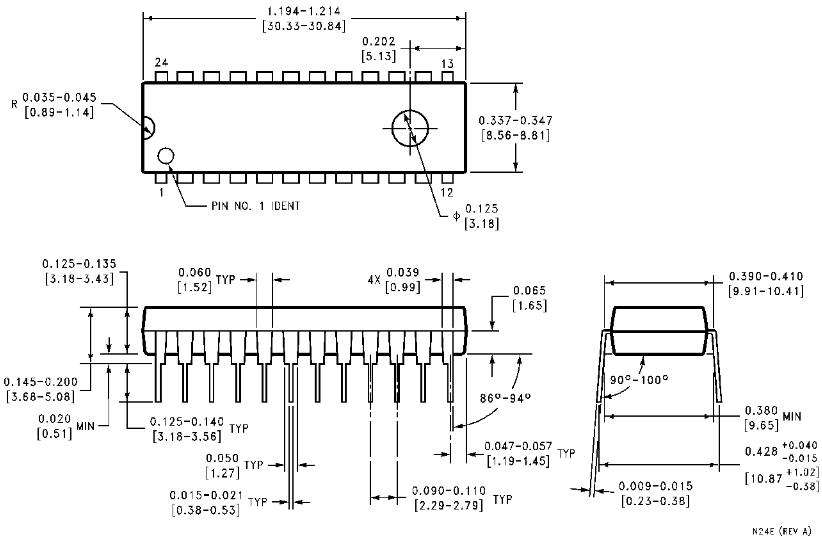


24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
Package Number J24E

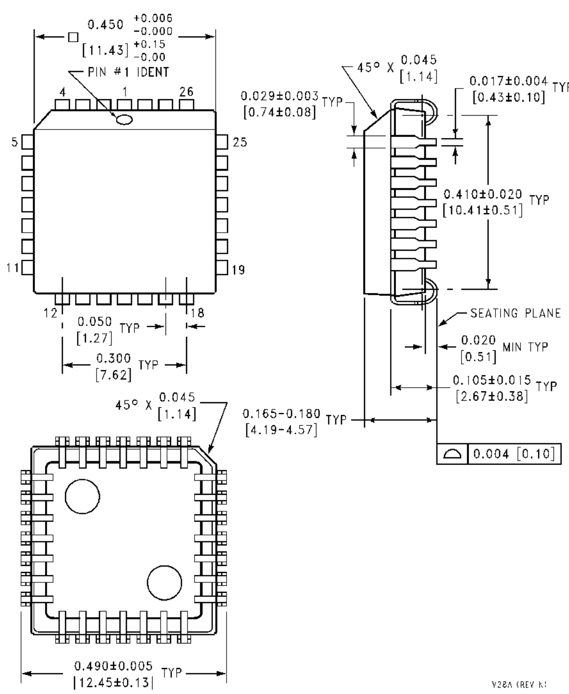


24-Lead Molded Package (0.300" Wide) (S)
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

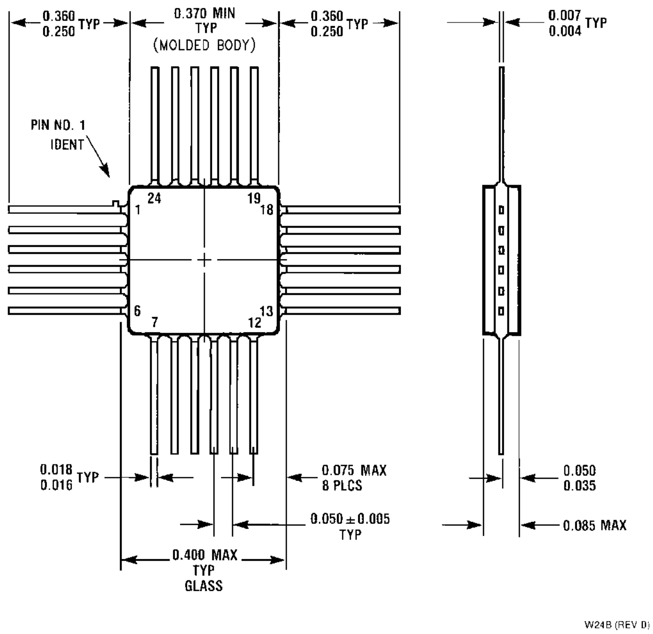


24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E



28-Lead Plastic Chip Carrier (Q)
Package Number V28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Quad Cerpak (F)
Package Number W24B

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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