Intel® Curie™ Module

Datasheet

March 2017

Document rev. 1.3

The Intel® Curie™ module is a hardware product offering design flexibility in a small form factor. This complete, low-power solution comes with compute, motion sensor, Bluetooth® low energy, battery-charging, and pattern matching capabilities for optimized analysis of sensor data—enabling quick and easy identification of actions and motions.

Intel® Quark™ SE Microcontroller C1000 Processor Core

- x86 ISA-compatible CPU
- 32 MHz clock, 32-bit address bus
- 8 kB 2-way L1 instruction cache
- 1.33 DMIPs/MHz, total of 42.56 DMIPs max.

Sensor Subsystem

- ARC* EM4 DSP core with floating point unit
- 8 kB L1 instruction cache, 8 kB data CCM
- Tightly coupled IO to interface sensors/actuators
- 1.4 DMIPS/MHz

Pattern Recognition Accelerator

- Built-in Neuron nodes
- K-Nearest Neighbors (k-NN) and Radial Basis Functions (RBF)

Sensor Subsystem Interfaces

- Two I²C master with standard and fast modes
- Two SPI master up to 16 MHz clock with 4 chip selects
- 19 channel 12-bit ADC
- 16 GPIOs
- Two timers

Power Management

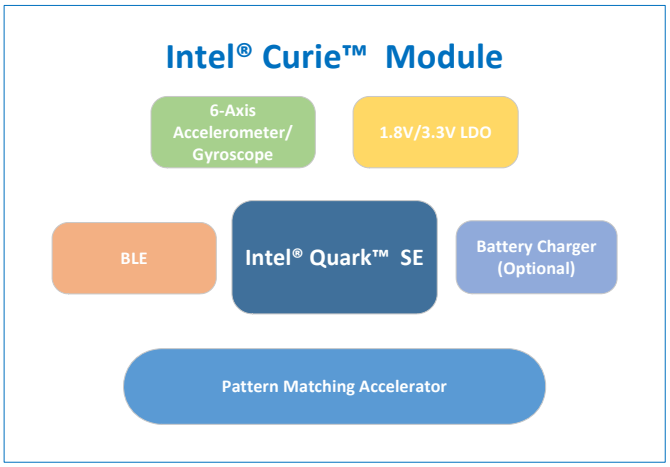
- SoC states: Active, Sleep and Off
- Sensor subsystem: Sensing active, sensing wait and sensing standby
- Platform power DC-DC 1.8 V, 3.3 V

Memory

- 384 kB Flash +8 kB OTP Flash
- 80 kB SRAM

Thermals

- -25 to 70°C operating range



Security

- Secure boot and update
- Isolated SRAM regions
- Flash (NVM) read/write access

Host Interfaces

- USB 1.1 FS device
- Two I²C master/slave with standard, fast & fast mode plus
- Two SPI master up to 16MHz clock with 4 chip selects
- One SPI slave
- Two UARTs, 300 kBaud to 2 MBaud
- Four timers
- Four PWM
- I²S with sample size from 12 to 32-bit
- 32 GPIOs
- 19 comparators

Clock

- 32 kHz and 32 MHz crystal oscillators
- 32 MHz oscillator
- 32 kHz RTC and AON counters/timers
- control

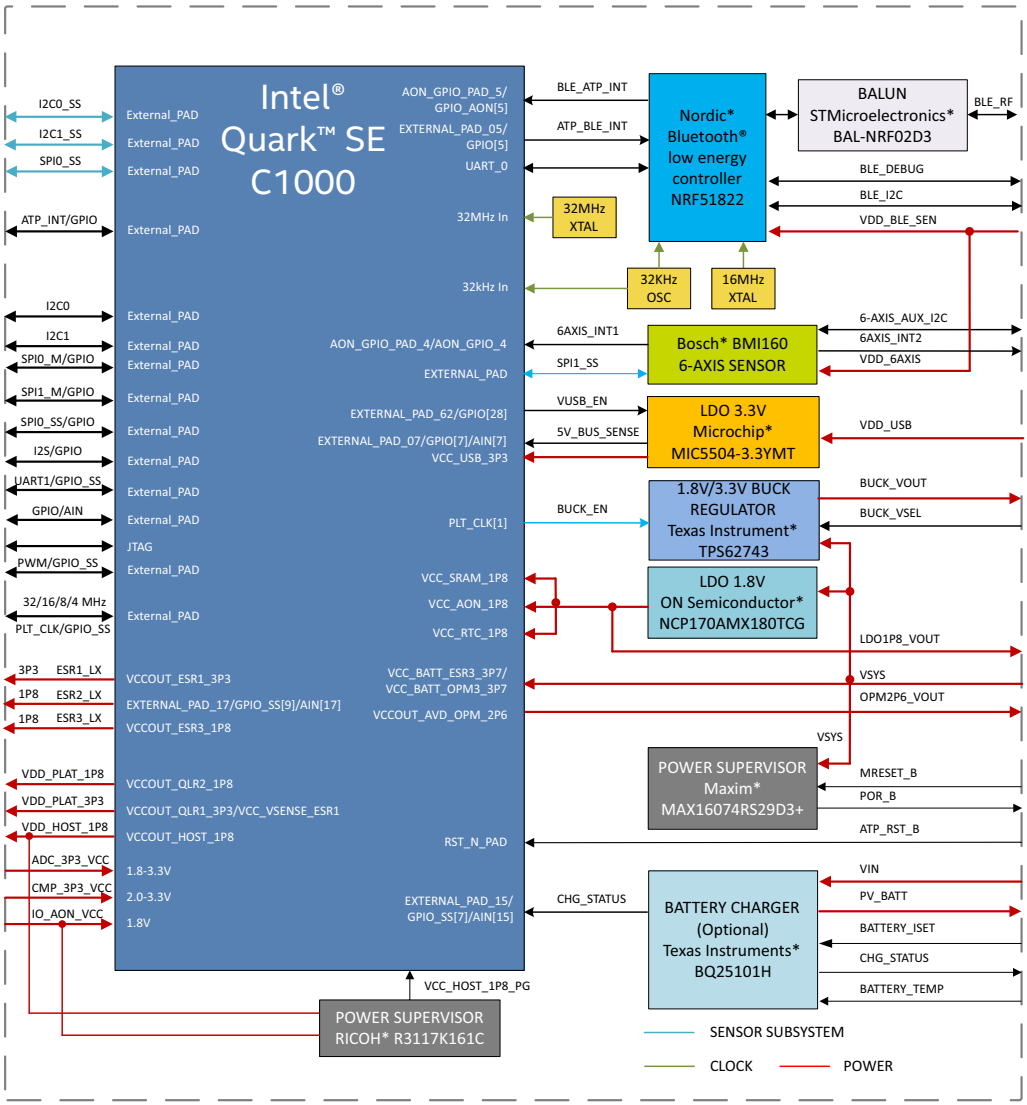
Hardware Reference Designs

Intel has multiple reference designs available through select partners and ODMs. One reference design for the maker community, for example, is the Arduino 101* (branded Genuino 101* in some countries) board which can be used for quick prototyping of concepts. It has the same pin configuration as the Arduino UNO, making it compatible with the majority of components in the Arduino community.

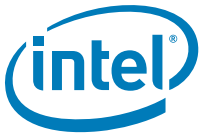
Intel Software Platform

Intel offers several software solutions for the Intel® Curie™ module. These include an open source solution designed to assist developers by increasing the speed and ease of development for a wide variety of products. The Intel® Curie™ Open Developer Kit (ODK) provides access to software, firmware, and services needed for a variety of use cases. The software platform affords more flexibility to the developers to build with multiple environments and the capability to integrate into different IDEs.

Intel® Curie™ Module Block Diagram



For more information, please visit: http://www.intel.com/curie



Content

About This Datasheet 11
- Intel® Curie™ module 11
- Intended audience 11
- Resources, references and terminology 11

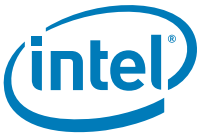
1 Ball Map and Pin Definitions 12
1.1 Module physical bump map 12
1.2 Module-to-SoC mapping table 13
1.3 Pin definitions 19
1.3.1 Battery and power management pins 19
1.3.2 Platform buck converter pins 20
1.3.3 Additional buck converter pins 20
1.3.4 Reference voltage pins 21
1.3.5 Module ground pins 21
1.3.6 Reset pins 21
1.3.7 Debugging pins 22
1.3.8 Wake-capable interrupt pins 22
1.3.9 Clock out pin 23
1.3.10 GPIO pin mapping 23
1.3.11 6-Axis sensing device pins 26
1.3.12 Bluetooth® low energy controller pins 27
1.3.13 I^2C interface pins 27
1.3.14 I^2S interface pins 28
1.3.15 Pulse width modulator (PWM) pins 28
1.3.16 SPI master pin out 29
1.3.17 SPI slave pin out 30
1.3.18 UART interface pins 30
1.3.19 USB interface pins 30
1.3.20 ADC pins 31

2 Specifications 32
2.1 Electrical characteristics 32
2.1.1 Absolute maximum and minimum voltages 32
2.1.2 Operating maximum and minimum voltages 32
2.1.3 DC operating specifications 33
2.1.4 Operating temperature range 35
2.1.5 ESD considerations 35
2.2 Power and timing considerations 35
2.2.1 Power architecture 35
2.2.2 Primary power 36
2.2.3 Optional platform power 36
2.2.4 Device power states 37
2.2.5 Intel® Quark™ SE microcontroller C1000 power states 38
2.2.6 Boot and reset sequences 38
2.2.7 Platform power distribution 43
2.2.8 Current draw (typical) 43
2.3 Clocking 45
2.4 BLE (Bluetooth® low energy) 46

3 Detailed Description 47
3.1 Block diagram 48
3.2 Features 49
3.2.1 Processor cores 49
3.2.2 Memory subsystem 49

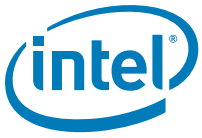
3.2.3 Six-axis accelerometer/gyroscope 49
3.2.4 Bluetooth® low energy integration 50
3.2.5 Pattern matching engine 51
3.2.6 USB device 51
3.2.7 I²C 52
3.2.8 I²S 52
3.2.9 UART 52
3.2.10 SPI 53
3.2.11 DMA controller 53
3.2.12 GPIO subsystem 54
3.2.13 Timers and pulse width modulator (PWM) 55
3.2.14 Analog comparators 55
3.2.15 Watchdog timer (WDT) 55
3.2.16 Real-time clock (RTC) 55
3.2.17 Analog-to-digital converter (ADC) unit 56
3.2.18 Interrupt 56
3.2.19 Power management 57
3.2.20 Clock management 58
3.2.21 Test and debug 58
3.3 Bluetooth® low energy controller 59
3.3.1 Power 59
3.3.2 Clock 60
3.3.3 Interfaces 60
3.3.4 2.4 GHz radio 60
3.3.5 Signals 61
3.3.6 Software stack support 61
3.3.7 Programming and debug 62
3.4 Sensor device 62
3.4.1 Feature summary 62
3.4.2 Power 63
3.4.3 Sensor timing 64
3.4.4 Data synchronization 64
3.4.5 Data processing 64
3.4.6 FIFO 64
3.4.7 Interfaces 65
3.4.8 Interrupt management 65
3.4.9 Signals 66
3.4.10 Sensor position on Intel® Curie™ module 67
3.5 Memory 68
3.5.1 Memory map 68
4 Reference and Resources 69
4.1 Software support 69
4.2 Related documents 69
4.3 Intel® Curie™ module-related community resources 69
4.4 Component reference 69
4.5 Terminology 70
5 Packaging and Ordering 72
5.1 Package information 72
5.1.1 Packing geometry 72
5.1.2 Package marking 73
5.2 Ordering information 73
5.3 Storage information 74
6 Manufacturing Information 75

6.1 Bootloader information 75
6.2 PCB pad design guidelines 75
6.3 Manufacturing guidelines 77
6.3.1 SMT reflow parameters 77
6.3.2 Board rework 78
6.4 General handling recommendations 79



Tables

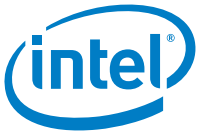
1-1 Module ball /pin map 12
1-2 Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping 13
1-3 Battery and power management pins 19
1-4 Platform buck converter pins 20
1-5 Additional buck converter pins 20
1-6 Reference voltages on module 21
1-7 Ground pins 21
1-8 Reset pins 21
1-9 Debugging pins 22
1-10 Intel® Quark™ SE microcontroller C1000 always-on wake capable interrupt pins 22
1-11 Clock out pin 23
1-12 GPIO/analog input pins 23
1-13 GPIO/AON/INT 24
1-14 GPIO/multifunction lines 24
1-15 Internal GPIO signals 26
1-16 Six-axis interface pins 26
1-17 Bluetooth® low energy controller interface pins 27
1-18 I^2C interface pins 27
1-19 I^2S interface pins 28
1-20 PWM output pins 28
1-21 SPI master pins 29
1-22 SPI slave pins 30
1-23 UART Interface pins 30
1-24 USB Interface pins 30
1-25 Intel® Curie™ module external pins connected to Intel® Quark™ SE microcontroller ADC interface pins 31
1-26 Intel® Quark™ SE microcontroller ADC interface multifunction pins connected to Intel® Curie™ module external pins 31
2-1 Absolute min-max specifications for the Intel® Quark™ SE microcontroller C1000 32
2-2 Operating Min - Max specifications for the Intel® Curie™ module 32
2-3 AON_IO_VCC=3.3 VDC 33
2-4 AON_IO_VCC=1.8V 33
2-5 ADC - DC I/O specifications 34
2-6 Comparator voltage range 34
2-7 USB I/O - DC specifications 34
2-8 USB IO AC specifications 35
2-9 Intel® Curie™ module component ESD data 35
2-10 ESR requirements 37
2-11 Maximum current range 37
2-12 Power-up sequence parameters 41
2-13 Power rail maximum current output 43
2-14 Intel® Curie™ module power consumption: idle - without motion sensing 43
2-15 Intel® Curie™ module power consumption: idle - motion sensing without movement 44
2-16 Intel® Curie™ module power consumption: Bluetooth® low energy fast advertising at 100ms - without motion sensing 44
2-17 Intel® Curie™ module power consumption: Bluetooth® low energy connection at 150 ms - without motion sensing 45
2-18 Dhrystone 2.1 results: without motion sensing 45
2-19 Clock sources 45
3-1 Intel® Curie™ module system clocks 58



2 Bluetooth® low energy controller signals 61
3 Bosch* BMI260 6-axis Sensing Device Signals 66
4-1 Terminology 70
5-1 Module package details 72
5-2 Package marking 73
5-3 Ordering information for Intel® Curie™ module 73
5-4 Package storage specifications 74
6-1 SMT reflow parameters 77
6-2 Rework reflow parameter recommendations 78

Figures

2-1 Power supervisor 40
2-2 Power state change diagram 40
2-3 Power rail timing sequence 41
2-4 Timing relationship between VIN, OPM2P6_VOUTand LDO1P8_VOUT 42
2-5 Timing relationship between LDO1P8_VOUT, VDD_HOST_1P8 and VDD_HOST_1P8-PG 42
3-1 Intel® Curie™ module block diagram 48
3-2 Intel® Curie™ module X-Y dimensions and position of the six-axis sensor 67
5-1 Package marking 73
6-1 PCB pad layout 75
6-2 Metal-defined pad 76
6-3 General handling recommendations 79



Revision History

Revision	Description	Date
1.0	Initial release.	August 2016
1.1	Reorganized the content into the existing chapters and renamed some chapters. Updated the list of reference documents. Added sections about Manufacturing Information, Ordering information, Package marking, and ESD considerations. Updated Table 1-9 to remove external pull-up/pull-down recommendation for JTAG signals.	October 2016
1.2	Added reference to *Intel® Curie™ Power Sequence Considerations* application note in the Power and timing considerations section of the Specifications chapter.	November 2016
1.21	Minor fixes.	December 2016
1.3	Restructured and expanded the content of chapters "Ball Map and Pin Definitions", "Specifications", and "Detailed Description". Also updated the content of the front cover.	March 2017

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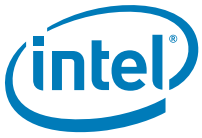


About This Datasheet

This section introduces the Intel® Curie™ module. It covers:

- Intel® Curie™ module
- Intended audience
- Resources, references and terminology

Intel® Curie™ module

This datasheet documents the Intel® Curie™ module, an advanced device built around the Intel® Quark™ SE microcontroller C1000, integrating compute, sense, awareness, connectivity and a programmable input/output controller within a common package.[1] See Chapter 3, "Detailed Description", for more descriptive details.

Intended audience

This datasheet is intended to provide detailed technical information about the Intel® Curie™ module to the vendors, system integrators, and other engineers and technicians who need this level of information.

Resources, references and terminology

See Chapter 4, "Reference and Resources" for information on Software support, Related documents, and Intel® Curie™ module-related community resources as well as Component reference and a list of Terminology.

1. Note that this module is not a FCC-certified module. Emission testing has been performed and designs based on the Intel® Curie™ module that have FCC certification are available, but all new designs based on the module require regulatory approval prior to public availability.

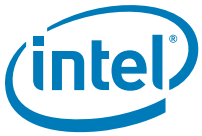
1 Ball Map and Pin Definitions

1.1 Module physical bump map

Table 1-1 shows a map of the module pin out map as a top view into the part.

Table 1-1. Module ball / pin map

	1	2	3	4						21	22	23	24
A	NO BALL	ATP_GND1	I2S_RXD	SPI0_M_CS1						6AXIS_SDA	6AXIS_SCL	6AXIS_INT2	ATP_GND1
B	I2S_RWS	I2S_RSCK	SPI0_M_CS0	ATP_RST_B						SPI1_M_CS2	SPI1_M_MISO	BLE_SDA	BT_GPIO
C	I2S_TWS	I2S_TSCK	SPI0_M_CS2	SPI0_M_SCK						SPI1_M_SCK	SPI1_M_CS3	ATP_GND1	GPIO/AIN_14
D	I2S_TXD	I2C1_SDA	SPI0_M_MOSI	SPI0_M_MISO						SPI1_M_CS1	SPI1_M_CS0	MRESET_B	BLE_SW_CLK
E	I2C1_SCL	I2C1_SS_SDA	PLT_CLK_0	ATP_SPI_S_SCK						AON_IO_VCC	SPI1_M_MOSI	POR_B	BLE_SWDIO
F	I2C1_SS_SCL	PWM3_OUT	ATP_SPI_S_CS	ATP_SPI_S_MOSI						ATP_INT3	ATP_INT0	BLE_SCL	BLE_RF
G	PWM2_OUT	PWM1_OUT	ATP_SPI_S_MISO	SPI0_SS_CS3						ATP_GND1	COMP_AREF	BLE_DEC2	ATP_GND1
H	PWM0_OUT	GPIO/AIN_12	SPI0_SS_CS1	SPI0_SS_CS0						GPIO/AIN_11	CMP_3P3_VCC	ADC_3P3_VCC	VDD_BLE_SEN
J	AVD_OPM_2P6	GPIO/AIN_10	SPI0_SS_MISO	SPI0_SS_SCK						UART1_TX	UART1_CTS	USB_DM	USB_DP
K	BUCK_VOUT	BUCK_VSEL	SPI0_SS_CS2	VDD_USB						UART1_RTS	UART1_RX	ATP_TRST_B	VIN[1]
L	LDO1P8_VOUT	GPIO/AIN_13	ATP_INT2	VSYS						ATP_ADC_AGND	BATT_ISET	ATP_TCK	ATP_TMS
M	PV_BATT	VDD_PLAT_1P8	SPI0_SS_MOSI	ESR2_LX						ATP_TDI	CHG_STATUS	ATP_TDO	I2C0_SCL
N	ESR1_LX	VDD_PLAT_3P3	ATP_INT1	ESR2_VBATT						VIN[2]	BATT_TEMP	I2C0_SS_SDA	I2C0_SS_SCL
P	ATP_GND1	ESR1_VBATT	VDD_HOST_1P8	ESR3_LX						SW_FG_VBATT	ATP_GND1	I2C0_SDA	ATP_GND1



1.2 Module-to-SoC mapping table

The Intel® Curie™ module is based on the Intel® Quark™ SE microcontroller C1000. Some of the microcontroller signals are used internally within the module to operate the integrated Bosch* BMI160 six-axis sensor, the battery charger and the Nordic* nRF51822 Bluetooth® low energy controller, while other SoC signals are routed directly to the module interface.

Table 1-2 provides the list of high-level reference mapping signals between the Intel Quark microcontroller core and the Intel Curie module. It also includes, where available, alternate functions that interface pins can be configured for.

Consult the Intel® Quark™ SE microcontroller C1000 datasheet for additional information on specific microcontroller functions and registers.

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
A1	No Ball	-	-	-	-	-
A2	ATP_GND1[3]	ATP_GND1[3]	VSS3	ATP_GND1	VSS	F3
A3	I2S_RXD	I2S_RXD	GPIO[15]	I2S_RXD	EXTERNAL_PAD_49	B8
A4	SPI0_M_CS1	SPI0_M_CS_B[1]	GPIO[25]	SPI0_M_CS_B[1]	EXTERNAL_PAD_59	A10
A21	6AXIS_SDA	6AXIS_SDA	ASDX (6AXIS / 2)	-	6AXIS I^2C to external magnetometer to get 9AXIS	-
A22	6AXIS_SCL	6AXIS_SCL	ASCX (6AXIS / 3)	-		-
A23	6AXIS_INT2	6AXIS_INT2	INT2 (6AXIS / 9)	-	6AXIS Interrupt to external magnetometer to get 9AXIS	-
A24	ATP_GND1[9]	ATP_GND1[9]	VSS9	ATP_GND1	VSS	M1
B1	I2S_RWS	I2S_RWS	GPIO[17]	I2S_RWS	EXTERNAL_PAD_51	B9
B2	I2S_RSCK	I2S_RSCK	GPIO[16]	I2S_RSCK	EXTERNAL_PAD_50	A8
B3	SPI0_M_CS0	SPI0_M_CS_B[0]	GPIO[24]	SPI0_M_CS_B[0]	EXTERNAL_PAD_58	E8
B4	ATP_RST_B	RST_B	RST_B		RST_N_PAD	F11
B21	SPI1_M_CS2	SPI1_M_CS_B[2]	GPIO[13]	SPI1_M_CS_B[2]	EXTERNAL_PAD_47	B07
B22	SPI1_M_MISO	SPI1_M_MISO	GPIO[9]	SPI1_M_MISO	EXTERNAL_PAD_43	D6
B23	BLE_SDA	BLE P0_31 / E8	-	-	BLE I^2C to external device optional	-
B24	BT_GPIO	BLE P0_18 / H1	-	-	BLE GPIO to external device optional	-
C1	I2S_TWS	I2S_TWS	GPIO[19]	I2S_TWS	EXTERNAL_PAD_53	C9
C2	I2S_TSCK	I2S_TSCK	GPIO[18]	I2S_TSCK	EXTERNAL_PAD_52	A9
C3	SPI0_M_CS2	SPI0_M_CS_B[2]	GPIO[26]	SPI0_M_CS_B[2]	EXTERNAL_PAD_60	B10
C4	SPI0_M_SCK	SPI0_M_SCK	GPIO[21]	SPI0_M_SCK	EXTERNAL_PAD_55	D8

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
C21	SPI1_M_SCK	SPI1_M_SCK	GPIO[8]	SPI1_M_SCK	EXTERNAL_PAD_42	C6
C22	SPI1_M_CS3	SPI1_M_CS_B[3]	GPIO[14]	-	EXTERNAL_PAD_48	A7
C23	ATP_GND1[5]	ATP_GND1[5]	VSS5	ATP_GND1	VSS	L12
C24	GPIO/AIN_14	GPIO_SS[6]	GPIO_SS[6]	AIN[14]	EXTERNAL_PAD_14	F01
D1	I2S_TXD	I2S_TXD	GPIO[20]	I2S_TXD	EXTERNAL_PAD_54	D9
D2	I2C1_SDA	I2C1_SDA	I2C1_SDA	-	EXTERNAL_PAD_23	D2
D3	SPI0_M_ MOSI	SPI0_M_MOSI	GPIO[23]	SPI0_M_MOSI	EXTERNAL_PAD_57	E9
D4	SPI0_M_ MISO	SPI0_M_MISO	GPIO[22]	SPI0_M_MISO	EXTERNAL_PAD_56	E7
D21	SPI1_M_CS1	SPI1_M_CS_B[1]	GPIO[12]	SPI1_M_CS_ B[1]	EXTERNAL_PAD_46	C7
D22	SPI1_M_CS0	SPI1_M_CS_B[0]	GPIO[11]	SPI1_M_CS_ B[0]	EXTERNAL_PAD_45	D7
D23	MRESET_B	MR (MAX16074 / B2)	-	-	-	-
D24	BLE_SW_CLK	SWDCLK (BLE / H2)	GPIO[27]	SPI0_M_CS_ B[3]	EXTERNAL_PAD_61	C10
E1	I2C1_SCL	I2C1_SCL	-	-	EXTERNAL_PAD_22	D1
E2	I2C1_SS_ SDA	I2C1_SS_SDA	-	-	EXTERNAL_PAD_26	B3
E3	PLT_CLK_0	PLT_CLK[0]	GPIO_SS[14]	PLT_CLK[0]	EXTERNAL_PAD_67	D12
E4	ATP_SPI_S_ SCK	SPI_S_SCK	GPIO[2]	AIN[2]/ SPI_S_SCK	EXTERNAL_PAD_02	H5
E21	AON_IO_VCC	AON_IO_VCC	VCC_IO_AON1	VCC_IO_AON1	VCC_IO_AON1	A11
			VCC_IO_AON2	VCC_IO_AON2	VCC_IO_AON2	G6
E22	SPI1_M_ MOSI	SPI1_M_MOSI	GPIO[10]	SPI1_M_MOSI	EXTERNAL_PAD_44	E6
E23	POR_B	RESETN (MAX16074 / B1)	-	-	Power supervisory Power On Reset output	-
E24	BLE_SWDIO	SWDIO (BLE/J2)	GPIO[6]	AIN[6]	EXTERNAL_PAD_06	H4
F1	I2C1_SS_SCL	I2C1_SS_SCL	I2C1_SS_SCL	-	EXTERNAL_PAD_27	A3
F2	PWM3_OUT	PWM[3]	GPIO_SS[13]	PWM[3]	EXTERNAL_PAD_66	B11
F3	ATP_SPI_S_ CS	SPI_S_CS_B	GPIO[0]	AIN[0] / SPI_S_CS_B	EXTERNAL_PAD_00	F2
F4	ATP_SPI_S_ MOSI	SPI_S_MOSI	GPIO[3]	AIN[3] / SPI_S_MOSI	EXTERNAL_PAD_03	J6
F21	ATP_INT3	ATP_INT3	GPIO_AON[3]	-	AON_GPIO_PAD_3	F9
F22	ATP_INT0	ATP_INT0	GPIO_AON[0]	-	AON_GPIO_PAD_0	G9
F23	BLE_SCL	BLE P0_30 / D8		-	BLE I^2C to external device optional	-
F24	BLE_RF	BALUN SE / A1	-	-	Antenna Micro Strip (50 ohms)	-

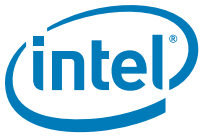


Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
G1	PWM2_OUT	PWM[2]	GPIO_SS[12]	PWM[2]	EXTERNAL_PAD_65	C11
G2	PWM1_OUT	PWM[1]	GPIO_SS[11]	PWM[1]	EXTERNAL_PAD_64	D11
G3	ATP_SPI_S_MISO	SPI_S_MISO	GPIO[1]	AIN[1]	EXTERNAL_PAD_01	G4
G4	SPI0_SS_CS3	SPI0_SS_CS_B[3]	GPIO[30]	SPI0_SS_CS_B[3]	EXTERNAL_PAD_34	A4
G21	ATP_GND1[7]	ATP_GND1[7]	VSS7	ATP_GND1	VSS	M11
G22	COMP_AREF	COMP_AREF	COMP_AREF	-	COMP_AREF (or AREF_PAD)	F5
G23	BLE_DEC2	DEC2 (BLE / F1)	-	-	-	-
G24	ATP_GND1[6]	ATP_GND1[6]	VSS6	ATP_GND1	VSS	M12
H1	PWM0_OUT	PWM[0]	GPIO_SS[10]	PWM[0]	EXTERNAL_PAD_63	E10
H2	GPIO/AIN_12	GPIO_SS[4]	GPIO_SS[4]	AIN[12]	EXTERNAL_PAD_12	J04
H3	SPI0_SS_CS1	SPI0_SS_CS_B[1]	SPI0_SS_CS_B[1]	-	EXTERNAL_PAD_32	C4
H4	SPI0_SS_CS0	SPI0_SS_CS_B[0]	SPI0_SS_CS_B[0]	-	EXTERNAL_PAD_31	D4
H21	GPIO/AIN_11	GPIO_SS[3]	GPIO_SS[3]	AIN[11]	EXTERNAL_PAD_11	G1
H22	CMP_3P3_VCC	CMP_3P3_VCC	VCC_CMP_3P3[2]	-	VCC_CMP_3P3[2]	J3
			VCC_CMP_3P3[1]	-	VCC_CMP_3P3[1]	M2
H23	ADC_3P3_VCC	-	-	-	-	-
H24	VDD_BLE_SEN	-	-	-	-	-
J1	OPM2P6_VOUT	OPM2P6_VOUT	VCC_AVD_OPM_2P6	-	VCCOUT_AVD_OPM_2P6	K11
		AVD_OPM_2P6	VCCOUT_AVD_OPM_2P6	-		
		VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6	-	VCC_AVD_OPM_2P6	K12
		AVD_OPM_2P6		-		
J2	GPIO/AIN_10	GPIO_SS[2]	-	AIN[10]	EXTERNAL_PAD_10	K5
J3	SPI0_SS_MISO	SPI0_SS_MISO	SPI0_SS_MISO	-	EXTERNAL_PAD_28	C3
J4	SPI0_SS_SCK	SPI0_SS_SCK	SPI0_SS_SCK	-	EXTERNAL_PAD_30	D3
J21	UART1_TX	UART1_TX	GPIO_SS[8]	AIN[16]/ UART1_TXD	EXTERNAL_PAD_16	L4
J22	UART1_CTS	UART1_CTS	GPIO_SS[0]	AIN[8]/ UART1_CTS_B	EXTERNAL_PAD_08	L5
J23	USB_DM	USB_DM	USB_DN	-	USB_PADN	H2
J24	USB_DP	USB_DP	USB_DP	-	USB_PADP	H1

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
K1	BUCK_VOUT	BUCK_VOUT	-	-	-	-
K2	BUCK_VSEL	VSEL1,3 (TPS62743)	-	-	-	-
K3	SPI0_SS_CS2	SPI0_SS_CS2]	SPI0_SS_CS_B[2]	GPIO[29]	EXTERNAL_PAD_03	B4
K4	VDD_USB	VDD_USB	-	-	EXTERNAL_PAD_07	G3
K21	UART1_RTS	UART1_RTS	GPIO_SS[1]	AIN[9]/ UART1_RTS_B	EXTERNAL_PAD_09	M5
K22	UART1_RX	UART1_RX	GPIO_SS[9]	AIN[17]/ UART1_RXD	EXTERNAL_PAD_17	M4
K23	ATP_TRST_B	ATP_TRST_B	TRST_B	-	TRST_PAD	G5
K24	VIN[1]	VIN (BQ25101 / A2)	-	-	-	-
L1	LDO1P8_VOUT	LDO1P8_VOUT	VCC_AON_1P8[2]	-	VCC_AON_1P8	A2
			VCC_SRAM_1P8	-	VCC_SRAM_1P8	C8
			VCC_RTC_1P8	-	VCC_RTC_1P8	G10
			VCC_AON_1P8[1]	-	VCC_AON_1P8	J7
L2	GPIO/AIN_13	GPIO/AIN_13]	GPIO_SS[5]	AIN[13]	EXTERNAL_PAD_13	G2
L3	ATP_INT2	ATP_INT2	GPIO_AON[2]	-	AON_GPIO_PAD_2	E12
L4	VSYS	VSYS	VCC_BATT_OPM_3P7	-	VCC_BATT_OPM_3P7	L10
			VCC_BATT_ESR3_3P7	-	VCC_BATT_ESR3_3P7	M9
L21	ATP_ADC_AGND	ATP_ADC_AGND	VSS_ADC_AGND	-	VSS_ADC_AGND	L3
L22	BATT_ISET	BATT_ISET	-	-	-	-
L23	ATP_TCK	ATP_TCK	TCK	-	TCK_PAD	G7
L24	ATP_TMS	ATP_TMS	TMS	-	TMS_PAD	F6
M1	PV_BATT	OUT (BQ25101 / A1)	-	-	-	-
M2	VDD_PLAT_1P8	VDD_PLAT_1P8	VCCOUT_QLR2_1P8	-	VCCOUT_QLR2_1P8	J11
M3	SPI0_SS_MOSI	SPI0_SS_MOSI	SPI0_SS_MOSI	-	EXTERNAL_PAD_29	E3
M4	ESR2_LX	ESR2_LX	VCCOUT_ESR2_1P8	-	EXTERNAL_PAD_17	J12
M21	ATP_TDI	ATP_TDI	TDI	-	TDI_PAD	F4
M22	CHG_STATUS	CHGN (BQ25101 / C1)	GPIO_SS[7]	AIN[15]	EXTERNAL_PAD_15	J5
M23	ATP_TDO	ATP_TDO	TDO	-	TDO_PAD	F8
M24	I2C0_SCL	I2C0_SCL	I2C0_SCL	-	EXTERNAL_PAD_20	C1

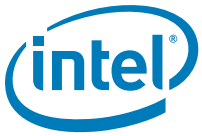
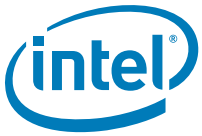


Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
N1	ESR1_LX	ESR1_LX	VCCOUT_ESR1_3P3	-	VCCOUT_ESR1_3P3	J8
N2	VDD_PLAT_3P3	VDD_PLAT_3P3	VCC_VSENSE_ESR1	-	VCC_VSENSE_ESR1	H9
			VCCOUT_QLR1_3P3	-	VCCOUT_QLR1_3P3	J9
N3	ATP_INT1	ATP_INT1	GPIO_AON[1]	-	AON_GPIO_PAD_1	E11
N4	ESR2_VBATT	ESR2_VBATT	VCC_BATT_ESR2_3P7	-	VCC_BATT_ESR2_3P7	L11
N21	VIN[2]	VIN (BQ25101 / A2)	-	-	-	-
N22	BATT_TEMP	TSN (BQ25101 / B1)	-	-	-	-
N23	I2C0_SS_SDA	I2C0_SS_SDA	I2C0_SS_SDA	-	EXTERNAL_PAD_24	E1
N24	I2C0_SS_SCL	I2C0_SS_SCL	I2C0_SS_SCL	-	EXTERNAL_PAD_25	E2
P1	ATP_GND1[1]	ATP_GND1[1]	VSS1	ATP_GND1	VSS	A1
P2	ESR1_VBATT	ESR1_VBATT	VCC_BATT_ESR1_3P7	-	VCC_BATT_ESR1_3P7	M10
P3	VDD_HOST_1P8	VDD_HOST_1P8	VCC_HOST_1P8[2]	-	VCC_HOST_1P8[2]	A5
			VCC_HOST_1P8[1]	-	VCC_HOST_1P8[1]	H6
			VCC_PLL_1P8	-	VCC_PLL_1P8	K3
			VCCOUT_HOST_1P8	-	VCCOUT_HOST_1P8	K10
P4	ESR3_LX	ESR3_LX	VCCOUT_ESR3_1P8	-	VCCOUT_ESR3_1P8	K9
P21	SW_FG_VBATT	SW_FG_VBATT / AIN[4])	-	-	EXTERNAL_PAD_04	K6
P22	ATP_GND1[4]	-	-	-	-	-
P23	I2C0_SDA	I2C0_SDA	I2C0_SDA	-	EXTERNAL_PAD_21	C2
P24	ATP_GND1[10]	ATP_GND1[10]	VSS9	ATP_GND1	VSS	M01
-	Internal to 6AXIS	6AXIS_MISO	SDO (6AXIS / 1)	SPI1_SS_MISO	-	B5
-		6AXIS_MOSI	SDX (6AXIS / 14)	SPI1_SS_MOSI	EXTERNAL_PAD_36	C5
-		6AXIS_SCLK	SCX (6AXIS / 13)	SPI1_SS_SCK	EXTERNAL_PAD_37	D5
-		6AXIS_CS	CSB (6AXIS / 12)	SPI1_SS_CS_B[0]	EXTERNAL_PAD_38	E5
-		6AXIS_INT1	INT1 (6AXIS / 4)	GPIO_AON[4]	AON_GPIO_PAD_4	F10

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
-	Internal to BLE	UART0_CTS	P0_12 (BLE / J5)	SPI1_SS_CS_B[2]	UART0_CTS_B	A6
-		UART0_TXD	P0_09 (BLE / J7)	UART0_TXD	GPIO[31]	B2
-		UART0_RTS	P0_10 (BLE / H6)	SPI1_SS_CS_B[3]	UART0_RTS_B	B6
-		UART0_RXD	P0_11 (BLE / J6)	UART0_RXD	AIN[18]	K4
-		ATP_BLE_INT	GPIO[5]	AIN[5]	EXTERNAL_PAD_05	L6
-	ATP_GND1	ATP_GND1[2]	VSS2	ATP_GND1	VSS	B1
-		ATP_GND1	VSS8			M6
-	GND	-	-	-	VSS_IO_AON1	B12
-		-	-	-	VSS_IO_AON2	F7
-		-	-	-	VSS_GNDSENSE_OPM	K7
-		-	-	-	VSS_PLL	L2
-		-	-	-	VSS_RTC	H11
-		-	-	-	VSS_USB	J1
-		-	-	-	VSS_AVS_ESR1	L7
-		-	-	-	VSS_GNDSENSE_ESR1	L8
-		-	-	-	VSS_AVS_ESR2	H7
-		-	-	-	VSS_GNDSENSE_ESR2	H8
-		-	-	-	VSS_GNDSENSE_ESR3	M7
-		-	-	-	VSS_AVS_ESR3	M8
-		-	-	-	VSS_AVSS_CMP1	H3
-		-	-	-	VSS_AVSS_CMP2	L1
-		-	PLT_REG_EN	-	PLT_REG_EN	H10
-	VSYS	VCC (MAX16074 / A2)	-	-	Power supervisory Power On Reset output	-



1.3 Pin definitions

This section presents the Intel® Curie™ module pins and their definitions grouped by function.

Note: The ball names differ from the Intel® Curie™ module to the Intel® Quark™ SE microcontroller C1000 processor core integrated in the module. Table 1-2 above shows the mapping between the two.

1.3.1 Battery and power management pins

Table 1-3 lists the pins on the module that provide battery and power management functionality.

The Intel® Curie™ module has a built-in battery charger, which is optional to use. The user can bypass this internal charger. Refer to the *Battery Charging and Management* section of the *Intel® Curie™ Module Design Guide* for more information.

Table 1-3. Battery and power management pins

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Function
J1	OPM2P6_VOUT	2.6 V reference voltage output. Can be used to power CMP_3P3_VCC. Otherwise leave disconnected.
K4	VDD_USB	DC power for USB interface (optional). This is supplied to the module by the USB cable or external 5V supply. It is also connected to SoC AIN7 internally via voltage divider to be able to detect the voltage presence by software (22k pull-down / 36k pull-up to VDD_USB). Then USB voltage converter can be enabled d by VUSB_EN (GPIO28) to provide 3.3V to the SoC for USB controller.
K24, N21	VIN[1], VIN[2]	Battery charger input voltage, These two pins are connected together internally in module to provide more current. Both pins externally need to be connected to the same voltage source.
L1	LDO1P8_VOUT	AON LDO power output. If used outside Intel® Curie™ module, maximum of 50mA can be drawn externally. It is also connected internally to the SoC VCC_AON_1P8[1], VCC_AON_1P8[2], VCC_SRAM_1P8.
L4	VSYS	Main DC input power. Provides input voltage to BUCK_VOUT (TPS62743) converter, VCC_BATT_OPM_3P7 (SoC), VCC_BATT_ESR3_3P7 (SoC), VCC_AON_PWR (NCP170AMX180TCG).
L22	BATT_ISET	Use a Pull-Down resistor value 0.54-13.5kohm to set charging current. Do not leave floating. Refer to (BQ2510H) datasheet for ISET.
M1	PV_BATT	Battery charger output (4.35 V maximum ±50 mV) to battery (positive) to charge it. External application circuit can be added for protection or / and fuel gauge circuit.
M22	CHG_STATUS	Open drain (15 mA maximum) pulls low when battery is being charged.
N21	See K24 above	
N22	BATT_TEMP	Connect to battery thermistor. See TI BQ25101H* Datasheet for details. If battery does not have internal thermistor to measure temperature, then external thermistor can be used touching the battery to measure temperature for safety and meeting charging requirement of the battery manufacture for reliability.
P21	SW_FG_VBATT	Analog input for software fuel gauge (bat voltage measurement). Connected to SoC AIN4 and can be configured via software to use ADC to measure voltage or current.

1.3.2 Platform buck converter pins

Table 1-4 lists the pins that provide platform control for the buck converter integrated in the module.

Table 1-4. Platform buck converter pins

Ball No.	Ball Name	Function
K1	BUCK_VOUT	Buck converter output of 1.8 V / 3.3 V. It can be connected and used for Awake ON (AON) IO supply voltage. Connect a 0.1 uF decoupling capacitor. The input voltage requirement is minimum of 3.7 V and maximum of 4.4 V. Internal signal BUCK_EN (GPIO_SS15) signal is used for software to disable or enable this converter. If software does not configure the BUCK_EN signal and leave it floating then AON_IO_VCC will enable it via a 10M pull-up resistor. It is highly recommended to enable and disable this via software. In some noisy application this pull-up may not be enough to keep this converter enabled all the time.
K2	BUCK_VSEL	0 (Ground) sets BUCK_VOUT to 1.8 V 1 (VSYS) sets BUCK_VOUT to 3.3 V

1.3.3 Additional buck converter pins

Table 1-5 lists the other pins that provide access to the buck converter integrated in the module.

Table 1-5. Additional buck converter pins

Ball No.	Ball Name	Function
M2	VDD_PLAT_1P8	Platform 1.8 V output[1]
M4	ESR2_LX	External inductor and capacitor connection (for Platform 1V8)[1]
N1	ESR1_LX	External inductor and capacitor connection (for Platform 3V3)[1]
N2	VDD_PLAT_3P3	Platform 3.3 V output[1]
N4	ESR2_VBATT	DC input for switching regulator 2[1]
P2	ESR1_VBATT	DC input for switching regulator 1[1]
P3	VDD_HOST_1P8	1.8 V input to host SoC
P4	ESR3_LX	External inductor and capacitor connection (for Host 1V8)

Notes:

1. Refer to the *Intel® Curie™ Module Design Guide* for guidance on the use of these pins. for further information regarding these pins, refer to the Power Architecture section of the *Intel® Quark™ SE Microcontroller C1000 Datasheet* (in the *Power Management* chapter).

1.3.4 Reference voltage pins

Table 1-6 lists the reference voltage pins for the module.

Table 1-6. Reference voltages on module

Ball No.	Ball Name	Function
E21	AON_IO_VCC	Alway-on GPIO supply voltage
G22	COMP_AREF	Comparator reference voltage external input. Software selectable external 0-3.63 V or internal 1.09 V reference voltage
H22	CMP_3P3_VCC	Comparator supply voltage. See Table 2-6 for voltage specifications.
H23	ADC_3P3_VCC	ADC supply and reference voltage

1.3.5 Module ground pins

Table 1-7 lists the ground pins for the module.

Table 1-7. Ground pins

Ball No.	Ball Name	Function
A2	ATP_GND1[3]	Module ground
A24	ATP_GND1[9]	Module ground
C23	ATP_GND1[5]	Module ground
G21	ATP_GND1[7]	Module ground
G24	ATP_GND1[6]	Module ground
L21	ATP_ADC_AGND	Analog ground. Can be connected directly to analog ground at a single point.
P1	ATP_GND1[1]	Module ground
P22	ATP_GND1[4]	Module ground
P24	ATP_GND1[10]	Module ground

1.3.6 Reset pins

Table 1-8 lists the reset pins for the module.

Table 1-8. Reset pins

Ball No.	Ball Name	Function
B4	ATP_RST_B	SoC hardware reset. Active low. See Section 2.2.6 for information on reset wiring.
D23	MRESET_B	Manual reset. Connect POR_B to reset signal ATP_RST_B and pull low trigger a hardware reset. Refer Power supervisor chip (MAX16074) datasheet for more information.
E23	POR_B	Power on reset from power supervisor chip. Active low / open drain requires a pull-up on this signal. Refer Power supervisor chip (MAX16074) datasheet for more information.

1.3.7 Debugging pins

Table 1-9 lists debugging pins for the module.

When the JTAG emulator is used to connect to the debugging pins on the module, the emulator options need to be configured appropriately to ensure there are no conflicts with these debugging pins.

Table 1-9. Debugging pins

Ball No.	Ball Name	Function
D24	BLE_SW_CLK	Two wire debug interface. For JTAG programming using J-Link. This is also connected to a GPIO[27] signal.
E24	BLE_SWDIO	Two wire debug interface. For JTAG programming using J-Link. This is also connected to a GPIO[6] signal.
K23	ATP_TRST_B	JTAG emulator debugger / programmer TRST signal.
L23	ATP_TCK	JTAG emulator debugger / programmer TCK signal.
L24	ATP_TMS	JTAG emulator debugger / programmer TMS signal.
M21	ATP_TDI	JTAG emulator debugger / programmer TDI signal.
M23	ATP_TDO	JTAG emulator debugger / programmer TDO signal.

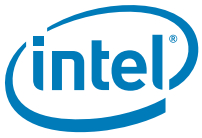
1.3.8 Wake-capable interrupt pins

Table 1-10 lists the pins that are capable of waking the Intel® Quark™ SE microcontroller from a sleep state.

These signals can be programmed to be GPIO input or output. These are always powered.

Table 1-10. Intel® Quark™ SE microcontroller C1000 always-on wake capable interrupt pins

Ball No.	Ball Name	Function	Drive (Low / High)
F21	ATP_INT3	AON GPIO_AON3 / Always On Wake capable digital IO / Interrupt 3, can be configured for one of the two cores.	4mA / 8mA
F22	ATP_INT0	AON GPIO_AON0 / Always On Wake capable digital IO / Interrupt 0, can be configured for one of the two cores.	4mA / 8mA
L3	ATP_INT2	AON GPIO_AON2 / Always On Wake capable digital IO / Interrupt 2, can be configured for one of the two cores.	4mA / 8mA
N3	ATP_INT1	AON GPIO_AON1 / Always On Wake capable digital IO / Interrupt 1, can be configured for one of the two cores.	4mA / 8mA



1.3.9 Clock out pin

Table 1-11 documents the clock out pin on the module.

The software can configure the PLT_CK_0 pin to bring out the SoC core clock (32/16/8/4). It can be used for debugging or for synchronizing the application circuitry. To reduce the power consumption, and if the application does not need it, you should not enable this pin.

Table 1-11. Clock out pin

Ball No.	Ball Name	Primary Function	Alt Function1	Drive (Low / High)
E3	PLT_CLK_0	32/16/8/4MHz Clock output from module	GPIO_SS[14]	4/8mA

1.3.10 GPIO pin mapping

The following subsections document the general purpose input/output (GPIO) pins for the module. These generic pins can be programmed either as input or as output pins at run time. The GPIO pins can be configured for primary or alternate function. Table 1-14 provides the mapping for the multiple functions each pin can be used for.

Table 1-15 documents the internal GPIO signals within the module.

1.3.10.1 GPIO/ analog input pins

Table 1-12 documents the GPIO pins capable of receiving analog inputs. Please note that the internal pull-up resistors are disabled at reset.

Table 1-12. GPIO/ analog input pins

Ball No.	Ball Name	Primary Function	Alt Function1	Drive (Low / High)	Internal Pull-up / Pull-down
C24	GPIO/AIN_14	GPIO_SS[6] (Should be used only for sensor devices)	AIN[14]	Selectable as 4/8	47 kohm
J2	GPIO/AIN_10	GPIO_SS[2] (Should be used only for sensor devices)	AIN[10]		
H21	GPIO/AIN_11	GPIO_SS[3] (Should be used only for sensor devices)	AIN[11]		
H2	GPIO/AIN_12	GPIO_SS[4] (Should be used only for sensor devices)	AIN[12]		
L2	GPIO/AIN_13	GPIO_SS[5] (Should be used only for sensor devices)	AIN[13]		
M22	CHG_STATUS	GPIO_SS[7] (Should be used only for sensor devices)[1]	AIN[15]		

Notes:

1. For CHG_STATUS, please note:
   - CHG_STATUS can be read via software at GPIO_SS[7] / AIN[15]
   - Charge status: Open drain (LOW) means charging and open means complete first charging cycle is complete
   - GPIO_SS[7] / AIN[15] is connected to the external pin (M22) for the device hardware to read the state
   - Internal or external pull-up resistor should be used for this pin
   - If the battery charger is not used then AIN[15] can be used as an external analog input or GPIO_SS[7]. Disable the battery charger by connecting BATT_TEMP to ground.
   - CHG_STATUS or GPIO_SS[7] / AIN[15] is also connected to Nordic* nRF51822 port P0_00. Make sure you keep this pin floating and do not define it as output.

1.3.10.2 GPIO/ AON/ INT mapping module to SoC

Table 1-13 shows the GPIO pins that are directly connected from the Intel® Curie™ module to the Intel® Quark™ SE microcontroller.

Please note that only AON pins and timers can wake the module from sleep. See Section 1.3.8, "Wake-capable interrupt pins".

Table 1-13. GPIO/ AON/ INT

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Intel® Quark™ SE Microcontroller C1000 Signal	Intel® Quark™ SE Microcontroller C1000 Pin
C24	AIN[14]	GPIO_SS[6]	F1
F21	ATP_INT3	GPIO_AON3	F9
F22	ATP_INT0	GPIO_AON0	G9
J2	AIN[10]	GPIO_SS[2]	K5
H21	AIN[11]	GPIO_SS[3]	G1
H2	AIN[12]	GPIO_SS[4]	J4
L2	AIN[13]	GPIO_SS[5]	G2
L3	ATP_INT2	GPIO_AON2	E12
N3	ATP_INT1	GPIO_AON1	E11

1.3.10.3 GPIO multifunction mapping

GPIO pins can be configured for primary or alternate functions. Table 1-14 provides the mapping for the multiple functions each pin can be used for.

Table 1-14. GPIO/ multifunction lines

Intel® Curie™ Module Ball No.	Primary Function	Alternate Function 1	Alternate Function 2
A3	12S_RXD	GPIO[15]	-
A4	SPI0_M_CS1	GPIO[25]	-
B1	I2S_RWS	GPIO[17]	-
B2	I2S_RSCK	GPIO[16]	-
B3	SPI0_M_CS0	GPIO[24]	-
B21	SPI1_M_CS2	GPIO[13]	-
B22	SPI1_M_MISO	GPIO[9]	-
C1	I2S_TWS	GPIO[19]	-
C2	I2S_TSCK	GPIO[18]	-
C3	SPI0_M_CS2	GPIO[26]	-
C4	SPI0_M_SCK	GPIO[21]	-
C21	SPI1_M_SCK	GPIO[8]	-
C22	SPI1_M_CS3	GPIO[14]	-
D1	I2S_TXD	GPIO[20]	-
D3	SPI0_M_MOSI	GPIO[23]	-
D4	SPI0_M_MISO	GPIO[22]	-

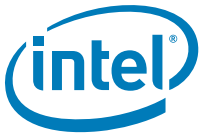


Table 1-14. GPIO/ multifunction lines (continued)

Intel® Curie™ Module Ball No.	Primary Function	Alternate Function 1	Alternate Function 2
D21	SPI1_M_CS1	GPIO[12]	-
D22	SPI1_M_CS0	GPIO[11]	-
E3	PLT_CLK[0]	GPIO_SS[14]	-
E4	SPI_S_CLK	GPIO[2]	AIN[2]
E22	SPI1_M_MOSI	GPIO[10]	-
F2	PWM3_out	GPIO_SS[13]	-
F3	SPI_S_CS_B	GPIO[0]	AIN[0]
F4	SPI_S_MOSI_B	GPIO[3]	AIN[3]
G1	PWM2_out	GPIO_SS[12]	-
G2	PWM1_out	GPIO_SS[11]	-
G3	SPI_S_MISO	GPIO[1]	AIN[1]
G4	SPI0_SS_CS3	GPIO[30]	-
H1	PWM0_out	GPIO_SS[10]	-
J21	UART1_TX	GPIO_SS[8]	AIN[16]
J22	UART1_CTS_B	GPIO_SS[0]	AIN[8]
K3	SPI0_SS_CS2	GPIO[29]	-
K21	UART1_RTS_B	GPIO_SS[1]	AIN[9]
K22	UART1_RX	GPIO_SS[9]	AIN[17]

1.3.10.4 Internal GPIO mapping

Table 1-15 documents the internal GPIO signals within the Intel® Curie™ module.

Some application software can be designed using SW_FG_VBAT to interrupt the Intel® Quark™ SE microcontroller to control the application external battery charging / protection circuit in addition to the battery charger internal resources. The Intel® Quark™ SE microcontroller can monitor the voltages and send signals to the application circuit to turn on and off the supply voltage (VIN) to the charger circuit.

BLE_SW_CLK signal has a 22 kohm internal pull-down resistor to keep it from floating.

BLE_SWDIO signal has a 22 kohm internal pull-up resistor to keep it from floating.

BLE_SW_CLK and BLE_SWDIO are used with the J-Link emulator to program or debug the Bluetooth® low energy controller. It is also connected to the Intel® Quark™ SE microcontroller for the software to implement the debugging function and programming capability if required by the application.

Table 1-15. Internal GPIO signals

Intel® Curie™ Module Signal (Primary Function)	Intel® Curie™ Module Signal (Secondary Function)	Intel® Quark™ SE Microcontroller C1000/ Component Signal	Intel® Quark™ SE Microcontroller C1000 Pin
5V_BUS_SENSE	GPIO[7]	AIN[7]	G3 VDD_USB (via resistor)
ATP_BLE_INT	GPIO[5]	BLE H4	AIN[5]
BLE_SW_CLK (Intel Curie module PIN D24)	BLE_SW_CLK	GPIO[27]	C10
BLE_SWDIO (Intel Curie module PIN E24)	BLE_SWDIO (BLE PIN J2)	GPIO[6]/AIN[6]	H4
BUCK_EN	GPIO_SS[15]	BUCK CONVERTER Enable PIN B1	PLT_CLK[1]
CHG_STATUS (Intel Curie module Pin M22)	SPIO_SS[7]	AIN[15]	J5
SW_FG_VBATT (Intel Curie module PIN P21)	SW_FG_VBAT	GPIO[4]/AIN[4]	K6
UART0_TXD	GPIO[31]	BLE J6	-
VUSB_EN	GPIO[28]	LDO VUSB PIN3 EN	D10
UART0_RXD	AIN[18]	BLE J7	-

1.3.11 6-Axis sensing device pins

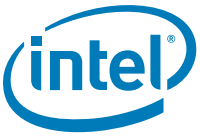
Table 1-17 lists the pins exposed externally from the 6-axis sensing device.

The I^2C interface on the 6-axis sensing device can be connected to a Bosch* BMM150 external magnetometer to make it a 9-axis sensing device.

Refer to the Bosch* BMI160 datasheet for more details.

Table 1-16. Six-axis interface pins

Ball No.	Ball Name	Function
A21	6AXIS_SDA	I^2C data interface to external sensor. Requires external pull-up.
A22	6AXIS_SCL	I^2C clock output to external sensor. Requires external pull-up.
A23	6AXIS_INT2	Auxiliary output pin. Interrupt to external sensor
N/A	6AXIS_INT1	Internal interrupt signal from the 6-axis accelerometer to the Intel Quark processor core



1.3.12 Bluetooth® low energy controller pins

The Intel® Curie™ module includes a Bluetooth® low energy controller that can be controlled externally using the pins in Table 1-17. below.

The debug pins for the integrated Bluetooth® low energy controller are documented in Table 1-9.

Table 1-17. Bluetooth® low energy controller interface pins

Ball No.	Ball Name	Function	Drive (Low / High)
B23	BLE_SDA	I^2C data interface Bluetooth® low energy controller; Can be connected to external master. Requires external pull-up.	Refer to the Nordic* nRf51822 datasheet.
B24	BT_GPIO	GPIO from Bluetooth® low energy (BLE) controller	
F23	BLE_SCL	I^2C clock interface for the Bluetooth® low energy controller chip. Requires external pull-up. Note that this is not supported in software.	
F24	BLE_RF	Bluetooth® antenna connection	
G23	BLE_DEC2	For 3.3 V IO leave unconnected. For 1.8V IO connections to VDD_BLE_SEN. Refer to nrf51822 datasheet for more information	
H24	VDD_BLE_SEN	Bluetooth® low energy controller power supply with internal 0.1 uF capacitor. Refer to the AVDD and VDD power rail in the nRf51822 datasheet for more information.	

1.3.13 I^2C interface pins

I^2C is a multi-master, multi-slave, single-ended serial bus. It is typically used to interface low speed components to the processor. There are four I^2C interfaces available in Intel® Curie™ module: two I^2C interfaces on Intel® Quark™ SE microcontroller processor core and two I^2C interfaces on the ARC* processor core (sensor subsystem). Table 1-18 lists the pins for these interfaces.

Table 1-18. I^2C interface pins

Ball No.	Ball Name	Function	Drive (Low / High)	Internal Pull-Up[1] / Pull-Down
M24	I2C0_SCL	I2C0 clock	4/8 mA	47 kohm internal pull-up configuration can be set in device Firmware for slower speed without external resistor External pull-up resistor needed to operate at higher speed Refer to I^2C specification
P23	I2C0_SDA	I2C0 data		
D2	I2C1_SDA	I2C1 data	2/4 mA	
E1	I2C1_SCL	I2C1 clock (maximum of 1MHz)		
N23	I2C0_SS_SDA	I2C0 sensor subsystem data	2/4 mA	
N24	I2C0_SS_SCL	I2C0 sensor subsystem clock (maximum of 400 kHz)		
E2	I2C1_SS_SDA	I2C1 sensor subsystem data		
F1	I2C1_SS_SCL	I2C1 sensor subsystem clock (maximum of 400 kHz)		

Notes:

1. Internal pull-up resistors are disabled at reset. These I/O's all have typical 47kohm optional internal pull-up that can be enabled by the software.

1.3.14 I²S interface pins

Table 1-19 lists the pins for the two I²S bus interfaces on the module. This electrical serial bus interface is used to connect digital audio devices.

The I²S interfaces on the module have a fixed output sample size of 32 bits. The input sample size ranges from 12–32bits. The data is sent in raw PCM format and has to be processed by the device connected to the port.

Table 1-19. I²S interface pins

Ball No.	Ball Name	Function	Alternate Function	Drive (Low / High)	Internal Pull-Up[1] / Pull-Down
A3	I2S_RXD	Receive RX data	GPIO[15]	2/4 mA	47 kohm Internal pull-up configuration can be set in device Firmware for slower speed without external resistor External pull-up resistor needed to operate at maximum speed
B2	I2S_RSCK	Receive clock input	GPIO[16]		
B1	I2S_RWS	Receive word select	GPIO[17]		
C1	I2S_TWS	Transmit word select	GPIO[19]	4/8 mA	
C2	I2S_TSCK	Transmit clock output	GPIO[18]		
D1	I2S_TXD	Transmit TX data	GPIO[20]		

Notes:

1. Internal pull-up resistors are disabled at reset. These I/Os all have typical 47 kohm optional internal pull-up that can be enabled by the software.

1.3.15 Pulse width modulator (PWM) pins

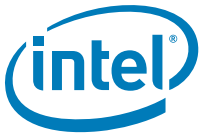
Pulse width modulation is a technique used to encode a message into a pulsing signal. The main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors. The Intel® Curie™ module has four counters capable of operating in PWM mode. Table 1-20 lists the pins providing the output from these counters.

Table 1-20. PWM output pins

Ball No.	Ball Name	Alternate Function	Function	Drive (Low / High)	Internal Pull-Up[1] / Pull-Down
F2	PWM3_OUT	PWM [3]	GPIO_SS[13]	4/8 mA	47 kohm
G1	PWM2_OUT	PWM [2]	GPIO_SS[12]		
G2	PWM1_OUT	PWM [1]	GPIO_SS[11]		
H1	PWM0_OUT	PWM [0]	GPIO_SS[10]		

Notes:

1. Internal pull-up resistors are disabled at reset. These I/O's all have typical 47 kohm optional internal pull-up that can be enabled by the software.



1.3.16 SPI master pin out

SPI is a synchronous serial communication interface used for communication in embedded platforms. Intel® Curie™ module has three SPI ports available to work in master mode: two SPIs from Intel® Quark™ SE microcontroller processor core and one from the ARC* processor core (sensor subsystem). Table 1-21 lists the pins for these ports, grouped according to the three ports respectively.

Table 1-21. SPI master pins

Ball No.	Ball Name	Source	Primary Function	Alt Function	Drive (Low / High)	Internal Pull-Up[1] / Pull-Down
A4	SPI0_M_CS1	SoC SPI0	chip select 1	GPIO[25]	2/4 mA	47 kohm
B3	SPI0_M_CS0		chip select 0	GPIO[24]		
C3	SPI0_M_CS2		chip select 2	GPIO[26]		
C4	SPI0_M_SCK		clock	GPIO[21]		
D3	SPI0_M_MOSI		data out	GPIO[23]		
D4	SPI0_M_MISO		data in	GPIO[22]		
B21	SPI1_M_CS2	SoC SPI1	chip select 2	GPIO[13]	2/4 mA	
B22	SPI1_M_MISO		data in	GPIO[9]	4/8 mA	
C21	SPI1_M_SCK		clock	GPIO[8]		
C22	SPI1_M_CS3		chip select 3	GPIO[14]	2/4 mA	
D21	SPI1_M_CS1		chip select 1	GPIO[12]		
D22	SPI1_M_CS0		chip select 0	GPIO[11]		
E22	SPI1_M_MOSI		data out	GPIO[10]		
H3	SPI0_SS_CS1	Sensor system	chip select 1	-	4/8 mA	
H4	SPI0_SS_CS0		chip select 0	-		
G4	SPI0_SS_CS3		chip select 3	GPIO[30]	2/4 mA	
J3	SPI0_SS_MISO		data in	-	4/8 mA	
J4	SPI0_SS_SCK		clock	-		
K3	SPI0_SS_CS2		chip select 2	GPIO[29]	2/4 mA	
M3	SPI0_SS_MOSI		data out	-	4/8 mA	

Notes:

1. Internal pull-up resistors are disabled at reset. These I/Os all have typical 47 kohm optional internal pull-up that can be enabled by the software.

1.3.17 SPI slave pin out

The module also has one SPI port available to work in slave mode. Table 1-22 lists the pins for that port.

Table 1-22. SPI slave pins

Ball No.	Ball Name	Primary Function	Alt Function 1	Alt Function 2	Drive (Low / High)	Internal Pull-Up[1] / Pull-Down
E4	ATP_SPI_S_SCK	clock	GPIO[2]	AIN[2]	4/8 mA	47 kohm
F3	ATP_SPI_S_CS	chip select	GPIO[0]	AIN[0]		
F4	ATP_SPI_S_MOSI	data in	GPIO[3]	AIN[3]		
G3	ATP_SPI_S_MISO	data out	GPIO[1]	AIN[1]		

Notes:

1. Internal pull-up resistors are disabled at reset. These I/Os all have typical 47 kohm optional internal pull-up that can be enabled by the software.

1.3.18 UART interface pins

The module has two UART interfaces for asynchronous serial communication. The data format and transmission speeds on this interface are configurable. Only one UART interface is available for the user, the other UART interface is dedicated to the Bluetooth® low energy controller inside the module. Table 1-23 lists the pins for the user-facing interface.

Table 1-23. UART Interface pins

Ball No.	Ball Name	Primary Function	Alt Function 1	Alt Function 2	Drive (Low / High)	Internal Pull-Up[1] / Pull-Down
J21	UART1_TX	Transmit Data	GPIO_SS[8]	AIN[16]	4/8 mA	47 kohm pull-up
J22	UART1_CTS	flow control	GPIO_SS[0]	AIN[8]		
K21	UART1_RTS	flow control	GPIO_SS[1]	AIN[9]		
K22	UART1_RX	Receive Data	GPIO_SS[9]	AIN[17]		

Notes:

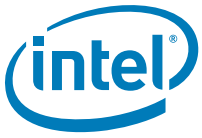
1. Internal pull-up resistors are disabled at reset. These I/Os all have typical 47 kohm optional internal pull-up that can be enabled by the software.

1.3.19 USB interface pins

USB is an industry standard used to connect peripheral devices or any pair of devices together through the USB port in order to communicate and/or supply power. the Intel® Curie™ module has a single USB 1.1 device port. Table 1-24 lists the pins for the USB port.

Table 1-24. USB Interface pins

Ball No.	Ball Name	Primary Function
J1	GROUND also known as VSS_USB and USB_VSS	Ground connection with external USB source
J23	USB_DM	USB Data Minus (-) bidirectional signal
J24	USB_DP	USB Data Positive (+) bidirectional signal
K4	VDD_USB	5 V DC used to sense from a power host and used to power the USB transceiver.



1.3.20 ADC pins

The module offers an analog-to-digital converter. Table 1-25 lists the Intel® Curie™ module external pins connected to Intel® Quark™ SE microcontroller ADC interface pins and Table 1-26 provides a list of Intel® Quark™ SE microcontroller ADC interface multifunction pins connected to Intel® Curie™ module external pins.

Table 1-25. Intel® Curie™ module external pins connected to Intel® Quark™ SE microcontroller ADC interface pins

Intel® Curie™ Module Ball No.	Analog Input Signal Name	Intel® Quark™ SE Microcontroller C1000 Ball No.
C24	AIN_14	F1
H2	AIN_12	G1
H21	AIN_11	G2
J2	AIN_10	J4
L2	AIN_13	K5

Table 1-26. Intel® Quark™ SE microcontroller ADC interface multifunction pins connected to Intel® Curie™ module external pins

Intel® Curie™ Module Ball No. (Intel® Quark™ SE Microcontroller C1000 Ball No.)	Optional Functions
E4	GPIO[2]/AIN[2]/SPI_S_SCK
E24 (Intel® Quark™ SE microcontroller pin H4)	GPIO[6]/AIN[6]/Intel® Quark™ SE microcontroller_SWDIO
F3	GPIO[0]/AIN[0]/SPI_S_CS_B
F4	GPIO[3]/AIN[3]/SPI_S_MOSI
G3	SPI_S_MISO/GPIO[1]/AIN[1]
J22 (Intel® Quark™ SE microcontroller pin L5)	GPIO_SS[0]/AIN[8]/UART1_CTS_B/
K4 (VDD_USB, Intel® Quark™ SE microcontroller pin G3)	GPIO[7]/5V_BUS_SENSE/AIN[7]
K21 (Intel® Quark™ SE microcontroller pin M5)	GPIO_SS[1]/AIN[9]/UART1_RTS_B
M22 (Intel® Quark™ SE microcontroller pin J5)	CHG_STATUS/GPIO_SS[7]/AIN[15]
P21 (Intel® Quark™ SE microcontroller pin K6)	GPIO[4]/SW_FG_VBATT/AIN[4]

2 Specifications

2.1 Electrical characteristics

This section covers the absolute maximum ratings, operating maximum and minimum voltages, and the DC operating specifications.

2.1.1 Absolute maximum and minimum voltages

The absolute maximum and minimum specifications are used to specify conditions allowable outside of the functional limits of the Intel® Curie™ module, but with possibly reduced life expectancy once returned to functional limits. At conditions exceeding absolute specifications, neither functionality nor long term reliability can be expected. Parts may not function at all once returned to functional limits.

Table 2-1 shows the absolute ranges for the Intel® Quark™ SE microcontroller C1000 integrated in the module.

Caution: Although the module contains protective circuitry to resist damage from electrostatic discharge (ESD), always take precautions to avoid high static voltages or electric fields. See Section 2.1.5 for ESD data.

Table 2-1. Absolute min-max specifications for the Intel® Quark™ SE microcontroller C1000

Intel® Curie™ Module Signal	Function	Intel® Quark™ SE Microcontroller C1000 Mapped Signal	Range
VDD_USB	USB input voltage	VUSB	–0.3 V to 3.63 V
VSYS	Supply voltage	VCC_BATT_OPM_3P7	–0.3 V to 4.4 V
AIN	Analog input voltage	VCC_ADC	–0.3 V to 3.63 V

2.1.2 Operating maximum and minimum voltages

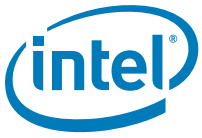
Table 2-2 provides the operating ranges for the Intel® Curie™ module.

Table 2-2. Operating Min - Max specifications for the Intel® Curie™ module

Ball	Function	Power I/O	Min	Typ	Max	Unit
VDD_PLAT_1P8	3.3 V for platform devices	-	1.62	1.8	1.98	V
VDD_PLAT_3P3	1.8 V for platform devices	-	2.97	3.30	3.63	V
VDD_HOST_1P8	1.8 V for host blocks	-	1.62	1.8	1.98	V
VDD_USB	USB power	-	3.5	5.0	5.25	V
VIN	Charging DC input	-	4.45	5.0	6.45	V
VSYS[1]	Main DC input power	-	2.1	-	4.4	V

Notes:

1. VSYS should be greater than 3.3 V if the module VDD_PLAT_3P3 regulator is used.



2.1.3 DC operating specifications

Table 2-3 through Table 2-8 include the DC operating specifications for Intel® Curie™ module.

2.1.3.1 DC specifications for I/O

Table 2-3 provides the voltage ranges for AON_IO_VCC at 3.3 V, while Table 2-4 provides the voltage ranges for AON_IO_VCC at 1.8 V.

Table 2-3. AON_IO_VCC= 3.3 VDC

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input low voltage	-	-	0.8	V
VIH	Input high voltage	2	-		V
VOL	Output low voltage	-	-	0.4	V
VOH	Output high voltage	2.4	-	-	V
IOL	2 mA @ VOL	2.4	3.8	5.3	mA
	4 mA @ VOL	4.7	7.6	10.6	mA
	8 mA @ VOL	9.4	15.3	21.2	mA
IOH	2 mA @ VOH	3.4	7.0	11.6	mA
	4 mA @ VOH	6.9	14.0	23.2	mA
	8 mA @ VOH	13.8	27.9	46.4	mA
RPU	Pull-up resistor	34K	49K	74K	ohm
VT	Threshold point	1.33	1.4	1.47	V
VT+	L-> H threshold point	1.53	1.6	1.66	V
VT-	H-> L threshold point	1.13	1.2	1.27	V

Table 2-4. AON_IO_VCC= 1.8V

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input low voltage	-	-	0.63	V
VIH	Input high voltage	1.17	-	-	V
VOL	Output low voltage	-	-	0.45	V
VOH	Output high voltage	1.35	-	-	V
IOL	2 mA @ VOL	1.0	2.0	3.6	mA
	4 mA @ VOL	1.9	4.0	7.2	mA
	8 mA @ VOL	3.9	8.1	14.4	mA
IOH	2 mA @ VOH	0.8	2.0	4.1	mA
	4 mA @ VOH	1.6	4.0	8.1	mA
	8 mA @ VOH	3.2	8.0	16.2	mA
RPU	Pull-up resistor	34K	49K	74K	ohm
VT	Threshold point	0.82	0.89	0.93	V
VT+	L-> H threshold point	0.99	1.07	1.12	V
VT-	H-> L threshold point	0.62	0.69	0.77	V

2.1.3.2 ADC - DC I/O specifications

Table 2-5 provides the voltage ranges for the analog-to-digital converter.

Note: The parasitic capacitance of the Intel® Quark™ SE microcontroller and the package are TBD. We recommend adding 10 pF to the calculations for input capacitor charging.

Table 2-5. ADC - DC I/O specifications

Symbol	Parameter	Min	Typ	Max	Unit
AIN	Full-scale input range	0	-	≤ADC_3P3_VCC ≤AON_IO_VCC	V
AGNDREF	Negative reference voltage	0	0	0.1	V
ADC_cap	Input sampling capacitance	-	5	-	pF

2.1.3.3 Comparator voltage specification

Table 2-6 provides the voltage ranges for the comparator.

Table 2-6. Comparator voltage range

Symbol	Parameter	Min	Typ	Max	Unit
COMP_AREF	External reference voltage	0.0	-	≤ CMP_3P3_VCC	V
AIN	Full scale input voltage	0.0	-	≤ CMP_3P3_VCC ≤ AON_IO_VCC	V
CMP_3P3_VCC	Comparator power	2.0	-	3.6	V

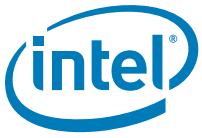
2.1.3.4 USB I/O - DC specifications

Table 2-7 provides the DC specifications for the USB I/O.

Note: Refer to the Intel® Quark™ SE microcontroller datasheet for the complete electrical specifications.

Table 2-7. USB I/O - DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input low voltage	-	-	0.8	V
VIH	Input voltage high	2.0	-	-	V
VOL	Output low voltage	-	-	0.3	V
VOH	Output high voltage	2.8	-	-	V
VCRS	Differential output signal cross-point	1.3	-	2.0	V
VCM	Common mode range	0.8	-	2.5	V
RPU	External pull-up resistor	1.425	-	1.575	kohm
Vtrm	Termination voltage	3.0	-	3.6	V



2.1.3.5 USB I/O - AC specifications

Table 2-8 provides the AC specifications for the USB I/O.

Table 2-8. USB IO AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
TFR	Rise time 50 pF	4	-	20	ns
TFF	Fall time 50 pF	4	-	20	ns
TFRFF	Rise/fall matching	90	-	111.11	%

2.1.4 Operating temperature range

Operating temperature range: -25°C to +70°C.

Charging: 0°C to 60°C when using the internal charger.

2.1.5 ESD considerations

Table 2-9 shows the ESD considerations for the Intel® Curie™ module.

Note: A reduction in either the HBM or CDM goal does not require additional design changes beyond the actual ESD guidance.

Table 2-9. Intel® Curie™ module component ESD data

Symbol	Description	Stress Conditions
HBM	ESD - Human Body Model - JS-001-2014	±1000 V
CDM	ESD - Charge Device Model - JESD22-C101	±500 V

2.2 Power and timing considerations

This section covers all the aspects of power consideration for the Intel® Curie™ module.

2.2.1 Power architecture

The power architecture is a power generation solution that provides both the internal – host and always on (AON) – and external (platform) supply rails. Some of these supply voltages can be internally or externally turned off to reduce the power consumption for the application.

The Intel® Curie™ module internal power supply resources are limited and can only be used in some applications. Applications which require higher power can use the application power converter circuits to provide their power needs. If any of these voltage converters are not used, the application firmware and hardware need to disable the unused voltage converters to reduce the leakage and improve the power consumption.

Also look at the third-party switching supplies and make sure their minimum output load is met otherwise their output voltage regulation may not be stable.

2.2.2 Primary power

The Intel® Curie™ module is designed to operate under battery-operated systems using 3.3 V or 1.8 V interfaces, or may be powered by external regulators providing 1.8 V or 3.3 V. The module has regulators available to power internal circuits or for use by platform applications. They are documented in this section and in Section 2.2.3, "Optional platform power".

An integrated power supervisor holds the system in reset when the input voltage drops below 2.9 V. Intel recommends ensuring that the OPM2P6_VOUT node (2.6 V reference voltage output; Ball Number J1) is discharged to ground (zero volt) before a power-up cycle. An external power supervisor may be required. Refer to the *Intel® Curie™ Power Sequence Considerations* application note for important information when designing your product.

Intel® Curie™ module has an 1.8 V power regulator (labeled ESR3) which must be used to power internal circuits.

The power regulators require an inductor and a bulk capacitor as a part of the switching regulator function. Table 2-10 provides the values of the inductors and the capacitors for the maximum power delivery for ESR3, as well as the optional regulators documented in Section 2.2.3, "Optional platform power". Table 2-11 shows the maximum current range.

Other core voltages include:

- VDD_BLE_SEN, used to supply voltage to the internal Bluetooth® low energy controller and the 6-axis sensing device.
- AON_IO_VCC, used to set the supply voltage to the IO level for the peripheral interfaces. The choice is 1.8 V or 3.3 V level.

2.2.3 Optional platform power

Intel® Curie™ module also has 1.8 V and 3.3 V regulators available for use by platform applications. These internal LDO and converters are optional to use and the application can provide their own converter or power source to meet their requirements.

- ESR1 provides the platform 3.3 V, which can be used by external platform devices.
- ESR2 provides the platform 1.8 V, which can be used by external platform devices.

The power regulators require an inductor and a bulk capacitor as a part of the switching regulator function. Table 2-10 provides the value of the inductor and the capacitor for the maximum power delivery for all the power regulators. Table 2-11 shows the maximum current range.

On-module regulators supply the integrated components while external devices need their own power system.

Note: Exceeding the maximum input specifications or using non-compliant USB chargers damages Intel® Curie™ module input regulators.

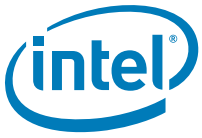


Table 2-10. ESR requirements

Parameter	Description	Tolerance Min	Typical	Tolerance Max	Unit
3.3V Platform rail requirements					
C_ESR1	Decoupling capacitor	-20%	8.2	+20%	µF
L_ESR1	Inductor	-30%	10	+30%	µH
1.8V Platform rail requirements					
C_ESR2	Decoupling capacitor	-20%	4.7	+20%	µF
L_ESR2	Inductor	-30%	22	+30%	µH
1.8V Host rail requirements					
C_ESR3	Decoupling capacitor	-20%	4.7	+20%	µF
L_ESR3 -	Inductor	-30%	22	+30%	µH

Table 2-11. Maximum current range

Power Rails from Intel® Curie™ Module	Description	Maximum Current (mA)
VDD_PLAT_3P3	ESR1 - 3.3 V for platform devices (from Intel® Quark™ SE microcontroller SoC)	150
VDD_PLAT_1P8	ESR2 - 1.8 V for platform device (from Intel® Quark™ SE microcontroller SoC)	100
VDD_HOST_1P8	ESR3 - 1.8 V for Host Blocks (from Intel® Quark™ SE microcontroller SoC). Internal switching regulator 1.8v supply that can be used to power the cores. Additional inductor and capacitor is required.	100
BUCK_VOUT*	1.8 V/3.3 V for platform devices. (from internal buck)	300

2.2.4 Device power states

2.2.4.1 Off state

In the Off state, all the voltage rails are disabled and no clocks are running.

The Off state is entered if the main power is removed or if the power is at an insufficient level to power the device.

When the power is applied, the device exits the Off state and transitions to Active.

2.2.4.2 Sleep state

Sleep is a suspend state in which:

- The core voltage rail and core clock are turned off, RTC clock is running.
- The always-on voltage rail remains powered in this state.
- The 3P3 and 1P8 voltage rails can be individually configured to power down for energy savings.
- A wake event via an enabled comparator, AON GPIO, AON timers or RTC event is required to exit the Sleep state.
- The contents of SRAM can optionally be retained during the Sleep state
- Peripherals within the module can remain active when the SoC is in a sleep state.

- GPIOs can be configured to go in retention mode to hold their state while the core is in sleep mode.
- Refer to the diagram "SoC power states" in the Intel® Quark™ SE microcontroller Datasheet under power management.

2.2.4.3 Active state

- The Active state is the normal operating state of the SoC:
  - The core clock and RTC clock are running.
  - The Core (1P8) and AON voltage rails are enabled.
  - Applications can select if the 3P3 voltage rail is energized.
- Within the Active state:
  - The host processor can transition into and out of various C-states.
  - The sensor subsystem can transition into and out of various sensing states.
  - The SoC peripherals can be disabled or clock-gated for additional power savings.

2.2.5 Intel® Quark™ SE microcontroller C1000 power states

The Intel Quark microcontroller and the ARC* processor cores can run at a lower internal clock, if acceptable to application / design intent, for additional power savings that can be further enhanced with proper use of sleep states and wake events.

Refer to the Intel® Quark™ SE Microcontroller C1000 Datasheet for detailed information.

2.2.6 Boot and reset sequences

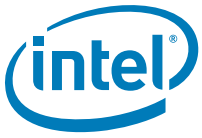
2.2.6.1 Power-up - Off to Active

When VCC_BATT_V3P7 is applied by means of an external battery or other power source, the Intel® Curie™ module can power up with any internal or external software-enabled power converter that is used in the application design.

LDO 1.8V NCP170 is enabled by the VCC_AON_1P8 rail when it reaches the logic high threshold.

TPS62743 buck regulator (1.8V / 3.3V) is enabled by the AON_IO_VCC rail when it reaches the logic high threshold if the software disables BUCK_EN by tri-stating GPIO_SS[15]. Or the software can set GPIO_SS[15] = 1 to enable or GPIO_SS[15] = 0 to disable the bulk regulator.

MIC5504-3.3YMT LDO (3.3v) is enabled by the VUSB_EN signal that is 61% of the 5 V USB supply voltage when the USB cable is plugged. The software can then be configured to get an interrupt and the software can set GPIO[28] = 1 to enable the LDO for the USB interface. The software can disable the LDO by setting GPIO[28] = 0.



2.2.6.2 Power-up sequence timings and thresholds

The power sequence and timings given in this section are representative of typical values measured.

All rails except VSYS and AON_IO_VCC are outputs.

VIN is the system power supply. AON_IO_VCC has to be supplied externally. It is recommended to use VCC_AON_PWR to power the AON_IO_VCC. If it is fed by any other source, please make sure that the timings are met.

Note: Refer to the *Intel® Curie™ Power Sequence Considerations* application note for important information when designing your product.

Refer to *Intel® Quark™ SE Microcontroller C1000 Datasheet* for power-up sequence timing parameters and power architecture section.

The Intel® Curie™ module includes a power supervisor shown in Figure 2-1. This holds off the boot up sequence until VCC_HOST_1P8 voltage is within specification.

Figure 2-2 below presents the power state change diagram, while Figure 2-3 illustrates the power rail timing sequence and Table 2-12 details the power-up sequence parameters.

Figure 2-1. Power supervisor

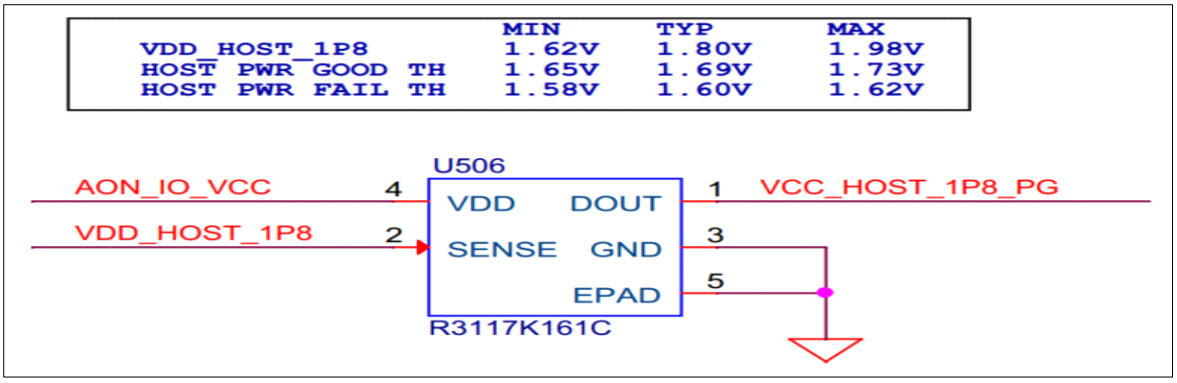


Figure 2-2. Power state change diagram

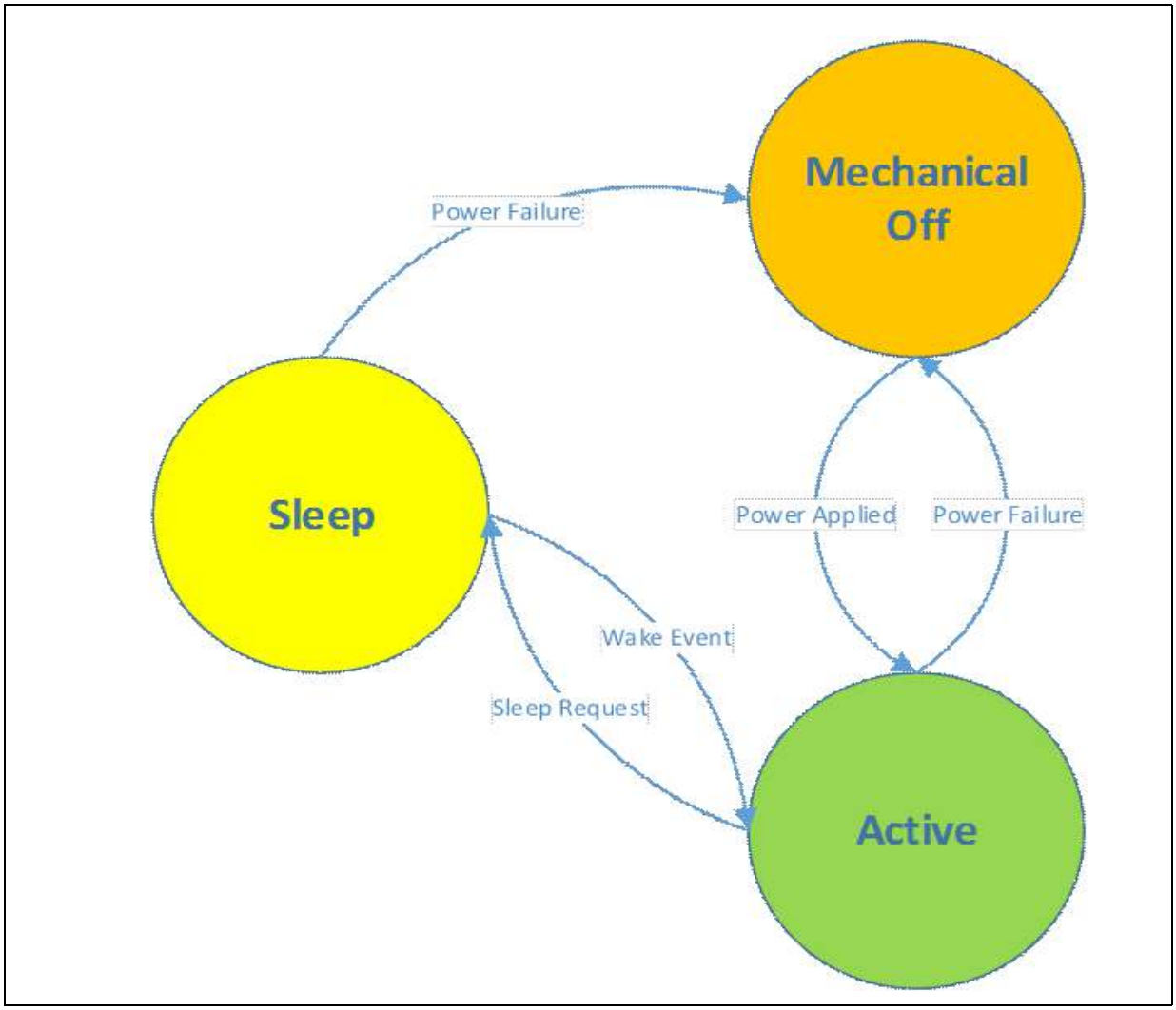


Figure 2-3. Power rail timing sequence

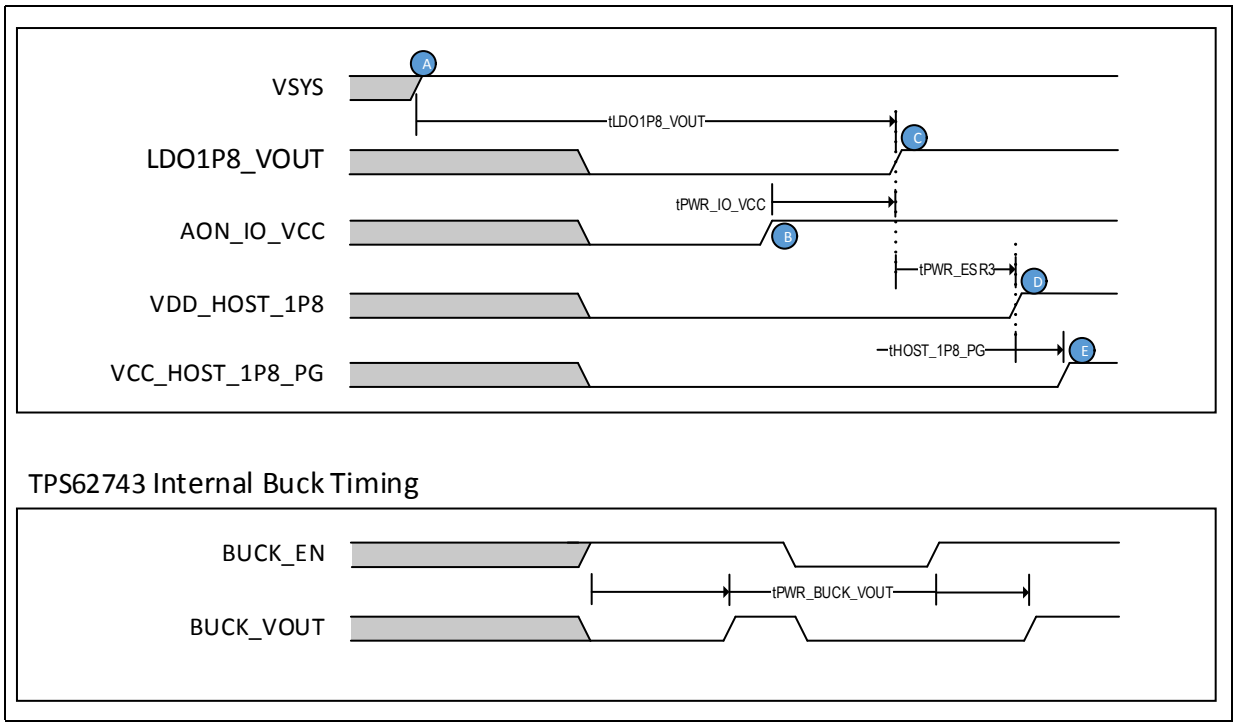


Table 2-12. Power-up sequence parameters

Parameter	Description	Min	Typ	Max	Unit
tLDO1P8_VOUT	Time interval between the VSYS and the availability of LDO1P8_VOUT	-	6.2	-	ms
tPRW_ESR3	Time interval for eSR3 starts regulate the output voltage when VCCOUT_AON_1P8 reaches threshold (1.55V).	-	925	-	µs
tPWR_IO_VCC	Time interval for LDO properly regulate output voltage when Enable asserted.	0	-	-	ms
tHOST_1P8_PG	Time interval for buck regulator properly regulate output voltage when Enable asserted.	-	100	-	µs
tPWR_BUCK_VOUT	Time interval for buck regulator (TPS62743) properly regulate output voltage when Enable (BUCK_EN) asserted.	-	10	25	ms

Waveforms from lab measurements are provided in Figure 2-4 and Figure 2-5 below as reference:

Figure 2-4. Timing relationship between VIN, OPM2P6_VOUTand LDO1P8_VOUT

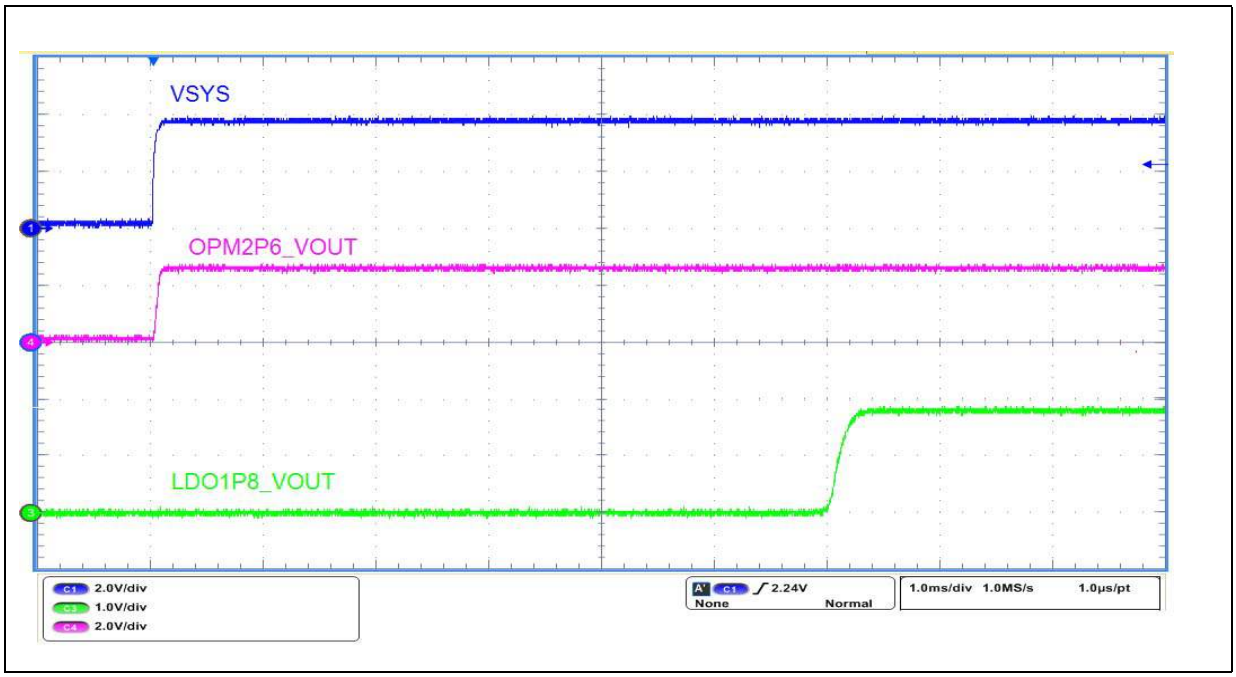
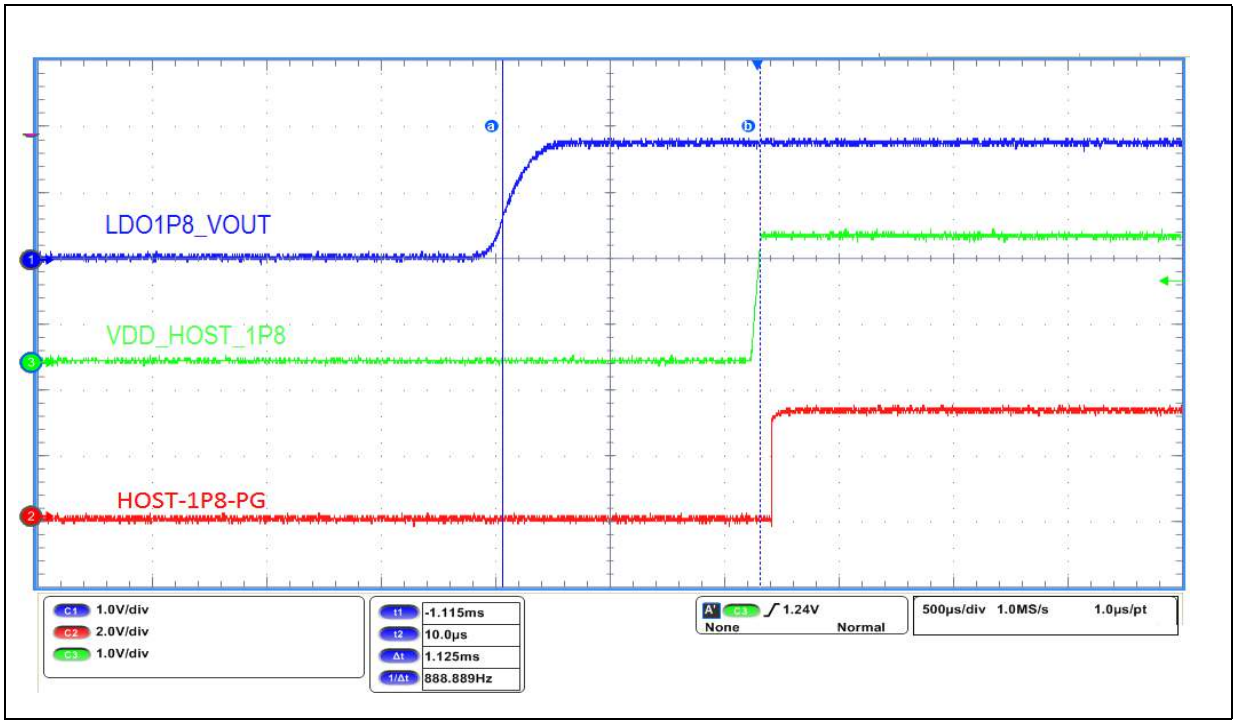
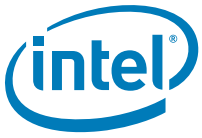


Figure 2-5. Timing relationship between LDO1P8_VOUT, VDD_HOST_1P8 and VDD_HOST_1P8-PG





2.2.7 Platform power distribution

Table 2-13 documents the maximum current output for each power rail.

Table 2-13. Power rail maximum current output

Power Rail	Sources	Maximum Current
1.9VDC to 4.4V RAIL		
VCC_BATT_OPM_3P7	Battery	300ua
VCC_BATT_ESR1_3P7	Battery	250mA
VCC_BATT_ESR2_3P7	Battery	125mA
VCC_BATT_ESR3_3P7	Battery	125mA
1.8VDC RAIL		
VCC_AON_1P8	Internal LDO in Intel® Curie™ module	150mA
VCC_HOST_1P8	ESR3	50mA (Preliminary)
VCC_SRAM_1P8	Internal LDO within Intel® Curie™ module	4mA
VCC_PLL_1P8	ESR3	2.2mA
VCC_RTC_1P8	Internal LDO within Intel® Curie™ module	125nA
3.3V RAIL		
ADC_3P3_VCC	Dedicated ADC LDO	1mA
VCC_CMP_3P3	ESR1/OPM_2P6/Dedicated Comp LDO	60uA
VCC_USB_3P3	Dedicated LDO for USB	1mA
VDD_BLE_SEN	BUCK_OUT	26.75mA

2.2.8 Current draw (typical)

The data provided in this section was measured on a design-development platform and does not include components outside the Intel® Curie™ module. Results shown are averages that are highly influenced by software configuration choices.

2.2.8.1 Module current consumption

Table 2-14 through Table 2-18 provide data on Intel® Curie™ module current consumption.

Table 2-14. Intel® Curie™ module power consumption: idle - without motion sensing

State	Value	Unit	Description
Intel® Curie™ module Idle - No motion sensing	29.62	uA	-
Peripherals breakdown			No motion sensing and No Bluetooth® low energy activity SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic* Bluetooth® low energy Idle BMI160 Accelerometer and Gyrometer suspend
Intel® Quark™ SE microcontroller Deep Sleep (RTC ON/SRAM/IO retention)	18.7	uA	
Intel® Quark™ SE microcontroller watchdog wake every 33.5s	1		
Bluetooth® low energy Idle - Low power mode	2.55		
Bosch* BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ module hardware floor current	5.5		

Table 2-15. Intel® Curie™ module power consumption: idle - motion sensing without movement

State	Value	Unit	Description
Intel® Curie™ module Idle - Motion sensing without any move	54.13	uA	-
Peripherals breakdown			No motion sensing and No Bluetooth® low energy activity SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic* Bluetooth® low energy Idle BMI160 Accelerometer low power & Gyrometer suspend
Intel® Quark™ SE microcontroller Deep Sleep (RTC ON/SRAM/IO retention/External IRQ Wakeup	18.7	uA	
Intel® Quark™ SE microcontroller watchdog wake every 33.5s	1		
Bluetooth® low energy Idle - Low power mode	2.36		
Bosch* BMI160 (Accel ODR 100Hz@AVG1 / Gyro in suspend mode)	26.57		
Intel® Curie™ module hardware floor current	5.5		

Table 2-16. Intel® Curie™ module power consumption: Bluetooth® low energy fast advertising at 100ms - without motion sensing

State	Value	Unit	Description
Intel® Curie™ module Bluetooth® low energy Fast Advertising @100ms - No motion sensing	153.67	uA	-
Peripherals breakdown			No motion sensing - BMI160 Accelerometer & Gyrometer suspend SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic* Bluetooth® low energy advertising every 100ms; in Bluetooth® low energy Low power mode rest of the time
Intel® Quark™ SE microcontroller Deep Sleep (RTC ON/SRAM/IO retention/External IRQ Wakeup)	18.7	uA	
Intel® Quark™ SE microcontroller watchdog wake every 33.5s	1		
Bluetooth® low energy Fast Adv 100ms + Low power mode	126.6		
Bosch* BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ module hardware floor current	5.5		

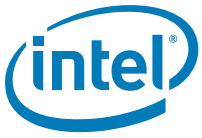


Table 2-17. Intel® Curie™ module power consumption: Bluetooth® low energy connection at 150 ms - without motion sensing

State	Value	Unit	Description
Intel® Curie™ module Bluetooth® low energy Connection @150ms - No motion sensing	57.77	uA	-
Peripherals breakdown			No motion sensing - BMI160 Accelerometer & Gyrometer suspend SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic* Bluetooth® low energy advertising every 100ms; in Bluetooth® low energy Low power mode rest of the time
Intel® Quark™ SE microcontroller Deep Sleep (RTC ON/SRAM/IO retention/External IRQ Wakeup)	18.7	uA	
Intel® Quark™ SE microcontroller watchdog wake every 33.5s	1		
Bluetooth® low energy Fast Adv 100ms + Low power mode	30.7		
Bosch* BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ module hardware floor current	5.5		

Table 2-18. Dhrystone 2.1 results: without motion sensing

State	Value	Unit	Description
Intel® Curie™ module Bluetooth® low energy Connection @150ms - No motion sensing	36.01	mA	-
Peripherals breakdown			No motion sensing - BMI160 Accelerometer & Gyrometer suspend SoC Idle (Deep Sleep + WDT wakeup every 5s) Nordic* Bluetooth® low energy advertising every 100ms; in Bluetooth® low energy Low power mode rest of the time
Intel® Quark™ SE microcontroller LTM C0 Dhrystone 2.1 ARC SS0 Dhrystone 2.1 with all peripherals clock gated ON	36	mA	
Bluetooth® low energy Idle - Low power mode	2.36	uA	
Bosch* BMI160 (Accel / Gyro in suspend mode)	1.87		
Intel® Curie™ module hardware floor current	5.5		

2.3 Clocking

The Intel® Curie™ module contains several clock sources which are described in this section. Accuracy is specified over the operating temperature range for the Intel® Curie™ module.

Refer to the chapter on *Clocking* in the *Intel® Quark™ SE Microcontroller C1000 Datasheet*, for further details on the SoC clocks mentioned in Table 2-19.

Table 2-19. Clock sources

Clock	Use	Accuracy
32kHz[1]	Always on timer	± 5ppm
SoC Silicon Oscillator	Enabled at boot time	± 20,000ppm
SoC XTAL Oscillator 4/8/16/32MHz[2]	Can be enabled by software	± 30ppm
16MHz Bluetooth® low energy clock	Active during BLE transmit/receive	± 30ppm

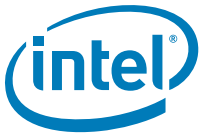
Notes:

1. This is a MEMS based temperature compensated clock that feeds both the AP SoC as well as the Nordic BLE controller. It is always running when power is applied. Primary use is for real time clock and software timer.
2. Must be used to meet UART timing

2.4 BLE (Bluetooth® low energy)

The Bluetooth® low energy controller in the Intel® Curie™ module provides BLE connectivity with the following performance metrics:

- -93 dBm sensitivity
- 250 kbps, 1 Mbps, and 2 Mbps supported data rates
- -20 to +4 dBm TX power output in 4 dB steps
- -30 dBm in whisper mode
- RSSI reporting with 1 dB resolution
- BT certified 4.1 LE stack



3 Detailed Description

The Intel® Curie™ module is an advanced device built around the Intel® Quark™ SE microcontroller C1000 processor core. It integrates compute, sense, and awareness functionality, as well as connectivity and a programmable input/output controller within a common package.[1]

The Intel® Curie™ module is a tiny hardware product offering design flexibility. The complete, low-power solution comes with compute, motion sensors, Bluetooth® low energy, battery-charging, and pattern matching capabilities for optimized analysis of sensor data, enabling quick and easy identification of actions and motions. The module is packaged into a very small form factor and runs a new software platform created specifically for the Intel® Curie™ module.

Powered by the Intel® Quark™ SE Microcontroller C1000, the Intel® Curie™ module is extremely power efficient and ideal for "always-on" applications such as health and wellness, social notification and sports activities. The Intel Quark microcontroller integrates a pattern classification engine that allows it to identify different motions and activities quickly and accurately.

The chapter includes the following sections:

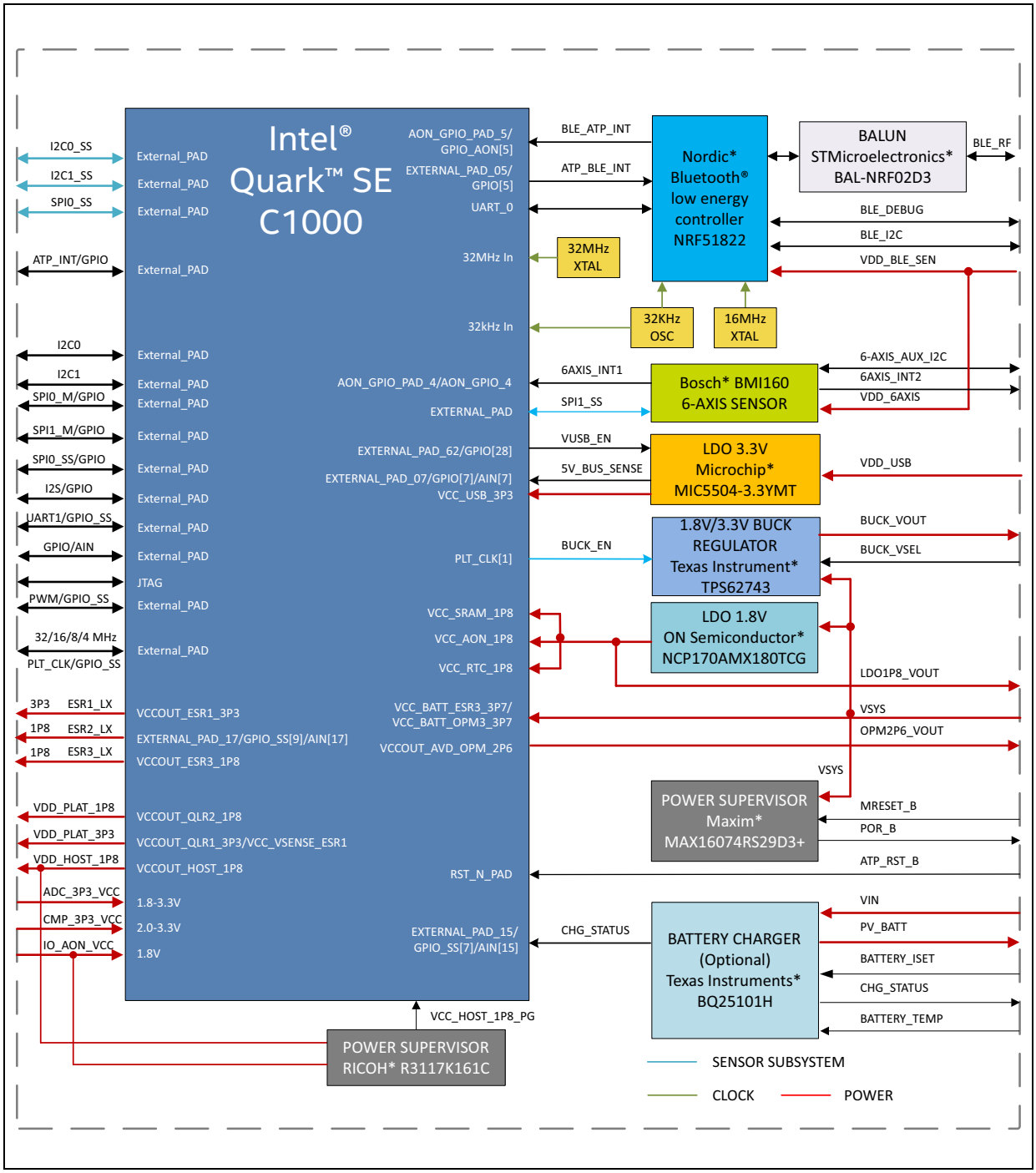
- Block diagram
- Features
- Bluetooth® low energy controller
- Sensor device
- Memory

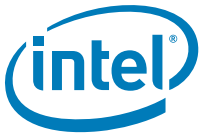
1. Note that this module is not a FCC-certified module. Emission testing has been performed and designs based on the Intel® Curie™ module that have FCC certification are available, but all new designs based on the module require regulatory approval prior to public availability.

3.1 Block diagram

Figure 3-1 depicts the main functional blocks and discrete devices within the Intel® Curie™ module.

Figure 3-1. Intel® Curie™ module block diagram





3.2 Features

This section lists the features of the components and interfaces included in Intel® Curie™ module.

3.2.1 Processor cores

The Intel® Curie™ module integrates an Intel® Quark™ SE microcontroller C1000 processor core and an ARC* EM4 DSP core-based sensor subsystem running on:

- 32-bit processor with 32-bit data bus
- 32 MHz clock frequency
- 32-bit address bus

3.2.1.1 Intel® Quark™ SE microcontroller C1000 processor core

- Pentium x86 ISA-compatible without x87 floating point unit
- 8 kB L1 instruction cache
- Low-latency data tightly-coupled memory (TCM) interface to on-die SRAM
- Integrated local APIC and I/O APIC

The *Intel® Quark™ SE Microcontroller C1000 Datasheet* provides additional details on the core processor.

3.2.1.2 ARC* EM4 DSP core-based sensor subsystem

The Intel® Curie™ module contains an ARC* EM4 DSP-based sensor subsystem and interrupt controller with the following features:

- 8 kB L1 instruction cache and 8 kB of closely coupled memory for data
- Four counters that can be used in PWM or timer mode. The timer mode supports 32-bit operation at 32 MHz granularity. These timers can be configured and used by both cores.
- One configuration watchdog timer with support to trigger an interrupt and/or a system reset upon timeout. This timer can be configured and used by both cores.

3.2.2 Memory subsystem

- 384 kB of on-die flash
- 80 kB of on-die SRAM

3.2.3 Six-axis accelerometer/ gyroscope

The Intel® Curie™ module includes a Bosch* BMI160 six-axis sensing device connected to the SPI1_SS interface port; only the ARC* processor core can communicate with this logical block.

The key features of the Bosch BMI160 integrated device include:

- SPI interface from the ARC processor core to the six-axis sensor to configure and read sensor data.

- GPIO_AON[4] is used to receive interrupt from the six-axis sensor when data is available or when an error condition occurs. The ARC core can be configured to receive this interrupt to process the information.
- Hardware synchronization of inertial sensor data
- Available I^2C from the Bosch* BMI160 6-axis sensing device to interface with compatible, external geomagnetic / magnetometer devices.
- 16-bit digital, tri-axial accelerometer
- 16-bit digital, tri-axial gyroscope
- Ability to average sampled data for more accuracy and improve the ARC core performance by reducing its processing time.
- Sleep or standby mode to support low-power applications
- Separate power supply for the sensor block, allowing the application to turn it off and on as needed to reduce the power consumption.

Note: Refer to Bosch* BMI160 datasheet for more detailed information.

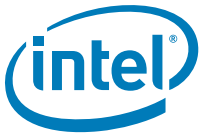
3.2.4 Bluetooth® low energy integration

The Intel® Curie™ module includes a Nordic* nRF51822 that is interfaced to the Intel® Quark™ SE microcontroller C1000 core via UART0.

All the low-level Bluetooth® low energy controller operations are handled by the Bluetooth low energy stack in the device. This makes the application implementation easier by treating the device as a modem and not worry about affecting all the Bluetooth® low energy low level activity because of the application code.

Features of this integrated device include:

- A 32-bit processor with AES hardware encryption
- 2.4 GHz transceiver
- Firmware update via DFU boot-loader, JTAG interface and Over-the-Air (OTA) methods
- Nordic S130 SoftDevice* software that supports Bluetooth 4.1 services and the Gazell™ protocol stack at the same time.
- Low-power sleep mode when not transmitting nor receiving messages. The stack can be configured in this mode without the application real time involvement saving processor real time cycles.
- The Bluetooth® low energy controller can receive or transmit messages while in sleep state, waking the Intel® Quark™ SE microcontroller when done and is also able to interrupt the core via GPIO_AON[5].
- The Bluetooth® low energy blocks are powered separately, allowing the application to turn it off and on as needed to reduce the power consumption. Ensure that there is no leakage or conflict between the blocks when one section is powered down with the others being powered up.



3.2.5 Pattern matching engine

The pattern matching engine (PME) is capable of learning and recognizing patterns in arbitrary sets of data. It is a parallel data recognition engine with the following features:

- 128 parallel arithmetic units (Processing Element or PE) with 8-bit features per PE
- Two pattern matching algorithms:
  - K Nearest Neighbors (KNN)
  - Radial Basis Function (RBF)
- Two distance evaluation norms with 16-bit resolution:
  - L1 norm (Manhattan Distance)
  - Lsup (Supremum) norm (Chebyshev Distance)
- Constant recognition time
- Vector data: up to 128 bytes
- Classification states:
  - ID - identified, only one category matches
  - UNC - uncertain, more than one category matches
  - UNK- unknown, no match
- Support for up to 32,768 categories
- Support for up to 127 contexts
- Supervised learning
- Save and restore network knowledge
- Three main operations supported:
  - Recognize a vector
  - Save the knowledge base from the network
  - Load the knowledge base to the network

3.2.6 USB device

- Single USB 1.1 device port
- Supports full speed (12 Mbps) operation.
- UART mode profile support
- Core detection of USB connected state via a comparator on GPIO[7]/AIN[7] (USB supply VDD_USB is connected to this interrupt).
  - AIN[7] is the interrupt line that will notify the Intel® Quark™ SE microcontroller that a USB voltage is present and thus enable the LDO via firmware. This feature only works with 5V USB sources, it will not detect a 3.3V USB source connection.
- The regulated USB 3.3V LDO supply is software controllable by setting (VUSB_EN) GPIO[28]=0 to disable or =1 to enable.

3.2.7 I²C

- Four I²C master interfaces: two on the Intel® Quark™ SE microcontroller processor core and two on the sensor subsystem (ARC* processor core)
- Three I²C speeds supported:
  - Standard mode (100 kbps)
  - Fast mode (400 kbps)
  - Fast mode Plus (1 Mbps) supported for the two I²C on the Intel® Quark™ SE microcontroller processor core only
  - These can also be configured as slave with a maximum data rate of 400 kbps for the ARC-only I²C
- Support for both 7-bit and 10-bit addressing modes
- Support for 8-entry transmit and 8-entry receive FIFO
- Support for hardware DMA that allows data transfer without CPU involvement
- Support for FIFO threshold setting to generate an interrupt for applications to retrieve received data or when multiple bytes have completed transmission

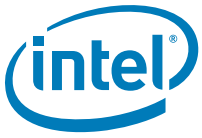
Note: Refer to the block diagram for I²C ports that are accessible by the main processor core and the ARC processor core.

3.2.8 I²S

- Two I²S interfaces – one transmit interface and one receive interface. Each interface supports two channels for stereo left and right channels.
- Sample size from 12- to 32-bits
- Support for Left Justified, Right Justified and DSP modes
- Each interface can operate in Master or Slave mode.
- FIFO mode supporting four words of selected data size transmit and receive for each channel.
- Support for hardware DMA that allows data transfer without CPU involvement.
- Audio sample rates up to 48 kHz
- Support for FIFO threshold setting to generate an interrupt for applications to retrieve received data or when multiple bytes have completed atransmission.

3.2.9 UART

- One of two 16550-compliant UART interfaces available to user (UART1); UART0 dedicated to the Bluetooth® low energy controller
- Baud rates from 300 baud to 2 Mbaud
- Hardware and software flow control
- FIFO mode support (16 bytes Tx and Rx FIFOs)
- Hardware DMA with configurable FIFO thresholds
- Hardware, software and no flow control



3.2.10 SPI

The Intel® Curie™ module exposes three master SPI ports:

- Two from the Intel® Quark™ SE microcontroller processor and ARC* processor cores, and one from the sensor subsystem (only accessible through the ARC core)
- One of the ARC SPI is used internally to communicate with the 6-axis sensing device (SPI1_SS)
- Master SPI clock frequencies from 488 hz up to 16 MHz
- One SPI slave interface with support for SPI clock frequencies up to 3.2 MHz (accessible from either the ARC processor core or from the Intel Quark microcontroller core).
- 1-4 chip select lines per each master SPI interface and one for slave interface
- Five slave select pins per master interface
- Support for 4-bit up to 16-bit frame size
- Eight word (4-16 bits) entry for TX and RX FIFOs
- Hardware DMA with configurable FIFO thresholds
- Configurable clock phase and polarity

3.2.11 DMA controller

The DMA engine can be configured and can start performing data transfer without using the CPU in real time to perform the transfer, thus improving performance and reducing the power consumption.

- Eight unidirectional channels
- Support for 16 hardware handshake interfaces
- Dedicated hardware handshaking interfaces with peripherals plus software handshaking support
- Single and multi-block transfers
- Supported transfer modes[1]:
  - Memory to Memory
  - Peripheral to Memory
  - Memory to Peripheral
  - Peripheral to Peripheral

1. Please note that peripherals for the sensor subsystem are not supported by the DMA controller.

3.2.12 GPIO subsystem

Two sets of GPIO signals are available; the ARC* processor core can access its private group of GPIO lines and another set is accessible by both the ARC* processor core and the Intel® Quark™ SE microcontroller C1000 processor core.

There are 54 GPIOs coming from the Intel® Quark™ SE microcontroller C1000 processor core (see the section 1.10 in the Intel® Quark™ SE microcontroller C1000 datasheet). Out of the 54 GPIOs, 12 GPIOs are used internally for Intel® Curie™ Module, and 42 are available out of Intel® Curie™ Module.

3.2.12.1 GPIO controller features

- All GPIOs are interrupt-capable supporting level-sensitive and edge-triggered modes.
- De-bounce logic for interrupt source
- Four external and two internal awake-ON interrupts and wake-capable GPIOs
- Up to four digital inputs and up to four analog inputs that can also can be used as digital I/O; configuration dependent.
- Four pulse width modulated outputs that can be configured as digital I/O lines.
- Separate data register bit and data direction control bit for each GPIO
- GPIO registers retain their state during sleep and wake events.
- Software selectable drive strength via internal pull-up; unused lines must be configured as inputs with internal pull-up or as GPIO with output set to low, or set as input with external pull-up.
- Interrupt mode supported for all GPIOs, with the following configuration:
  - Active High Level
  - Active Low Level
  - Rising Edge
  - Falling Edge
  - Both Edge

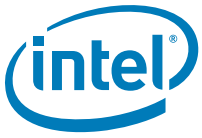
3.2.12.2 GPIO of Intel® Curie™ module

The Intel® Curie™ module includes 54 GPIOs in total:

- Four external AON interrupts
- Two internal wake-capable GPIO lines
- Four lines used for analog input for the ADC mux
- 32 GPIO/multifunction lines; these can be configured as GPIO if not consumed by other I/O signals. Refer to the Intel® Quark™ SE microcontroller datasheet for more information.
- 12 GPIO lines used internally within the module

The module internal GPIO signals are 12 in total: three are dedicated to the ARC* processor core, nine are shared and can be configure for either core. These are used internally for control or monitor/interrupt functions.

GPIO mapping tables are provided in section Section 1.3.10



3.2.13 Timers and pulse width modulator (PWM)

- Four counters capable of operating in PWM mode or in timer mode
- Configurable PWM high and low time with granularity of a single 32 MHz clock period per output
- Timer mode support for 32-bit timer operating at 32 MHz
- Two timers for the ARC* processor core and two timers for the Intel® Quark™ SE microcontroller processor core that can also be accessed by the ARC core.
- ARC* processor core timers can be configured as watchdog timers.

Note: PWM keep their state when going to sleep mode, allowing the application to set the wake configuration.

3.2.14 Analog comparators

- 19 analog comparators
  - — Six high-performance comparators
  - — 13 low-power comparators
- Configurable polarity
- Interrupt and wake event capable
- Can be used with any of the AIN external pins or can be internally connected between the SoC and the resources on the Intel® Curie™ module.
- Wake events support by the low-power comparator interrupt
- Comparator for Interrupt/wake event generation based on programmed match value
- Each comparator can be powered down to achieve even lower power.

3.2.15 Watchdog timer (WDT)

- Configurable watchdog timer able to issue an interrupt and/or a system reset upon timeout.
- Selectable timeout value settable between ~2ms and ~60s (at 32 MHz)
- Interrupt generation on first timeout
- If the interrupt has not been cleared by the second timeout, the WDT requests a microcontroller warm reset to recover for an application program error or unexpected condition.

3.2.16 Real-time clock (RTC)

- 32-bit counter running from 1 Hz up to 32.768 kHz
- Supports interrupt and wake event generation upon matching a programmed value
- Only requires a running 32.768 kHz clock to generate interrupt and wake events
- Supports an additional 32-bit always-on counter
- Supports a 32-bit always-on timer with interrupt and wake capability

3.2.17 Analog-to-digital converter (ADC) unit

- Five analog inputs AIN_10 – AIN_14, 11 other possible analog inputs using alternate functions
- The ADC controller is only accessible from the ARC* processor core and the DMA controller. All configuration and read access is via ARC software.
- Successive-approximation engine with selectable resolution (6, 8, 10 or 12 bit)
- 2.24 MSPS conversion rate – See the *Intel® Quark™ SE Microcontroller C1000 Datasheet* for more details.
- Internal voltage regulator and digital calibration algorithm to improve accuracy
- Only single-ended input options supported
- The digital offset calibration block aids the measurement and correction of the offset voltage for the ADC. This needs to be done after selection of the input pin and the temperature or supply voltage changes. Many applications do not require this type of accuracy and in that case initial calibration should be acceptable and re-calibration may not be required.
- ADC resolution set via ADC_RES[1:0] register; lower bit resolution can be sampled faster than the 12-bit maximum.
  - 11 = 12 bit
  - 10 = 10 bit
  - 01 = 8 bit
  - 00 = 6 bit.
    Note that a lower number of bits can be sampled quicker in less clock cycle than the 12-bit maximum number of bits.
- The ADC supply voltage must match the AIN supply voltage and COMP_AREF to meet the voltage requirement.

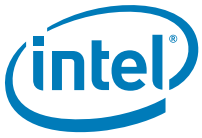
Note: The ADC block is sensitive to any noise from the digital IO, RF, Ground and VCC that may affect the accuracy of sampling. We recommend averaging samples, adding filtering to the input and increasing the number of clocks for the samples.

3.2.18 Interrupt

The interrupt is described in the Intel® Quark™ SE microcontroller datasheet.

The interrupt controller to either Intel® Quark™ SE microcontroller processor core or to the sensor subsystem is provided in the system control subsystem, and has the following features:

- Configurable interrupt priority
- Level or pulse sensitivity
- Fast interrupt support for the sensor subsystem second register bank for context switching without saving and restoring registers
- Interrupt vector mapping showing the vector number and associated peripheral, core and co-processor
- Interrupt wake event supported only by the AON signals identified by AON (Awake On / Always On) name



3.2.19 Power management

3.2.19.1 Power supply

The Intel® Curie™ module operates under battery-operated systems using 3.3 V or 1.8 V interfaces, or may be powered by external regulators that provide 1.8 V or 3.3 V. The regulators inside Intel® Curie™ module are used to power the internal circuits or the platform applications: ESR3 is the 1.8 V power regulator used to power the internal circuits, ESR 1 is the 3.3 V power regulator used by external platform devices, and ESR2 is the 1.8 V power regulator used by external platform devices.
An integrated power supervisor holds the system in reset when the input voltage drops below 2.9 V. An inductor and a bulk capacitor are used with the power regulators. VDD_BLE_SEN is the core voltage used to supply the internal Bluetooth® low energy controller. AON_IO_VCC controls the supply voltage to the IO level (1.8 V or 3.3 V) for the peripheral interfaces.
Refer to Section 2.2, "Power and timing considerations" for more details on power management.

3.2.19.2 Power states

Section 2.2.4, "Device power states" describes the Active, Sleep and Off states of the Intel® Curie™ module.

Section 2.2.6, "Boot and reset sequences" describes the power-up sequence that changes the Intel® Curie™ module mode from Off to Active.

Within the Intel® Quark™ SE microcontroller, the Intel Quark SE microcontroller processor core has three main power states: Active, Sleep and Off. The power consumption can be less than 1 uA in Sleep mode.The sensor subsystem also has three power states: sensing active, sensing wait and sensing standby. The power consumption can be as low as 250 uA in low-power sensing standby.
Refer to the Intel® Quark™ SE microcontroller C1000 datasheet for details on the SoC power management.

Section 3.3.1, "Power" provides an overview of the power management for the Bluetooth® low energy controller.

Section 3.4.2, "Power" provides information on the power management of the 6-axis sensing device.

The 3.3 V LDO voltage regulator comes with an active-high enable pin that allows the regulator to be disabled. Forcing the EN low disables the regulator and sends it into an off current state drawing virtually zero current. When disabled, the 3.3 V LDO voltage regulator switches an internal 25 ohm load on the regulator output to discharge the external capacitor. Refer to Microchip* MIC5504-3.3YMT datasheet for more information.

The 1.8 V LDO voltage regulator uses the EN pin to enable and/or disable the device and activate or deactivate the active discharge function. If the EN pin voltage is pulled below 0.4 V, the 1.8 V LDO regulator is guaranteed to be disabled, the Active Discharge Feature is activated and the output voltage is pulled to GND through an internal circuitry with effective resistance of about 100 ohm. iI the EN pin voltage is higher than 1.2 V, the 1.8 V LDO voltage regulator is guaranteed to be enabled. The internal active discharge circuitry is switched off and the desired output voltage is available at the output pin. Refer to ON Semiconductor* NCP170 AMX180TCG datasheet for more information.

Texas Instrument * TPS62743 bulk step-down converter operates in Power Save mode at light loads, and in Pulse Width Modulation (PWM) mode for medium and high load conditions. During PWM mode, the bulk converter operates in continuous conducting mode. The switching frequency is typically 1.2 MHz with a controlled frequency variation depending on the input voltage and load current. If the load current decreases, the converter enters the Power Save mode to maintain high efficiency down to very light loads. The transition from PWM to Power Save mode is seamless with minimum output voltage ripple. Refer to Texas Instrument * TPS62743 datasheet for more information.

3.2.20 Clock management

The system clock has the features listed hereafter. Specific properties are listed in Table 3-1. The accuracy of the clock is maintained within the operating temperature range.

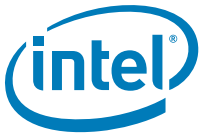
- Dynamic frequency scaling
  - The clocks can be reduced for all blocks—including the Intel® Quark™ SE microcontroller C1000 core, the ARC* processor core, the pattern matching engine, the AHB bus, and the peripherals—to reduce power consumption.
- Dynamic clock gating
  - For example the SPI master clock can be gated off when not sending data to a peripheral and gated back on when the SPI is in use again.
- Autonomous state-based clock gating and autonomous peripheral clock gating
- The 32 kHz clock is a MEMS-based temperature-compensated clock that feeds both the Intel® Quark™ SE microcontroller and the Nordic* Bluetooth® low energy controller. It is always running when power is supplied. Its primary use is for the real time clock and software timer.
- The 32 MHz XTAL oscillator must be used to meet the UART timing

Table 3-1. Intel® Curie™ module system clocks

Clock	Use	Accuracy
32 kHz	Always on timer. 32 kHz oscillator for RTC	±5ppm
SoC Silicon oscillator 4/8/16/32 MHz	Enabled at boot time	±20,000ppm
SoC XTAL oscillator - 32 MHz	Required for USB operation and timing. Can be enabled by software	±30ppm
16 MHz Bluetooth® low energy controller clock	Active during Bluetooth® low energy transmit/ receive	±30ppm

3.2.21 Test and debug

- Test and debug for Intel® Quark™ SE microcontroller
  - Five-pin IEEE 1149.1 JTAG interface
  - Boundary scan support
  - Intel® Quark™ SE microcontroller processor minutia debugger
- ARC* metaware debugger
- Serial Boot Loader
- Test and debug on separate hardware and out of Intel® Curie™ Module
  - Bluetooth® low energy debug and programming via J-Link / SWD emulator



3.3 Bluetooth® low energy controller

The Intel® Curie™ module incorporates a Nordic* nRF51822, which is built around a 32-bit central processing unit with 256 kB of embedded flash and 16 kB of RAM for improved application performance. The embedded 2.4 GHz transceiver supports Bluetooth® low energy as well as Nordic Gazell 2.4 GHz protocol stack. The Bluetooth® low energy controller interfaces with the Intel® Quark™ processor core within Intel® Quark™ SE microcontroller C1000 via UART0.

The Quark processor core software sends commands and receives status and messages from the Nordic* S130 Bluetooth® low energy protocol stack that runs in the Bluetooth® low energy controller and acts like a modem to simplify the software design.

Refer to Nordic* nRF51822 Bluetooth® low energy controller product specification for more details about the device.

3.3.1 Power

The Bluetooth® low energy controller supports three power supply alternatives:

- Internal LDO setup
- DC/DC converter setup
- Low-voltage mode setup

The internal LDO setup can be used with DC/DC converter bypassed, and the system power is generated directly from the supply voltage VDD. The internal LDO can also be used in combination with the DC/DC converter setup. The low voltage mode setup is for devices that are used in low-voltage mode where a steady 1.8 V supply is available externally.

The Bluetooth® low energy controller is powered by the 1.8 V discrete BULK regulator inside the Intel® Curie™ module. There are no hardware handshaking signals that control the power state of the Bluetooth® low energy controller.

In Intel® Curie module, VDD_BLE_SEN is the core voltage supply for the Bluetooth® low energy controller. BLE_DEC2 is the power supply decoupling signal used for 1.8 V IO connections to VDD_BLE_SEN.

Within the Bluetooth® low energy controller the power management is highly flexible with functional blocks such as the CPU, the radio transceiver and the peripherals for which the power state controls are separate, in addition to the global ON and OFF modes.

- In system OFF mode, the Bluetooth® low energy controller is in the deepest power saving mode. The system core functionality is powered down and all ongoing tasks are terminated. Only the Pin wakeup functionality can be setup to be responsive. One or more blocks of RAM can be retained and the device state can be changed to system ON through Reset, the GPIO DETECT signal, or the LPCOMP ANADETECT signal.
- In system ON mode the system is fully operational. The CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending whether the Low power or the constant latency sub-power mode is selected. All the functional blocks are independently in RUN or IDLE mode depending on the needed functionality.

In Low Power mode the automatic power management system is optimized to save power by keeping as much as possible of the system powered down.
In Constant Latency mode the system is optimized for keeping the CPU latency and the Programmable Peripheral Interconnect (PPI) task response constant and at a minimum, by forcing a set of base resources ON while in sleep mode. This results in higher power consumption for the system.

The Nordic* S130 Bluetooth® low energy protocol stack provides configuration parameters to allow the device to go to sleep when idle. Alternately the controller can be powered by external sources for direct activation to create application specific states.

3.3.2 Clock

Intel® Curie™ module provides the 16 MHz (run) and 32 kHz (standby) clocks to the Bluetooth® low energy controller;

- 16 MHz XTAL clock
- 32 kHz clock oscillator shared between Bluetooth® low energy and the Intel® Quark™ SE microcontroller

In Intel® Curie module, BLE_CL is the I^2C clock interface pin used for the Bluetooth® low energy controller.

3.3.3 Interfaces

The following blocks of the Nordic* nRF51822 interface with other devices within the Intel® Curie™ Module.

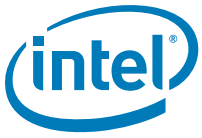
- Universal Asynchronous Receiver/Transmitter 0 (UART0) is the interface with Intel® Quark™ processor core
- Clock management (CLOCK) is the interface with the 16 MHz XTAL and the 32 kHz OSC clocks
- The 2.4 GHz radio (RADIO) is connected to the Balun transformer (STMicroelectronics* BAL-nRFD203) via the ANT1 and ANT2 interface pins
- The Two-Wire Interface (TWI) that communicates with a bi-directional wired-AND bus with two lines (SDA and SCL)
- The two-pin Serial Wired Debug (SWD) interface is part of a serial Debug Access port

3.3.4 2.4 GHz radio

The 2.4 GHz RF transceiver operates in the ISM frequency band at 2.400 to 2.4835 GHz. The transceiver receives and transmits data directly from the system memory for efficient packet data management.

The 2.4 GHz multi-protocol radio has the following characteristics:

- +4 dBm to -20 dBm output power in 4 dBm steps; default TX power of 0 dBm
- -30 dBm output power in whisper mode
- Adjustable data rates and power levels at the application level, dependent upon driver and API



3.3.5 Signals

Table 2 lists all the signals used with the Bluetooth® low energy controller, and their function. Also see Section 1.3.12, "Bluetooth® low energy controller pins".

Table 2. Bluetooth® low energy controller signals

Ball Name	Description
ATP_BLE_INT	Input interrupt signal from Intel® Quark™ SE microcontroller to the Bluetooth® low energy controller
BLE_ATP_INT	Output interrupt signal from the Bluetooth® low energy controller to Intel® Quark™ SE microcontroller
BLE_SW_CLK	Intel Curie module pin D24. This signal has a 22 kohm internal pull-down resistor to keep it from floating. Signal used with the J-Link emulator to program or debug the Bluetooth® low energy controller.
BLE_SWDIO	This signal has a 22 kohm internal pull-down resistor to keep it from floating. Signal used with the J-Link emulator to program or debug the Bluetooth® low energy controller.
BLE_SDA	I^2C interface data output signal from the Bluetooth® low energy controller to an external master. Requires an external pull-up
BT_GPIO	GPIO output signal from the Bluetooth® low energy controller
BLE_SCL	I^2C interface output clock signal from the Bluetooth® low energy controller to an external device (optional)
BLE_RF	Input/output signal used for the connection of the Bluetooth® low energy controller to the antenna via the BALUN (balanced/unbalanced) transformer
BLE_DEC2	Power supply decoupling. Leave unconnected for 3.3 V IO. Used for 1.8 V IO connection to VDD_BLE_SEN
VDD_BLE_SENS	Bluetooth® low energy controller power supply with internal 0.1 uF capacitor.
UART0_CTS	UART0 interface line input signal from Intel Quark processor core to Bluetooth® low energy controller, used for flow control
UART0_TXD	UART0 interface line transmitter output signal from the Bluetooth® low energycontroller to Intel Quark processor core
UART0_RTS	UART0 interface line output signal from the Bluetooth® low energycontroller to Intel Quark processor core, used for flow control
UART0_RXD	UART0 interface line receiver input signal from Intel Quark processor core to the Bluetooth® low energy controller

3.3.6 Software stack support

The Nordic* S130 Bluetooth® low energy protocol stack provides concurrent multi-link Central, Peripheral, Broadcaster, and Observer roles. The S130 series SoftDevice is compliant with Bluetooth® 4.1 and the SoftDevice enables Bluetooth network topologies.

3.3.7 Programming and debug

Multiple methods are available to load a software image into the Bluetooth® low energy section:

- If USB is implemented for the application, it can be used to load an image using the DFU utility.
- The JTAG programmer (Flyswatter2* or J-Link) supported by the Intel® Quark™ SE microcontroller can be used to load the image. Refer to the Nordic website for other ways to load an image to the Bluetooth low energy block.
- Software solutions can be used to receive the image from UART and use Over-the-Air to program it.

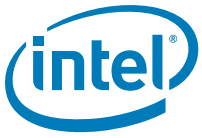
3.4 Sensor device

The Bosh* BMI160 is a 16-bit inertial measurement unit designed for low-power, low-noise and high precision 6-axis and 9-axis applications. The inertial measurement unit combines the data captured from the tri-axis low-g accelerometer and the 3-axis gyroscope. The 16-bit tri-axial accelerometer detects the linear motion and gravitational forces. The 16-bit tri-axial gyroscope measures the rate of rotation in space. The 6-axis sensor device is capable of handling external sensor data, for example geomagnetic or barometric pressure sensors.

Refer to Bosch* BMI160 datasheet and software library support.

3.4.1 Feature summary

- Digital resolution
  - Accelerometer (A): 16 bit
  - Gyroscope (G): 16 bit
- Measurement ranges (programmable)
  - (A): ± 2 g, ± 4 g, ± 8 g, ± 16 g
  - (G): ± 125°/s, ± 250°/s, ± 500°/s, ± 1000°/s, ± 2000°/s
- Sensitivity (calibrated)
  - (A): ±2g: 16384 LSB/g
  - ±4g: 8192 LSB/g
  - ±8g: 4096 LSB/g
  - ±16g: 2048 LSB/g
  - (G): ±125°/s: 262.4 LSB/°/s
  - ±250°/s: 131.2 LSB/°/s
  - ±500°/s: 65.6 LSB/°/s
  - ±1000°/s: 32.8 LSB/°/s
  - ±2000°/s: 16.4 LSB/°/s
- Zero-g offset (typ., over life-time)
  - (A): ±40 mg
  - (G): ± 10°/s



- Noise density (typ.)
  - (A): 180 µg/vHz
  - (G): 0.008°/s/vHz
- Bandwidths (programmable)
  - 1600 Hz … 25/32 Hz
- Temperature range
  - -40 … +85°C
- Current consumption
  - full operation = 950 µA
  - low-power mode = 3 µA
- FIFO data buffer
  - 1024 byte
- Shock resistance
  - 10,000 g x 200 µs

3.4.2 Power

Within Intel® Curie™ module, the VDD_6AXIS signal brings the power supply to Bosh* BMI160 device. The 6-axis sensing device is powered by the 1.8 V discrete BULK regulator inside Intel® Curie™ module. There are no hardware handshaking signals that control the power state of the sensing device. The power management configuration is done by software through the SPI interface with the ARC* processor core.

The built-in power management unit (PMU) of the 6-axis sensing device can be configured for example to further lower the power consumption by automatically sending the gyroscope into fast start-up mode and waking it up again by internally using the any-motion interrupt of the accelerometer.

By default the accelerometer and the gyroscope are in suspend mode after powering up the device. The device powers up in less than 10 ms.

The accelerometer has the following power modes:

- Normal mode: full operation
- Low-power mode: duty cycling between suspend and normal mode. FIFO data readout supported to a limited extent.
- Suspend mode: no data sampling, all data is retained and delays between subsequent I^2C operations are allowed. FIFO data readout is not supported.

The gyroscope has the following power modes:

- Normal mode: full operation
- Suspend mode: no data sampling, all data is retained and delays between subsequent I^2C operations are allowed. FIFO data readout is not supported.
- Fast start-up mode: start-up delay time to normal mode takes 10 ms or less

Suspend and fast start-up modes are sleep modes. Switching between normal and low power mode does not impact the output data from the sensor. This allows the system to switch from low power mode to normal mode to read out the sensor data in the FIFO with a data rate limited by the serial interface.

The power mode setting can be configured independently from the output data rate. The main difference between normal and low power modes is the power consumption. The highest current consumption occurs when both the accelerometer and the gyroscope are in normal mode, and reaches 925 uA. When both the accelerometer and the gyroscope are in suspend mode, the power consumption is of 3 uA.

When an external magnetometer is connected via the secondary I^2C interface in Intel® Curie™ module, the power management unit allows advanced power management, and supports the three power modes for the magnetometer: suspend, normal and low power.

3.4.3 Sensor timing

The register SENSORTIME is a free-running counter which increments with a resolution of 39 us. All sensor events such as the updates of data registers are synchronous to the SENSORTIME register. The time stamps in the SENSORTIME register are available independently of the power mode of the device.

3.4.4 Data synchronization

The sensor time is synchronized with the update of the data register. Synchronization is a digital statement.

The sensor data from the accelerometer and the gyroscope are strictly synchronized on hardware level. That is, they run on exactly the same sampling rate. Bosch* BMI160 supports various levels of data synchronization. See the Bosch* BMI160 datasheet for the list of supported data synchronization.

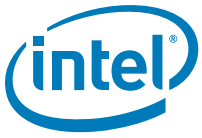
3.4.5 Data processing

The data from the sensor is always sampled with a data rate of 6400 Hz for the gyroscope and 1600 Hz for the accelerometer. The data processing implements a low pass filter configured in the register ACC_CONF for the accelerometer, and GYR_CONF for the gyroscope. Further down sampling for the interrupt engines and the FIFO is possible and configured in the register FIFO_DOWNS. This down sampling discards data frames.

3.4.6 FIFO

The FIFO block integrated in the Bosch* BMI260 sensing device is used to support low power applications and to prevent data loss in non-real time systems. The FIFO space for the accelerometer and the gyroscope is dynamically allocated.

Data is stored in the FIFO in data frame units. The frame rate for the FIFO is defined by the maximum output date rate of the sensors enabled via the register FIFO_CONFIG. If the setting for pre-filtered data is selected in the register FIFO_DOWNS, the data rate for the gyroscope is 6400 Hz and it is 1600 Hz for the accelerometer. The frame rate



can be further reduced by selecting the down sampling setting for each or both sensors in FIFO_DOWNS register. Down sampling decreases the sensor data rate. During down sampling no data processing nor data filtering are performed.

Refer to the Nordic* nRF51822 datasheet to see details on the FIFO frame configurations.

3.4.7 Interfaces

In Intel® Curie™ module, the Bosch* BMI260 sensing device primary SPI interface is used to connect to the ARC* processor core. On the ARC* processor core, the SPI interface is SPI1_SS.

Also in Intel® Curie™ module, the Bosch* BMI260 sensing device secondary I^2C interface can be used to connect to a magnetometer and achieve some 9-axis (9AXIS) sensing capability. When connected to a geometric sensor, the Bosh* BMI160 triggers autonomous read-out of the sensor data from the magnetometer without the need for intervention by the ARC* processor core. In this configuration the 6-axis sensing device controls the data acquisition of the external sensor. The synchronized data of all the sensors can be stored in the register data and additionally in the built-in FIFO.The integrated 1024 byte built-in FIFO prevents data loss in non-real time systems.

3.4.8 Interrupt management

The 6-axis sensing device features an on-chip interrupt engine enabling low-power motion-based gesture recognition and context awareness such as any-or no-motion detection, tap or double tap sensing, orientation detection, free-fall or shock events.

There are two output interrupt pins, to which 13 different interrupt signals can be mapped independently via user programmable parameters.

The available interrupts supported by the accelerometer in normal mode are:

- Any-motion (slope) detection
- Significant motion
- Step detection
- Tap sensing (detection of single or double tapping events)
- Orientation detection
- Flat detection
- Low-g/high for the detection of very small or very high accelerations
- No/slow motion

There are two additional common interrupts for the accelerometer and the gyroscope:

- Data ready (“new data”) for synchronizing the sensor data read-out with the ARC* processor core
- FIFO full/FIFO watermark, to handle the FIFO fill level and overflow

The interrupts are available in normal and low-power modes, but not in suspend mode.

The 6-axis sensing device can interrupt the external magnetometer to coordinate the communication to it. It can also interrupt the ARC* processor core when it needs priority attention.

In Intel® Curie™ module, GPIO_AON[4] in Intel® Quark™ SE microcontroller receives the interrupt signal 6AXIS_INT1 from the 6-axis sensing device when data is available.

3.4.9 Signals

Table 2 lists all the signals used with the Bosch* BMI2606-axis sensor, and their function. Also see Section 1.3.11, "6-Axis sensing device pins".

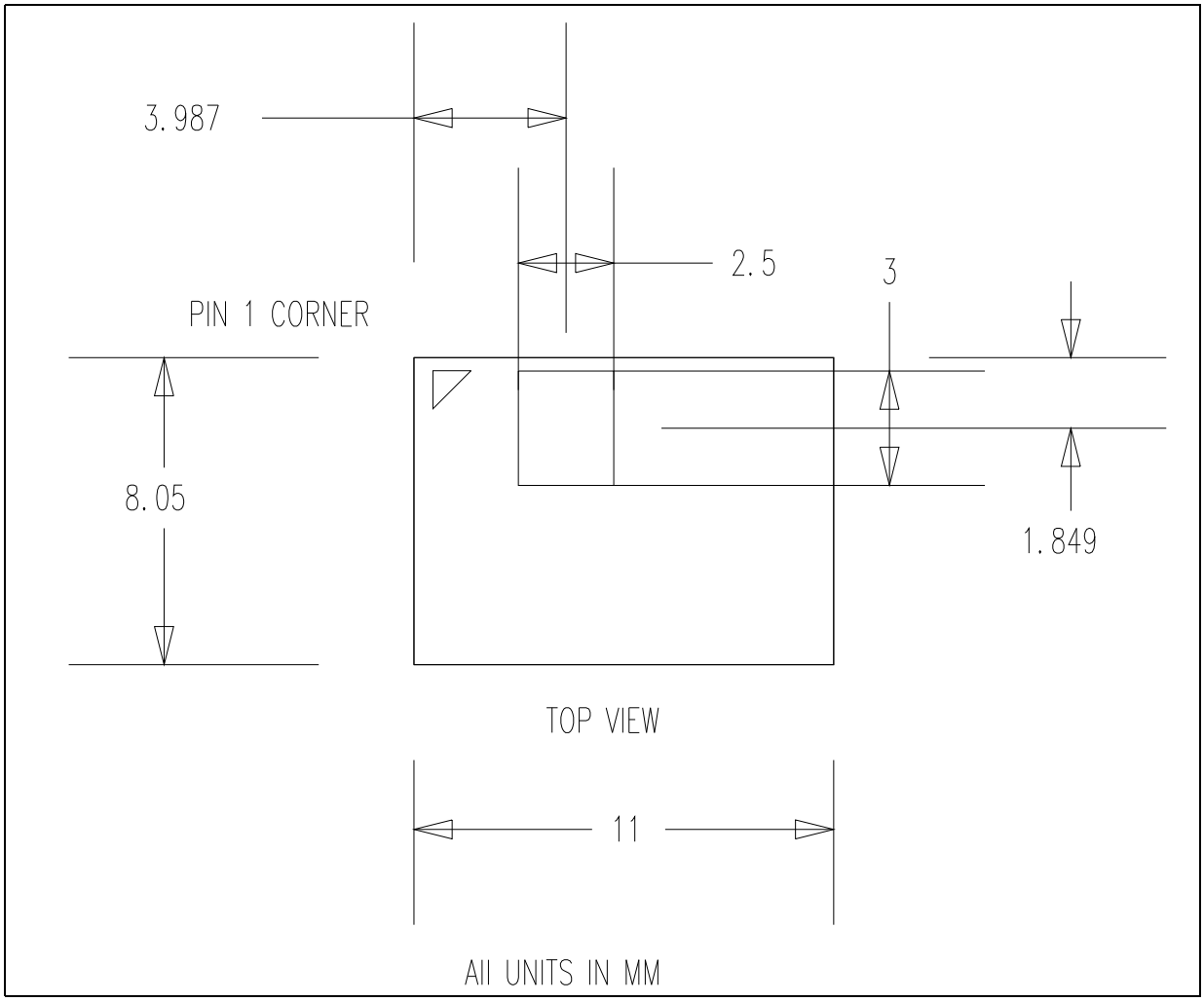
Table 3. Bosch* BMI260 6-axis Sensing Device Signals

Ball Name	Description
6AXIS_MISO	6-axis sensor SPI interface master input slave output signal
6AXIS_MOSI	6-axis sensor SPI interface master output slave input signal
6AXIS_SCLK	6-axis sensor SPI interface serial clock signal (output from the master)
6AXIS_CS	6-axis sensor SPI interface chip select signal
6AXIS_INT1	Internal interrupt output signal from the 6-axis sensing device to the Intel ARC* processor core
6AXIS_SDA	6-axis sensor I^2C interface serial data line output signal to the an external magnetometer to get a 9-axis sensing device. Requires external pull-up
6AXIS_SCL	6-axis sensor I^2C interface serial clock output signal to the an external magnetometer to get a 9-axis sensing. Requires external pull-up.
6AXIS_INT2	6-axis interrupt output signal to an external magnetometer to get 9-axis sensing

3.4.10 Sensor position on Intel® Curie™ module

Figure 3-2 shows the approximate location of the sensor device within Intel® Curie™ module.

Figure 3-2. Intel® Curie™ module X-Y dimensions and position of the six-axis sensor



3.5 Memory

The Intel® Quark™ SE microcontroller C1000 supports two address space mappings:

- Physical address space mappings
- Sensor subsystem auxiliary address space mappings

3.5.1 Memory map

3.5.1.1 Physical address space mappings

There are 4 GB (32 bits) of physical address space that can be used as:

- Memory mapped I/O (MMIO – I/O fabric)
- Physical memory (system Flash/system SRAM/external SRAM)
- System Flash 0: 192 kB (including system ROM)
- System ROM: 8 kB: Write protected section of the Flash that is used as One Time Programmable (OTP) memory for information memory and also for user information like ID or serial number
- System Flash 1: 192 kB
- Internal System SRAM: 80 kB
- 8 kB of Data Closely Coupled Memory (DCCM) in the sensor subsystem

Both the Intel Quark microcontroller core and the ARC* core can access the full physical address space. The ARC* processor core maps the peripherals directly attached to the sensor subsystem to an auxiliary address space that the ARC* processor core has exclusive access to.

All Intel® Curie™ module peripherals, except the ones on the ARC* processor core, map their registers and memory to physical address space. Other devices within the Intel® Curie™ module can only access regions of the physical address space presented to a given device via the multi-layer SoC fabric.

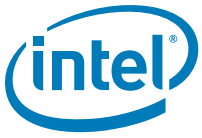
Refer to Intel® Quark™ SE microcontroller datasheet for the memory mapping information.

3.5.1.2 Sensor subsystem auxiliary memory map

The ARC* processor core has access to two physically separate memory spaces.

- The first memory space is the main memory space and is shared with the host processor and SoC peripherals.
- The other memory space is an auxiliary memory space that the ARC* processor core uses to access the peripherals that are directly connected to the sensor subsystem.

Only the ARC* processor core can access the auxiliary memory space.



4 Reference and Resources

4.1 Software support

The Intel® Curie™ Open Developer Kit (ODK) includes the software, tools and documentation for developers to build boards based on the Intel Curie module and turn them into products. Further information and resources for the ODK can be found at:

Intel® Curie™ Open Developer Kit (ODK)

4.2 Related documents

The following documents provide information related to the Intel® Curie™ module and the Intel® Quark™ SE microcontroller C1000:

- Intel® Curie™ Module Design Guide
- Module Power Sequencing for Intel® Curie™ Module
- Intel® Curie™ Modules support page
- Intel® Curie™ Module developer page
- Intel® Quark™ SE Microcontroller C1000 Datasheet
- Intel® Curie™ Module Specification Update

4.3 Intel® Curie™ module-related community resources

For frequently asked questions about the Intel® Curie™ module, please visit Intel® Curie™ Module Support page.

If you need further information or help, or to find and share solutions with Intel® Curie™ module users across the world, please visit Intel® Curie™ Forum in Intel's Support Communities.

4.4 Component reference

The Intel® Curie™ module incorporates the following components. Please see the respective manufacturer’s website for related documentation and other resources:

- SoC: Intel® Quark™ SE microcontroller C1000
- Bluetooth® low energy: Nordic* nRF51822--CEAAE0/PAN V3.0 (Stack S130)
- Balun transformer: STMicroelectronics* BAL-NRF02D3
- 6-axis sensing device: Bosch* BMI160
- Battery charger: Texas Instruments* BQ25101H
- Power supervisor: Maxim* MAX16074RS29D3+T
- Power supervisor: RICOH* R3117K161C
- LDO 1.8 V: OnSemiconductor* NCP170AMX180TCG

- LDO 3.3 V (USB): Microchip* MIC5504-3.3YMT
- Buck regulator 1.8 V/3.3 V: Texas Instruments* TPS62743

Note: Refer to the respective third-party, and Intel® Quark™ SE microcontroller documents as required.

4.5 Terminology

Table 4-1 lists some terms that are used in this document.

Table 4-1. Terminology

Term	Definition
AC	Alternating current
ADC	Analog-to-digital converter
AIN	Analog input
AHB	AMBA high-performance bus is a single clock-edge protocol
AON	Always-on (Wake Event)
ARC*	Argonaut RISC core
Intel® Quark™ SE microcontroller	Intel® Quark™ SE microcontroller C1000 (WLCSP package used in Intel® Curie™ module)
BALUN	Balanced-unbalanced
BLE	Bluetooth® low energy (formerly Bluetooth® Smart)
CPU	Central processing unit
CCM	Counter with CBC-MAC
DC	Direct current
DCCM	Data closely coupled memory
DFU	Device firmware update
DMA	Direct memory access
DMIPS	Dhrystone million instructions per second
DSP	Digital signal processor
ESD	Electrostatic discharge
FIFO	First in first out
GPIO	General-purpose input/output
I^2C	Inter-integrated circuit (bus)
I^2S	Inter-IC sound (bus)
IDE	Integrated development environment
IO, I/O	Input/output
ISA	Instruction set architecture
JTAG	Joint test action group (debugging interface)
LDO	Low-dropout regulator
MSL	Moisture sensitivity level
nCTF	Non critical to function
NVM	Non-volatile memory
ODM	Original design manufacturer
OS	Operating system

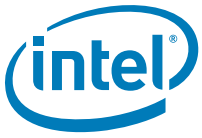


Table 4-1. Terminology (continued)

Term	Definition
OTA	Over the air
OTP	One-time programmable
PCB	Printed circuit board
PCM	Pulse code modulation
PTU	Power transmit unit
PWM	Pulse width modulation
RAM	Random access memory
RTC	Real-time clock
SMT	Surface mount technology
SoC	System on a Chip. Used for the Intel® Quark™ SE microcontroller C1000 in some sections of the document
SPI	Serial peripheral interface (bus)
SRAM	Static random access memory
SW	Software
TBD	To be determined
TCM	Tightly coupled memory
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
WDT	Watchdog timer
XTAL	Crystal

5 Packaging and Ordering

5.1 Package information

This section presents information on Intel® Curie™ module package geometry and package marking.

5.1.1 Packing geometry

Table 5-1 shows details for the Intel® Curie™ module package.

Table 5-1. Module package details

Module Attribute	Value and Tolerance
Package size	11.00 x 8.05 mm ±0.05 mm
Package height	1.95 mm ±0.09 mm
Solder ball material	SAC 1205
Surface finish	CuOSP
Ball count	111
Ball pitch	0.57 x 0.45 mm
Solder result opening	0.240 mm
Ball diameter (pre-attach)	0.308 mm / 12.13 mil
Die thickness	0.240 mm
Substrate thickness	0.70 mm
Maximum Z-height (pre/post SMT)	1.86 mm to 1.95 mm ± 0.09 mm
NCFT corner balls	N/A
Overmold (mold cap showing device identification and marking)	Yes - 1 mm

5.1.2 Package marking

Figure 5-1 shows the marking for Intel® Curie™ module.

Figure 5-1. Package marking

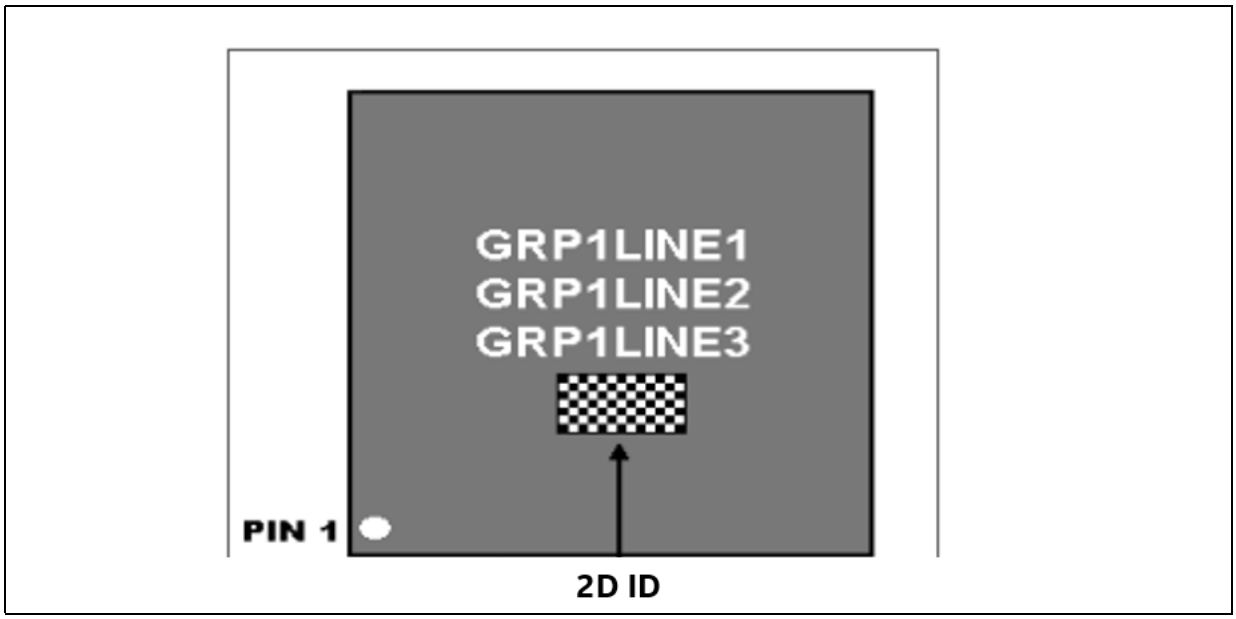


Table 5-2. Package marking

Line Number	Overview	Description
Line 1	-	Intel symbol
Line 2	{FPO}	FPO field number
Line 3	SR2NW {e1}	Product identification (engineering sample of HVM) and Pb-free compliance indicator {e1}

5.2 Ordering information

Table 5-3 provides information on Intel part numbers. Contact your regional sales representative for pricing information.

Table 5-3. Ordering information for Intel® Curie™ module

Part Number (MM#)	Description	Packing
948119 - OBSOLETE[1]	Intel® Curie™ module integrated in Arduino* 101 (branded Genuino* 101 in some countries)	N.A.
949350	Intel® Curie™ module with battery charger, in 11.00 mm x 8.05 mm package	Tray[2]

Notes:

1. These parts cannot be ordered.
2. No being shipped in tape and reel at this time.

5.3 Storage information

Table 5-4 specifies the package storage requirements.

Please note that:

- $T_{ABSOLUTE\ STORAGE}$ applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
- The specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC J-STD-020 and MAS documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
- Post board attach storage temperature limits are not specified. Consult your board manufacturer for storage specifications.

Table 5-4. Package storage specifications

Parameter	Description	Min	Max
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time.	-25°C	125°C
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5°C	40°C
$R_{HSUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24°C	-
$T_{IMESUSTAINED\ STORAGE}$	A prolonged or extended period of time: associated with customer shelf life in applicable Intel® boxes and bags	0 months	6 months

6 Manufacturing Information

6.1 Bootloader information

The Intel® Curie™ module comes with a manufacturing bootloader by default and customers can flash the bootloader of their choice through JTAG.

6.2 PCB pad design guidelines

To achieve the highest solder joint strength and reliability, we recommend the following:

- PCB pad size: 10 mil, MD pad
- No nCTF

Figure 6-1 illustrates the pad layout.

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Figure 6-1. PCB pad layout

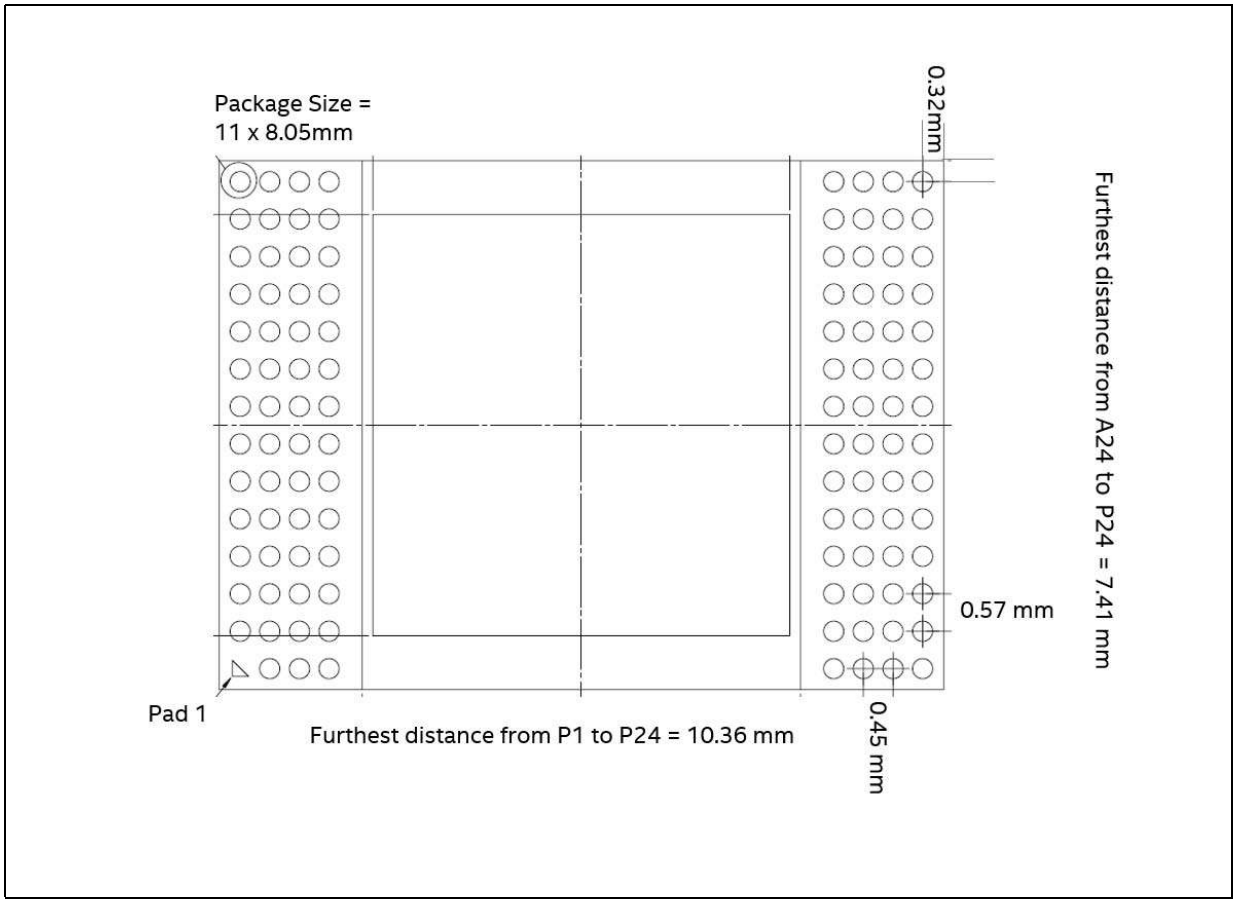
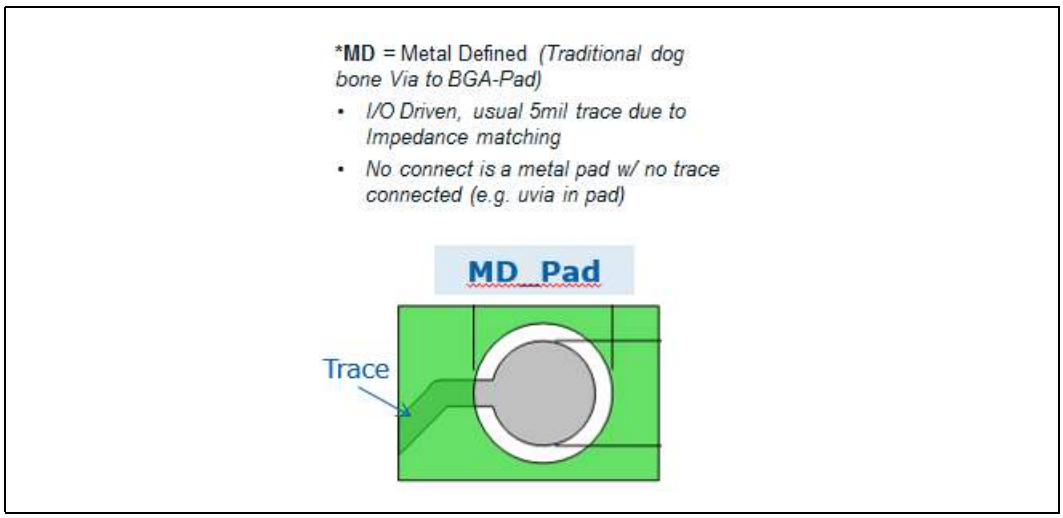
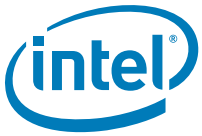


Figure 6-2 provides details about the metal defined pad.

Figure 6-2. Metal-defined pad





6.3 Manufacturing guidelines

The following two subsections provide some general guidelines on the reflow and rework for systems associated with Intel® Curie™ module.

6.3.1 SMT reflow parameters

Table 6-1 lists the SMT reflow parameters.

Disclaimer: These results are provided for informational purposes only. Any sourcing decision is solely at the discretion of the Customer. Intel neither warrants, nor makes any representation whatsoever as to any supplier's products, including its availability, suitability, and reliability for the application for which this information is provided. Other pastes not listed above may perform better or worse based on customer SMT / board characteristics. The solder paste formulation above have passed Intel's SMT stress test and are recommended for customer evaluation with the Intel® Curie™ module, to achieve acceptable SMT Yields.

Table 6-1. SMT reflow parameters

Parameter	Description/ Values
Intel evaluated solder paste	SAC305 Type 4
Solder joint peak temperature	240°C ±5°C, should remain below 245°C
Maximum body and substrate temperature	Never exceed 245°C
Time above =<217°C (TAL)	60-90 sec
Soak	Paste dependent. Consult paste manufacturer.
Rising ramp rate	< 3°C per second
Falling ramp rate	Maximum 3°C per second. Minimum 1°C per second from peak to 205°C
Reflow ambient[1]	N2 ambient (air is acceptable)
Reflow profile	Intel® Curie™ module is validated for 3 reflows
Pallet Support for Board Warpage	Recommended
SMT stencil information	Stencil thickness 3 mil aperture 10 mil round
MSL level	MSL Level 6. Must be reflowed within the time limit specified on the label. Units should not be left on the floor as parts can absorb moisture and fail. If parts are not being used they should be put back into MBB and the bags should be vacuum packed or sealed with desiccant and HIC card. Floor exposure should be tracked.
Other critical information	Please SMT the parts within 8 hours of opening the bag (typical 1 shift). If the cumulative time out of the bag (as measured from the 1st open bag time) exceeds 8 hours but is below 48 hours, the parts should be baked at 125°C for 24 hours. Please note that only 1 bake is allowed. Please SMT the parts within 8 hours of bake. Partial lots after bake can be put back in MBB with desiccant to stop (but not reset) MET clock but cumulative moisture exposure should not exceed 8 hours after bake. If moisture exposure is beyond 48 hours then the units are irrecoverable.

Notes:

1. Intel internal SMT development result indicated N2 is highly recommended to achieve the optimized SMT result. Intel internal SMT development used O2<1000 ppm concentration.

6.3.2 Board rework

The primary factors for board rework are the following:

- Flux formulation, solder paste formulation and volume
- A capable thermal reflow profile
- Proper PCB pad solder preparation/wicking (clean-up of the residual solder from the PCB pads)

The application design/board size, material and thickness will change the SMT profile. This section provides some guideline for building a board size.

Caution: Always remove the batteries before reworking the board.

Table 6-2 lists the rework recommendations for customer considerations.

Notes: Intel internal SMT development result indicated N2 is highly recommended to achieve the optimized SMT result. Intel internal SMT development used O2<1000 ppm concentration.

Disclaimer: These results are provided for informational purposes only. Any sourcing decision is solely at the discretion of the Customer. Intel neither warrants, nor makes any representation whatsoever as to any supplier's products, including its availability, suitability, and reliability for the application for which this information is provided. Other pastes not listed above may perform better or worse based on customer SMT / board characteristics. The solder paste formulation above have passed Intel's SMT stress test and are recommended for customer evaluation with the Intel® Curie™ module, to achieve acceptable SMT Yields.

Please share SMT yield summary (yield Pareto if possible) with Intel representative for revenue builds so we can track performance against our goals. In case of SMT failures, please secure the boards for timely failure analysis by Intel team to understand the defect mode.

Table 6-2. Rework reflow parameter recommendations

Parameter	FBGA and Chipset
Solder paste formulation	SAC305 type A, same stencil used in SMT
Flux formulation	TBD
Solder paste volume	Over-print
Rework pallets	Case dependent. Follow customer practice.
Gap between nozzle and PCB surface (optimize air flow)	762 um (30mils)
Placement force	0 grams (paste application) 140 grams (flux application)
Rework ambient	Air (Nitrogen was not evaluated)
Solder joint peak reflow temperature	230 to 245°C
Time above ≥ 217°C	60 to 90 seconds
Maximum body temperature	Never exceed component temperature ≥ 245°C
Component delta T (ΔT)	≤ 10°C
Soak temperature and time	Paste dependent - Consult the paste manufacturer.
Rising ramp rate below 150°C (+)	0.5 to 2.5°C/sec
Rising ramp rate between 205°C and 215°C (+)	0.35 to 0.75°C/sec
Falling ramp rate (-)	0.50 to 2.0°C/sec

6.4 General handling recommendations

The general handling recommendations are illustrated in Figure 6-3.

Figure 6-3. General handling recommendations