Introduction

The HI2303 evaluation kit can be used to examine the performance of the HI2303 triple 8-bit analog to digital converter (ADC). The evaluation board includes a buffered clock driver, voltage reference, triple A/D converter, data latches and triple D/A converter (DAC). Please refer to the functional block diagram in Figure 1.

Evaluation Board

The HI2303 evaluation board is a four layer board with a layout optimized for the best performance of the ADC. The optimization includes segmenting the analog and digital signals to prevent digital noise from degrading the analog-to-digital conversion process. The physical board is divided into an analog and digital area with supporting analog and digital ground planes. The power supplies hook-up is detailed in Table 1.

Included in the application note is an electrical schematic of the evaluation board circuitry, a components layout, a components part list and views of the various board layers that make up the printed wiring board. Please refer to Figures 2 through 8. The user should feel free to copy the layout in their application. Refer to the components layout and the evaluation board electrical schematics for the following discussions.

Table 1 lists the operational supply voltages for the evaluation board. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	NOMINAL VALUE	CURRENT (TYP)	FUNCTION(S) SUPPLIED
AVDD	5.0V ±5%	170	Analog power to ADC, Reference and DAC.
AGND			Analog Ground
DVDD	5.0V ±5%	80	Digital power to ADC, Clock, Latches and DAC.
DGND			Digital Ground

Analog Input

The analog inputs to the HI2303 are obtained via BNC connectors J1, J2 and J3 for A_{IN}, B_{IN} and C_{IN} respectively. The input is terminated by a 75Ω resistor and DC blocked by capacitors. To bias the inputs at the desired 0.5 to 2.5V range bias tees are provided and can be set via potentiometers R24, R25 and R26. In addition, jumpers JP21, JP22 and JP23 may removed to disconnect the bias tee. Care should be taken to ensure the inputs do not exceed the absolute maximum ratings of the ADC.

Reference Voltage Circuit

The analog input range of the HI2303 is set by the voltage between V_{RT} and V_{RB}. The voltage can either be internally generated or for increased accuracy externally provided. Please refer to table 2 for the appropriate jumpers on the evaluation board to ENSURE the internal and external reference are not enabled at the same time to prevent permanent damage to the HI2303.

Internal reference

The internal reference is enabled by connecting V_{RBS} to ANGD and V_{RTS} to AV_{DD}. The HI2303 will then generate approximately 2.5V and 0.6V for V_{RT} and V_{RB} respectively. An external voltage reference is also provided on the board.

External Reference

The external reference section contains two circuits which generate the top (V_{RT}) and bottom (V_{RB}) voltages. The precision reference is derived by using the Intersil ICL7663S programmable voltage regulator. For complete design theory please refer to the ICL7663 datasheet. As detailed in the datasheet, the output of the voltage regulator is defined in Equation 1. In addition, the sense pin is used along with the 10Ω resistors to provide short circuit protection of approximately 44mA.

$$V_{REF} = V_{SET} (R + R2/R1) \quad \text{(EQ. 1)}$$

V_{RT}

The top reference is derived by U3 and the supporting components which enables V_{RT} to be adjusted, via the variable resistor R17, from 1.25V to approximately 2.7V. The nominal voltage of V_{RT} should be set to 2.5V.

V_{RB}

The bottom reference is derived by U4 and the supporting components which allows V_{RB} to be adjusted, via the variable resistor R21, from 0V to approximately 2.5V. The nominal voltage of V_{RB} should be set to 0.5V.

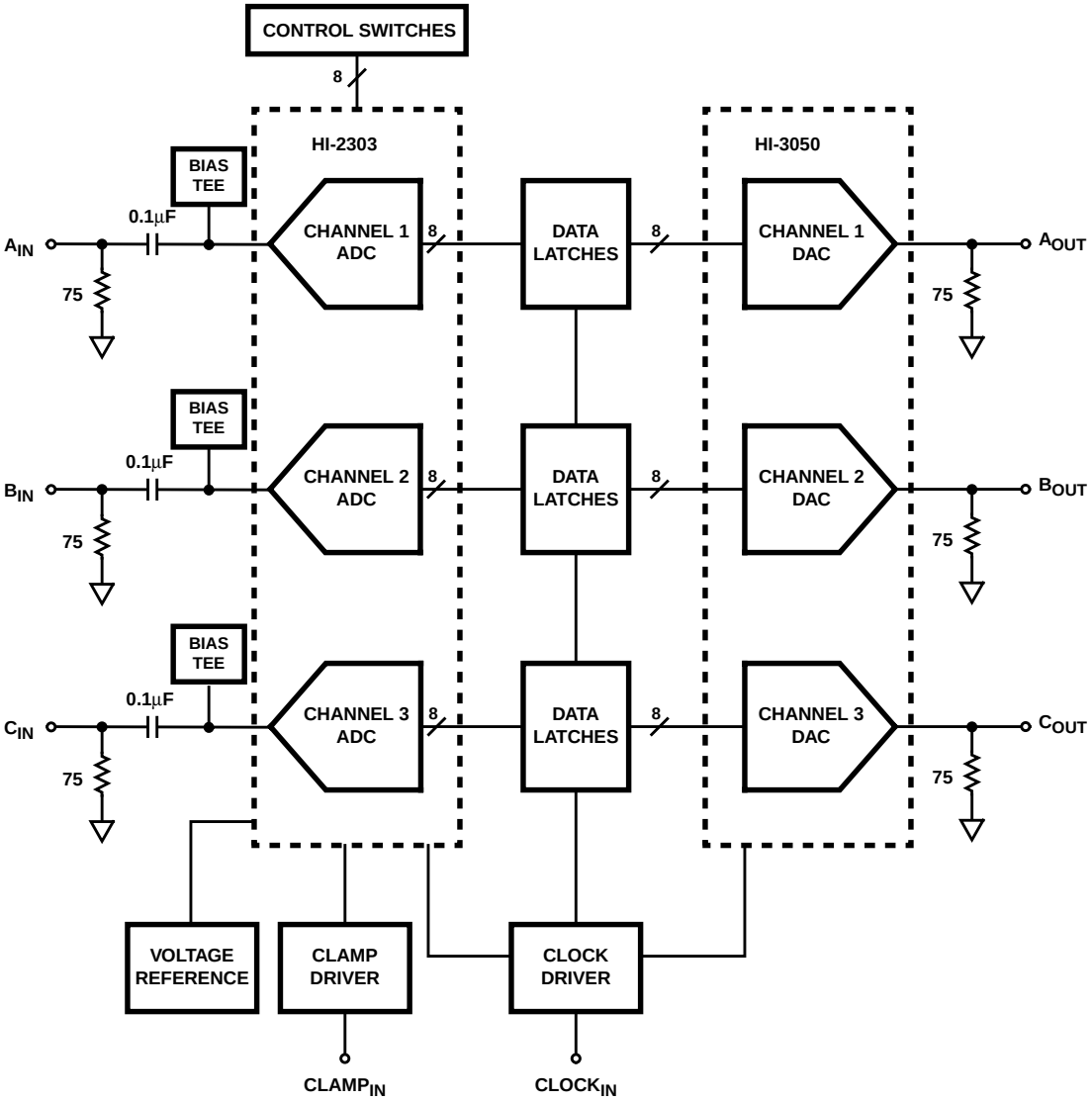


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Buffered Clock Driver

In order to ensure rated performance of the HI2303, the duty cycle of the sample clock should be set to 50%. It must also have low phase noise and operate at standard TTL logic levels.

It can be difficult to find a low phase noise generator that will provide a 50MHz squarewave at TTL logic levels. Consequently, the evaluation board is designed with a logic buffer (U2) acting as a voltage comparator to generate the sampling clock for the HI2303 when a sinewave (<±1.5V) is applied to the CLK input of the evaluation board. The sample clock sinewave is AC coupled into the input of the inverter and a discrete bias tee is used to bias the sinewave around the trigger level of the inverter's input. The variable resistor varies the DC bias voltage added to the sinewave input allowing the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC and to evaluate the effects of sample clock duty cycle on the performance of the converter. The sinewave to logic level comparator drives a series of additional buffers that provides isolation between the three sample clocks used on the evaluation board. One clock drives the ADC clock input pin (AD_CLOCK), a second clock drives output data latches (LATCH_CLOCK), and the last clock provides the DAC reconstruct clock(DA_CLOCK).

Reconstruction DAC

To easily verify the performance of the ADC a reconstruction DAC is provided. The 10-bit HI3050 triple DAC was selected to ensure the user measures the real ADC performance without any degradation from the reconstruct DAC. The DAC is configured to convert the latched data into a 2V fullscale output. The fullscale output can be adjusted slightly via R9. The DAC is optimized for the fullscale output voltage of 1.8 to 2.0V so care should be exercised when operating outside of the designed range.

TABLE 2. JUMPER SETTINGS

JUMPER	NAME	PURPOSE
JP1	ART IN	Connects top external board references V_{RT} to the reference top of Channel A (V_{ART}). For proper operation the top internal reference should not be selected via JP7.
JP2	ARB IN	Connects bottom external board references V_{RB} to the reference bottom of Channel A (V_{ARB}). For proper operation the bottom internal reference should not be selected via JP8.
JP3	BRT IN	Connects top external board references V_{RT} to the reference top of Channel B (V_{BRT}). For proper operation the top internal reference should not be selected via JP10.
JP4	BRB IN	Connects bottom external board references V_{RB} to the reference bottom of Channel B (V_{BRB}). For proper operation the bottom internal reference should not be selected via JP11.
JP5	CRT IN	Connects top external board references V_{RT} to the reference top of Channel C (V_{CRT}). For proper operation the top internal reference should not be selected via JP13.
JP6	CRB IN	Connects bottom external board references V_{RB} to the reference bottom of Channel C (V_{CRB}). For proper operation the bottom internal reference should not be selected via JP14.
JP7	ARTS	Enables top internal reference of channel A. JP1 should be removed.
JP8	ARBS	Enables bottom internal reference of channel A. JP2 should be removed.
JP9	AIO	Connects digital clamp output to channel input. Remove if internal clamp function is not used.
JP10	BRTS	Enables top internal reference of channel B. JP3 should be removed.
JP11	BRBS	Enables bottom internal reference of channel B. JP4 should be removed.
JP12	BIO	Connects digital clamp output to channel input. Remove if internal clamp function is not used.
JP13	CRTS	Enables top internal reference of channel C. JP5 should be removed.
JP14	CRBS	Enables bottom internal reference of channel C. JP6 should be removed.
JP15	CIO	Connects digital clamp output to channel input. Remove if internal clamp function is not used.
JP16	LATCH_EN3	Enables channel A latch (U5).
JP17	L1_ENABLE	Enables clock buffers. (U2).
JP18	L2_DISABLE	Disables clamp buffer. (U2).
JP19	LATCH_EN1	Enables channel B latch (U7).
JP20	LATCH_EN2	Enables channel C latch (U6).
JP21	Cin	Connects bias-T to C Channel input.
JP22	Ain	Connects bias-T to A Channel input.
JP23	Bin	Connects bias-T to B Channel input.
JP24	XAOE	Enable A Channel digital output.
JP25	XBOE	Enable B Channel digital output.
JP26	XCOE	Enable C Channel digital output.

Measured Performance

The performance of the evaluation board was measured by capturing the ADC data and performing the Fast Fourier Transform (FFT) to derive Signal-to-Noise and Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD) and Effective Number of Bits (ENOB). This data is summarized in Table 3 and graphically displayed in Figures 1 and 2.

Note: Coherent testing is recommended in order to avoid the inaccuracies of windowing.

TABLE 3. DYNAMIC PERFORMANCE

f_{IN} (MHz)	ENOB	SINAD dB	SNR dB	THD dB
0.1	7.63	47.71	48.41	-54.91
1	7.51	49.96	48.14	-53.19
5	7.32	45.81	46.51	-54.1
10	7.01	43.97	46.90	-47.06
15	6.54	41.13	46.9	-42.46
20	6.18	38.96	47	-39.65

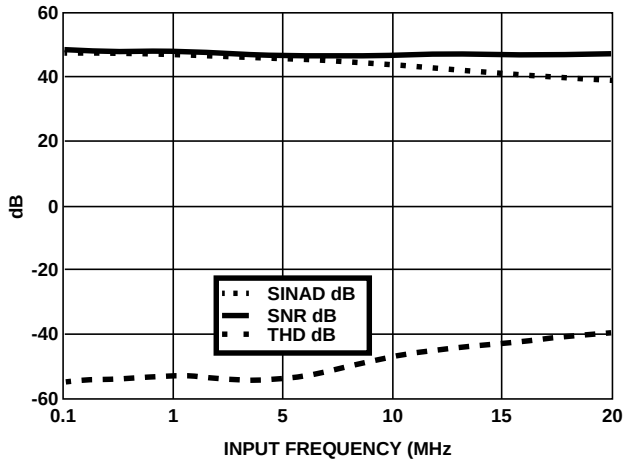


FIGURE 2. SINAD, SNR AND THD vs f_{IN}

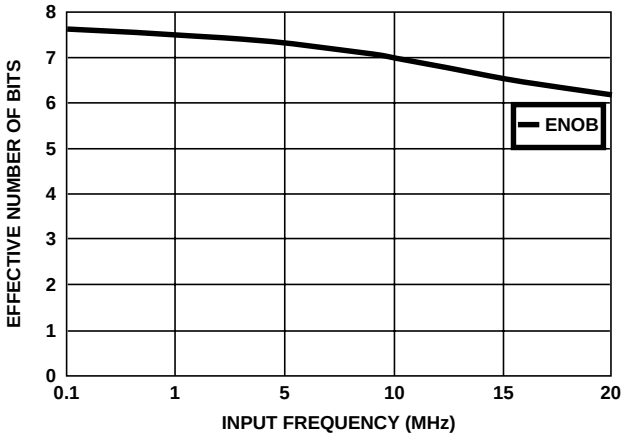


FIGURE 3. ENOB vs f_{IN} (f_{CLOCK} = 50MHz

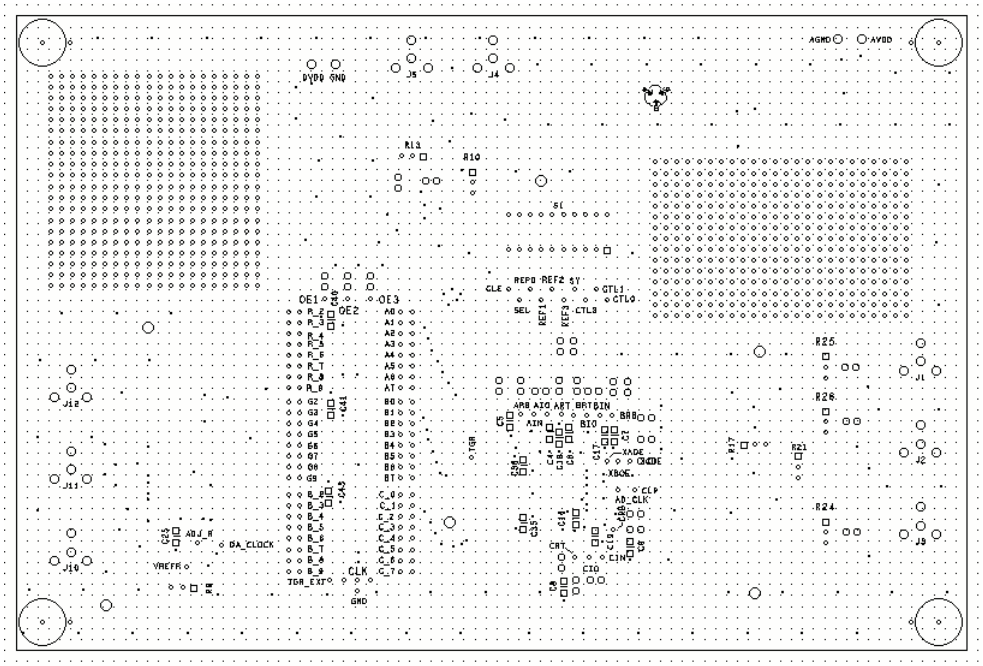


FIGURE 4. TOP SILK SCREEN

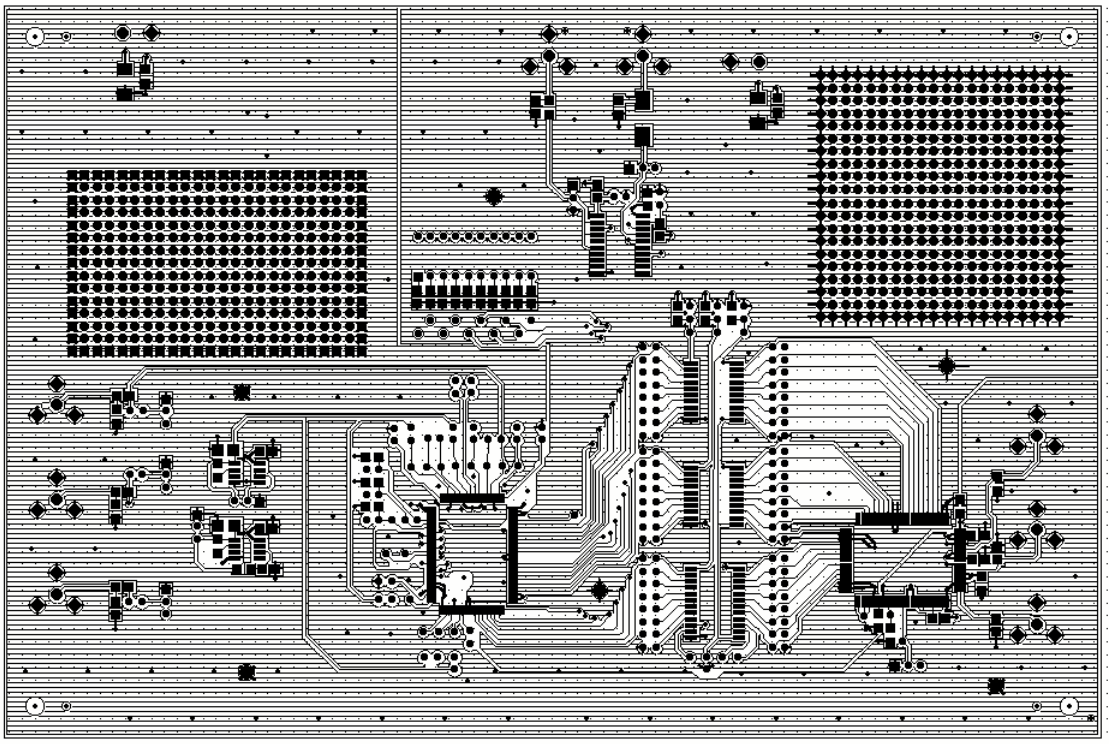


FIGURE 5. TOP SIGNAL LAYER

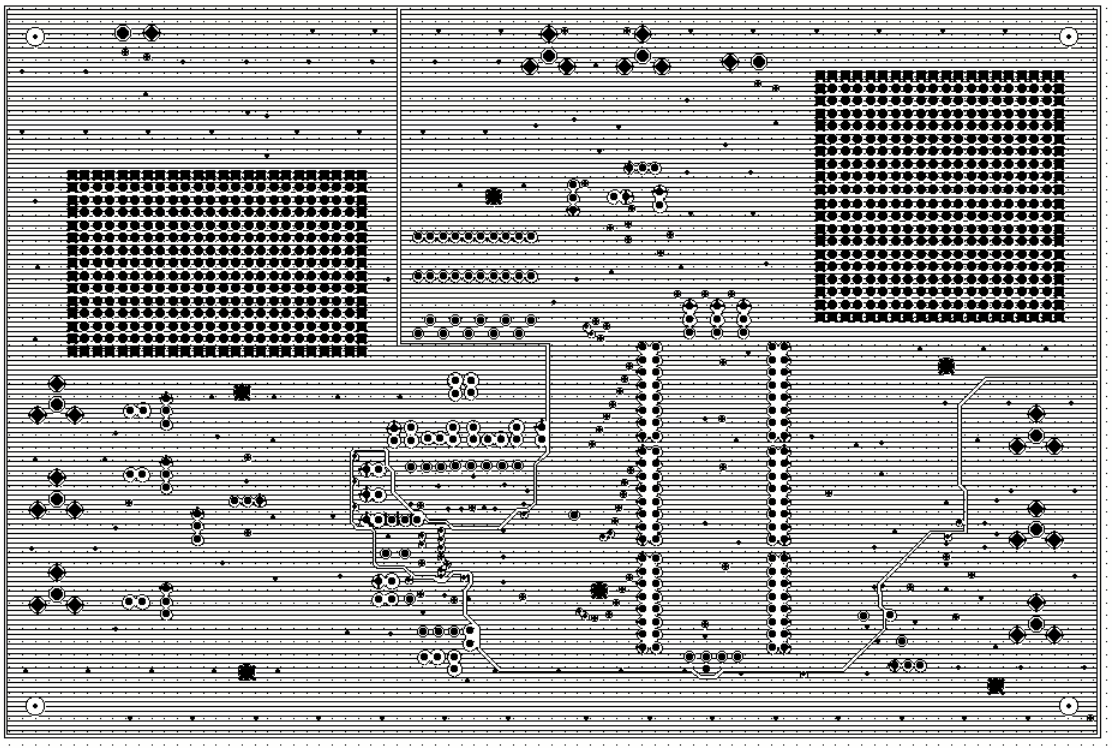


FIGURE 6. ANALOG AND DIGITAL GROUND PLANE

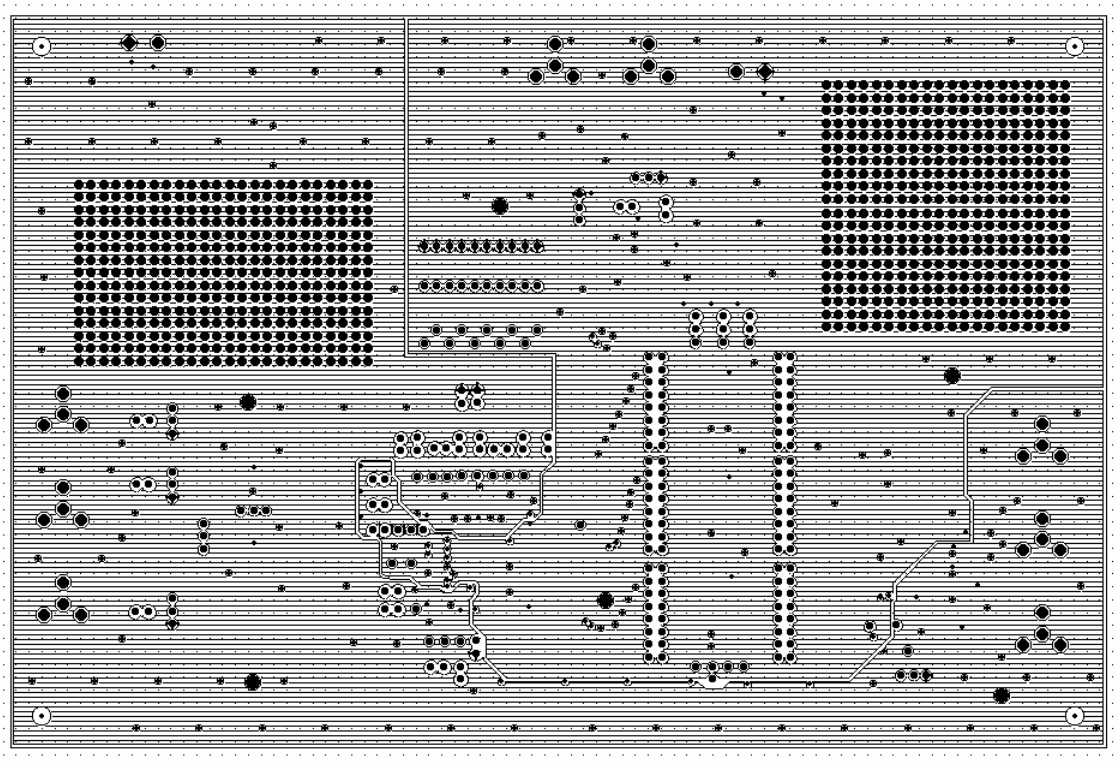


FIGURE 7. ANALOG AND DIGITAL POWER PLANE

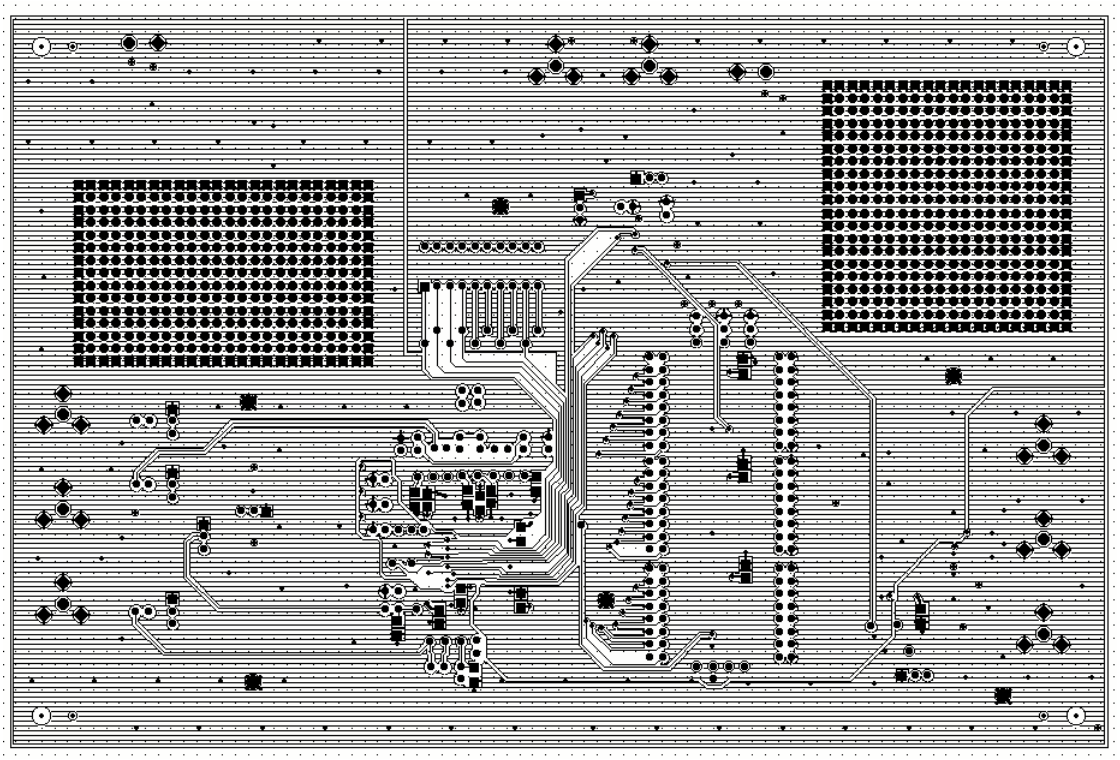


FIGURE 8. BOTTOM SIGNAL LAYER

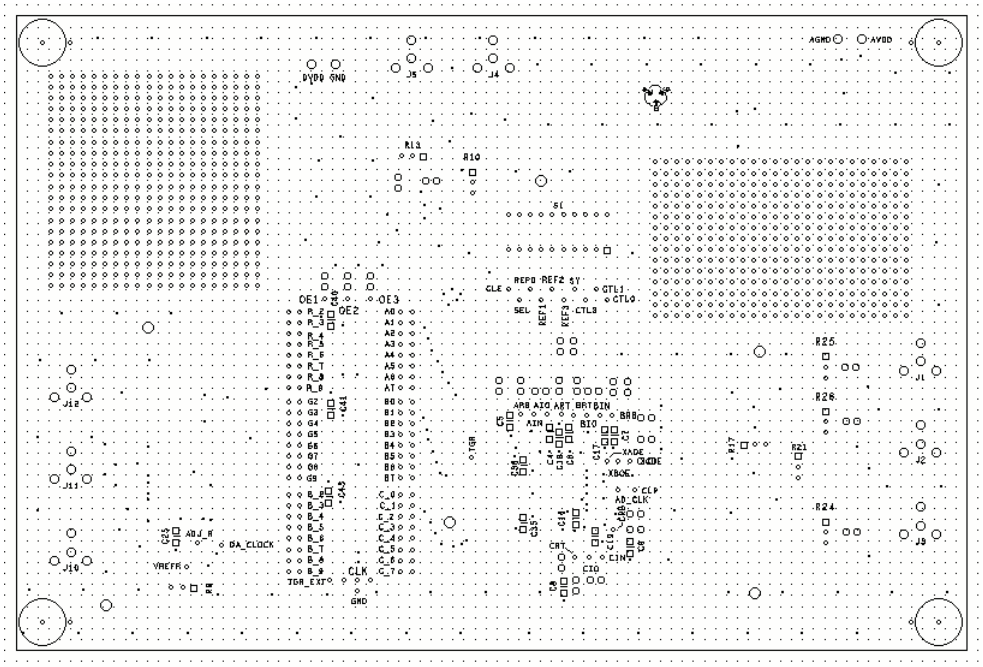


FIGURE 9. BOTTOM SILKSCREEN

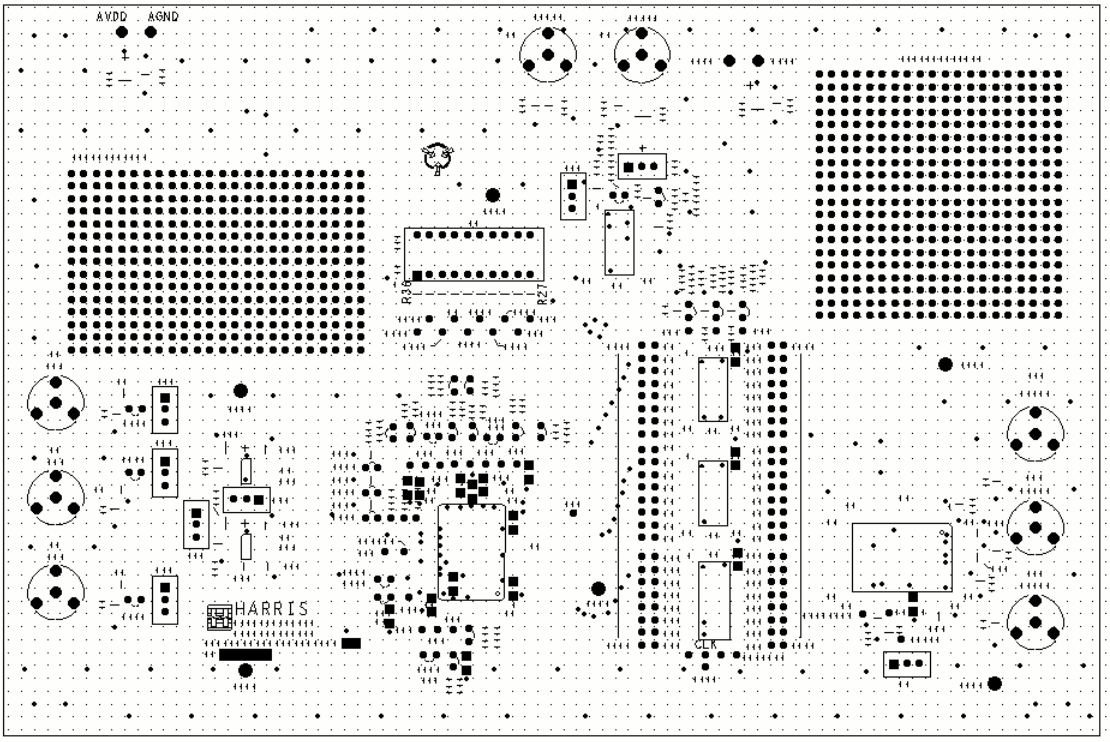
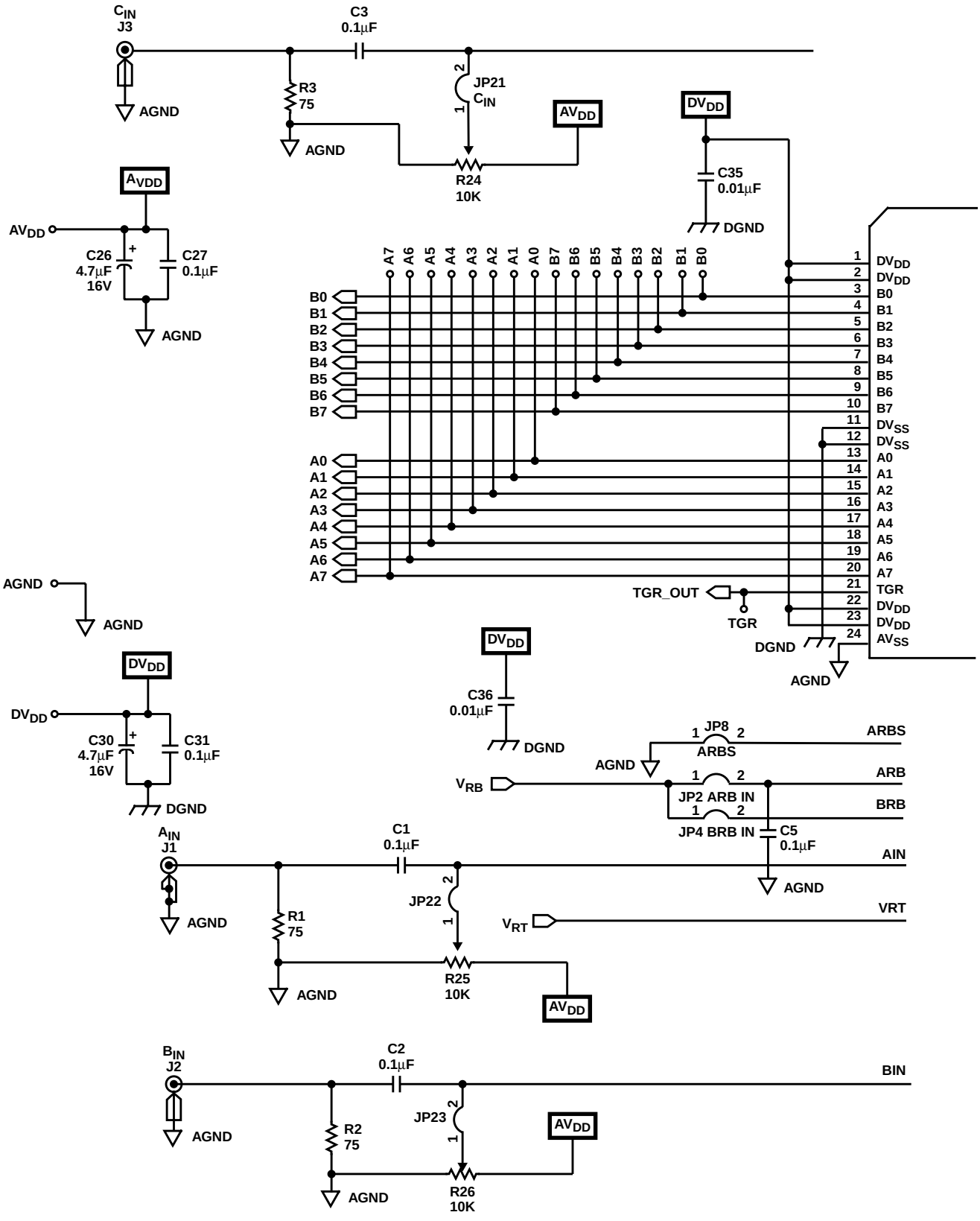
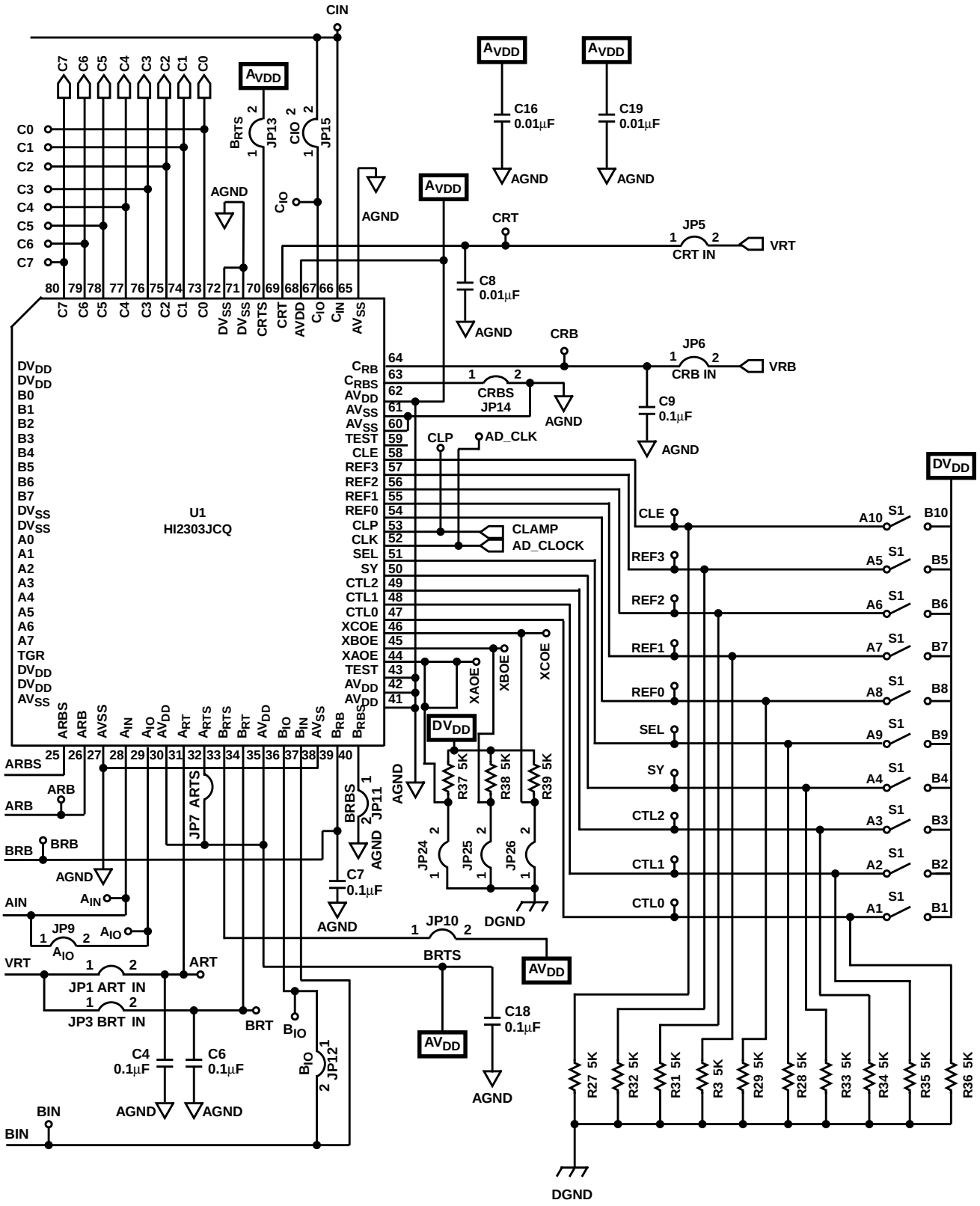
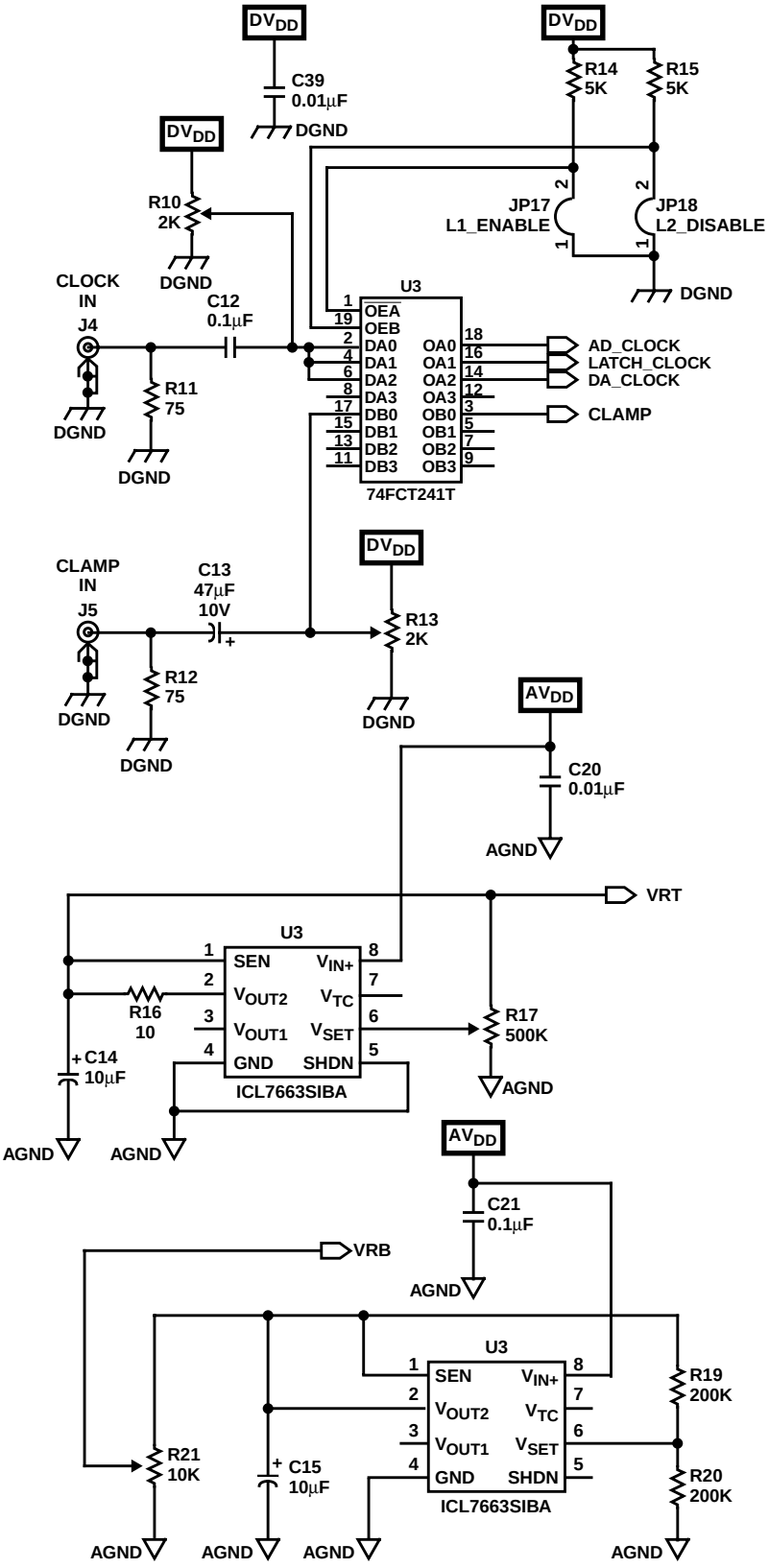
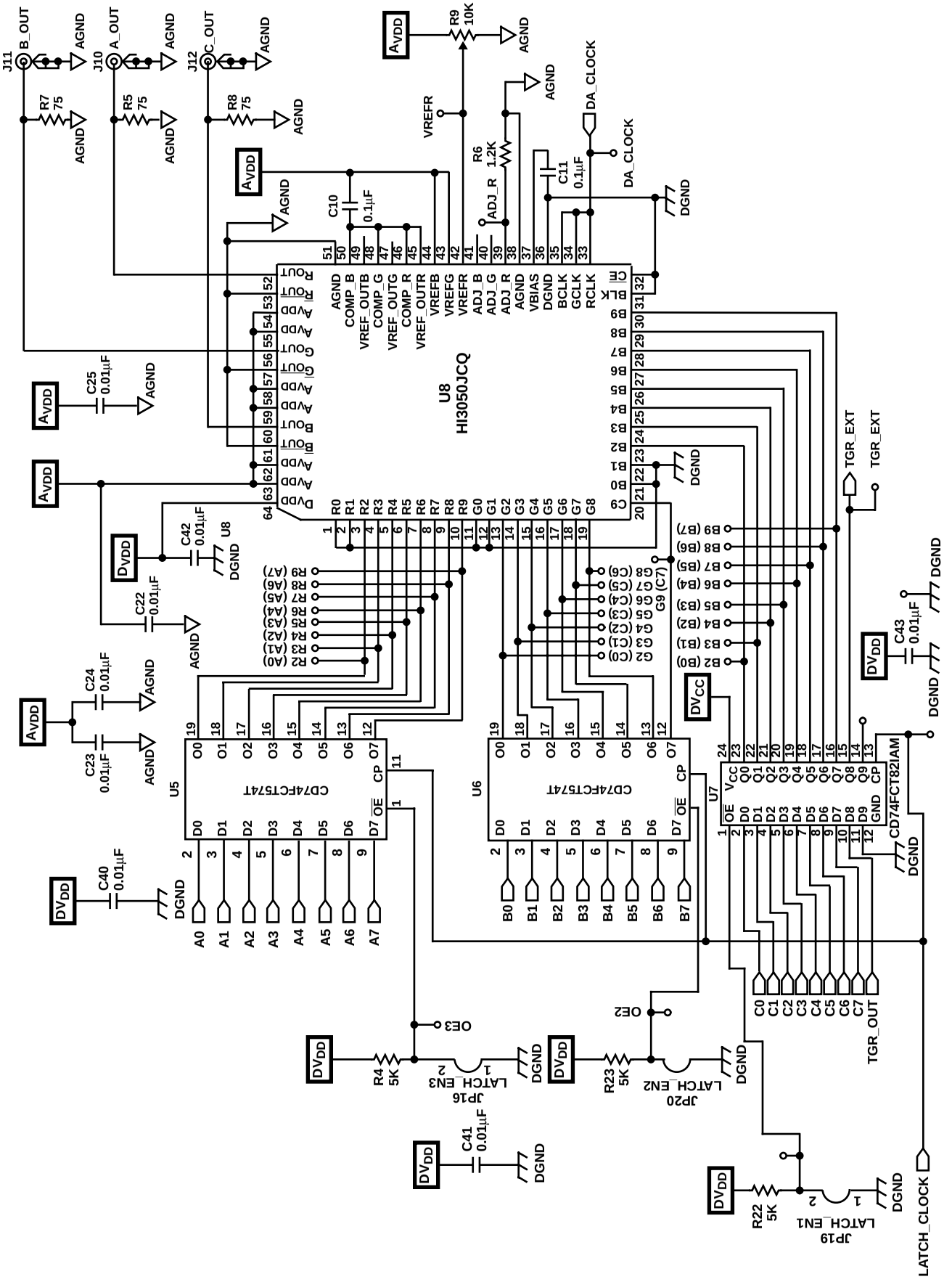


FIGURE 10.


CIN
J3
C3
0.1µF
AGND
R3
75
JP21
CIN
AVDD
DVDD
R24
10K
C35
0.01µF
DGND
AVDD
AVDD
C26
4.7µF
16V
C27
0.1µF
AGND
A7 A6 A5 A4 A3 A2 A1 A0 B7 B6 B5 B4 B3 B2 B1 B0
B0 B1 B2 B3 B4 B5 B6 B7
A0 A1 A2 A3 A4 A5 A6 A7
1 DVDD
2 DVDD
3 B0
4 B1
5 B2
6 B3
7 B4
8 B5
9 B6
10 B7
11 DVSS
12 DVSS
13 A0
14 A1
15 A2
16 A3
17 A4
18 A5
19 A6
20 A7
21 TGR
22 DVDD
23 DVDD
24 AVSS
TGR_OUT
TGR
DGND
AGND
AGND
AGND
DVDD
DVDD
C30
4.7µF
16V
C31
0.1µF
DGND
DVDD
C36
0.01µF
DGND
JP8
ARBS
ARBS
AGND
VRB
ARB
JP2 ARB IN
BRB
JP4 BRB IN
C5
0.1µF
AIN
AGND
VRT
AIN
J1
C1
0.1µF
AGND
R1
75
JP22
VRT
R25
10K
AGND
AVDD
BIN
J2
C2
0.1µF
BIN
AGND
R2
75
JP23
AVDD
R26
10K
AGND


CIN
C7 C6 C5 C4 C3 C2 C1 C0
C0 C1 C2 C3 C4 C5 C6 C7
AVDD
BRTS JP13 CIO JP15
AGND
CIO
C16 0.01µF
C19 0.01µF
CRT
JP5 CRT IN VRT
C8 0.01µF
CRB
JP6 CRB IN VRB
CRBS JP14
C9 0.1µF
CLP AD_CLK
U1
HI2303JCQ
CLAMP AD_CLOCK
DVDD
CLE REF3 REF2 REF1 REF0 SEL SY CTL2 CTL1 CTL0
A10 A5 A6 A7 A8 A9 A4 A3 A2 A1
B10 B5 B6 B7 B8 B9 B4 B3 B2 B1
S1
XAOE XBOE XCOE
R37 5K R38 5K R39 5K
JP24 JP25 JP26
DGND
ARBS ARB AVSS AIN AIO AVDD ART ARTS BRTS BRT AVDD BIO BIN AVSS BRB BRBS
JP7 ARTS
BRBS JP11
C7 0.1µF
JP10
BRTS
JP9
JP1 ART IN
JP3 BRT IN
C4 0.1µF
C6 0.1µF
JP12
C18 0.1µF
R27 5K R32 5K R31 5K R3 5K R29 5K R28 5K R33 5K R34 5K R35 5K R36 5K


DVDD
C39
0.01µF
DGND
R14
5K
R15
5K
R10
2K
JP17
L1_ENABLE
JP18
L2_DISABLE
CLOCK
IN
J4
C12
0.1µF
U3
OEA
OEB
DA0
DA1
DA2
DA3
DB0
DB1
DB2
DB3
OA0
OA1
OA2
OA3
OB0
OB1
OB2
OB3
AD_CLOCK
LATCH_CLOCK
DA_CLOCK
CLAMP
74FCT241T
R11
75
CLAMP
IN
J5
C13
47µF
10V
R13
2K
R12
75
AVDD
C20
0.01µF
AGND
VRT
SEN
VOUT2
VOUT1
GND
VIN+
VTC
VSET
SHDN
ICL7663SIBA
R16
10
R17
500K
C14
10µF
VRB
C21
0.1µF
R19
200K
R20
200K
R21
10K
C15
10µF


U8
HI3050JCQ
U5
U6
U7
CD74FCT574T
CD74FCT821AM
J11 B_OUT
J10 A_OUT
J12 C_OUT
AGND
DGND
AVDD
DVDD
DVCC
R7 75
R5 75
R8 75
R9 10K
R6 1.2K
C10 0.1µF
C11 0.1µF
C25 0.01µF
C42 0.01µF
C22 0.01µF
C24 0.01µF
C23 0.01µF
C40 0.01µF
C43 0.01µF
C41 0.01µF
R4 5K
R23 5K
R22 5K
JP16 LATCH_EN3
JP20 LATCH_EN2
JP19 LATCH_EN1
VREFR
ADJ_R
DA_CLOCK
TGR_EXT
OE3
OE2
LATCH_CLOCK
TGR_OUT

HI2303EVAL1 TRIPLE 8-BIT 50MHz A/D

X__ Authorized to use a tighter tolerance part if the requested tolerance is not available. (Ex: Requested 10%, ok to use 5% or lower)

_X__ Authorized to use a higher voltage part if the requested voltage is not available but not to exceed ____ volts. (Ex: Requested 16 volts but not to exceed 50 volts)

NOTES:

1. The above action items will only be in effect if it will impact Intersil delivery schedule or if a part is not available due to a long lead time.
2. The purchased part will meet all form, fit and function requirements.
3. Substitute Component Authorization (SCA) will be submitted for any manufacturer/manufacturer part numbers

LINE ITEM #	QTY. PER PCB	REFERENCE DESIGNATOR	DESCRIPTION	PART#/ VALUE	DIEL	TOL	PKG SIZE RADIAL AXIAL LEAD SPACE	VOLT	WATTS	MFGR	MFGR'S PART #	COMMENTS
1	8	R1, R2, R3, R5, R7, R8, R11, R12	Res, Chip	75Ω		1%	1206		1/8W	Any		
2	18	R4, R14, R15, R22, R23, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39	Res, Chip	4.99kΩ		1%	1206		1/8W	Any		
3	2	R16, R18	Res, Chip	10Ω		1%	1206		1/8W	Any		
4	1	R6	Res, Chip	1.2kΩ		1%	1206		1/8W	Any		
5	2	R19, R20	Res, Chip	200kΩ		1%	1206		1/8W	Any		
6	5	R9, R21, R24, R25, R26	Trimmer Potentiometer	10kΩ		10%	3296W			Bourns		
7	2	R10, R13	Trimmer Potentiometer	2kΩ		10%	3296W			Bourns		
8	1	R17	Trimmer Potentiometer	500kΩ		10%	3296W			Bourns		
9	1	U1	Triple 8-Bit A/D	HI2303JCQ			MQFP			Intersil		
10	1	U2	Buffer	CD74FCT241DTM			SOIC			Intersil		
11	2	U3, U4	Programmable Voltage Regulator	ICL7663SIBA			SOIC			Intersil		
12	2	U5, U6	8-Bit Interface Registers	CD74FCT574DTM			SOIC			Intersil		
13	1	U7	10-Bit Interface Registers	CD74FCT821CTM			SOIC			Intersil		
14	1	U8	Triple 10-bit D/A	HI3050JCQ			MQFP			Intersil		
15												

X__ Authorized to use a tighter tolerance part if the requested tolerance is not available. (Ex: Requested 10%, ok to use 5% or lower)

_X__ Authorized to use a higher voltage part if the requested voltage is not available but not to exceed ____ volts. (Ex: Requested 16 volts but not to exceed 50 volts)

NOTES:

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2. The purchased part will meet all form, fit and function requirements.
3. Substitute Component Authorization (SCA) will be submitted for any manufacturer/manufacturer part numbers **(Continued)**

LINE ITEM #	QTY. PER PCB	REFERENCE DESIGNATOR	DESCRIPTION	PART#/ VALUE	DIEL	TOL	PKG SIZE RADIAL AXIAL LEAD SPACE	VOLT	WATTS	MFGR	MFGR'S PART #	COMMENTS
16	0	Was C1, C2, C3	Cap	1µF			EIA CASE A				PCS2475CT	Electrolytic
17	11	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C27, C31	Cap, Chip	0.1µF		10%	1206			Any, Panasonic	PCC104BCT	
18	1	C13	Cap	47µF			EIA CASE D				ECS_H1ED106R	
19	2	C14, C15	Cap, Chip	10µF			EIA CASE B		10VWDC	Any, Panasonic	PCS2106CT	
20	22	C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C35, C36, C39, C40, C41, C42, C43	Cap, Chip	0.01µF		10%	1206			Any, Panasonic	PCC103BCT	
21	2	C26, C30	Cap, Chip	4.7µF		20%	EIA CASE A		16WVDC			
22	8	J1, J2, J3, J4, J5, J10, J11, J12	BNC Connector							AMP		
23	26	JP1-JP26	HEADER, 1X2							Berg Electron-ics/Any	69190-402	
24	26	CON	JUMPER, 1X2							Berg Electronics/Any	55-50275P (Black) 617-6600	
25	4		Rubber Feet							3M Any Allied		
26	6		HEADER, 2X8							Any		
27	6		Terminal							Cambion	160-2044-02-01	