

RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

Check for Samples: [MAX3386E](#)

FEATURES

- V_L Pin for Compatibility With Mixed-Voltage Systems Down to 2.5 V on Logic Side
- Enhanced ESD Protection on RIN Inputs and DOUT Outputs
 - ±15-kV Human-Body Model
 - ±15-kV IEC 61000-4-2, Air-Gap Discharge
 - ±8-kV IEC 61000-4-2, Contact Discharge
- Low 300- μ A Supply Current
- Specified 250-kbps Data Rate
- 1- μ A Low-Power Shutdown
- Meets EIA/TIA-232 Specifications Down to 3 V

APPLICATIONS

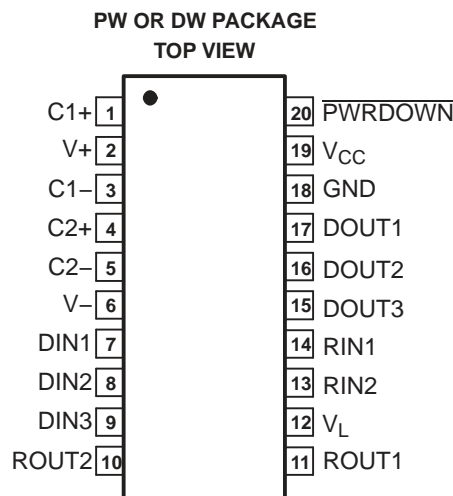
- Hand-Held Equipment
- PDAs
- Cell Phones
- Battery-Powered Equipment
- Data Cables

DESCRIPTION/ORDERING INFORMATION

The MAX3386E is a three-driver and two-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ±15 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human-Body Model.

The charge pump requires only four small 0.1- μ F capacitors for operation from a 3.3-V supply. The MAX3386E is capable of running at data rates up to 250 kbps, while maintaining RS-232-compliant output levels.

The MAX3386E has a unique V_L pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the V_L pin. The MAX3386E is available in a space-saving thin shrink small-outline package (TSSOP).



ORDERING INFORMATION

T _A	PACKAGE ^{(1) (2)}	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – PW	MAX3386ECPWR	MP386EC
	SOIC – DW	MAX3386ECDW	MAX3386EC
–40°C to 85°C	TSSOP – PW	MAX3386EIPWR	MP386EI
	SOIC – DW	MAX3386EIDW	MAX3386EI

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

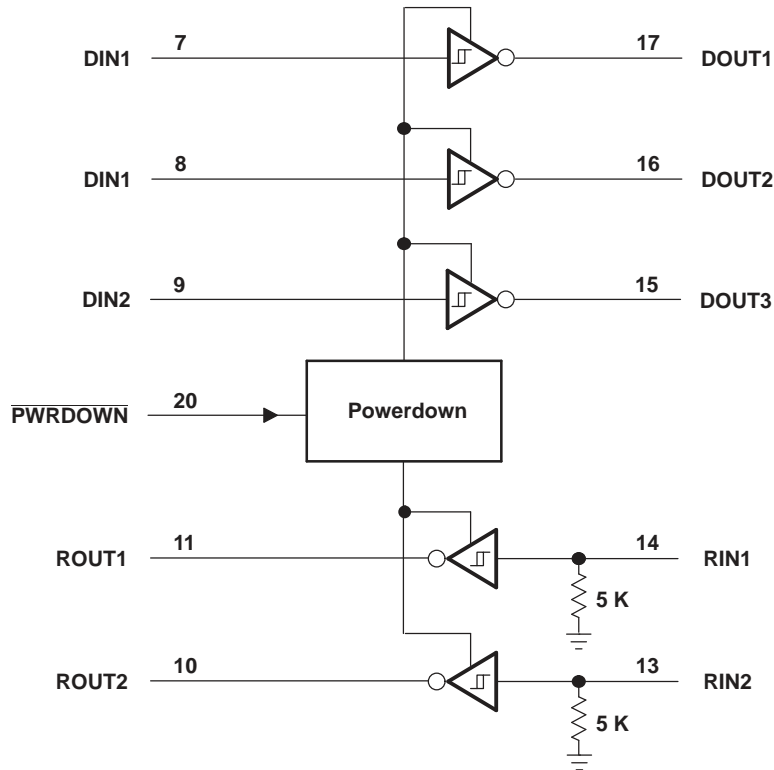


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. TRUTH TABLE (SHUTDOWN FUNCTION)

$\overline{\text{PWRDWN}}$	DRIVER OUTPUTS	RECEIVER OUTPUTS	CHARGE PUMP
L	High-Z	High-Z	Inactive
H	Active	Active	Active

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
C1+	1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	2	5.5-V supply generated by the charge pump
C1-	3	Negative terminal of the voltage-doubler charge-pump capacitor
C2+	4	Positive terminal of the inverting charge-pump capacitor
C2-	5	Negative terminal of the inverting charge-pump capacitor
V-	6	-5.5-V supply generated by the charge pump
DIN1 DIN2 DIN3	7 8 9	Driver inputs
ROUT2 ROUT1	10 11	Receiver outputs. Swing between 0 and V_L .
V_L	12	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN2 RIN1	13 14	RS-232 receiver inputs
DOUT3 DOUT2 DOUT1	15 16 17	RS-232 driver outputs
GND	18	Ground

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
V _{CC}	19	3-V to 5.5-V supply voltage
$\overline{\text{PWRDWN}}$	20	Powerdown input L = Powerdown H = Normal operation

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC} to GND		-0.3	6	V
V _L to GND		-0.3	V _{CC} + 0.3	V
V+ to GND		-0.3	7	V
V- to GND		0.3	-7	V
V+ + V- ⁽²⁾			13	V
V _I Input voltage	DIN, $\overline{\text{PWRDWN}}$ to GND	-0.3	6	V
	RIN to GND		±25	
V _O Output voltage	DOUT to GND		±13.2	V
	ROUT	-0.3	V _L + 0.3	
Short-circuit duration DOUT to GND			Continuous	
Continuous power dissipation		T _A = 70°C, 20-pin TSSOP (derate 7 mW/°C above 70°C)		559 mW
T _J Junction temperature			150	°C
T _{stg} Storage temperature range		-65	150	°C
	Lead temperature (soldering, 10 s)		300	

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- (2) V+ and V- can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC} Supply voltage		3	5.5	V
V _L Supply voltage		2.25	V _{CC}	V
Input logic threshold low	DIN, $\overline{\text{PWRDWN}}$	V _L = 3 V or 5.5 V	0.8	V
		V _L = 2.3 V	0.6	
Input logic threshold high	DIN, $\overline{\text{PWRDWN}}$	V _L = 5.5 V	2.4	V
		V _L = 3 V	2.0	
		V _L = 2.7 V	1.4	
Operating temperature	MAX3386ECPWR	0	70	°C
	MAX3386EIPWR	-40	85	
Receiver input voltage		-25	25	V

Electrical Characteristics

over operating free-air temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DC Characteristics (V_{CC} = 3.3 V or 5 V, T_A = 25°C)					
Powerdown supply current	$\overline{\text{PWRDWN}}$ = GND, All inputs at V _{CC} or GND		1	10	μA

- (1) Typical values are at V_{CC} = V_L = 3.3 V, T_A = 25°C.

Electrical Characteristics (continued)

over operating free-air temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1\text{--}C4 = 0.1\ \mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\ \mu\text{F}$, $C2\text{--}C4 = 0.33\ \mu\text{F}$ (tested at $5\text{ V} \pm 10\%$) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Supply current	$\overline{\text{PWRDWN}} = V_{CC}$, No load		0.3	1	mA

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	± 15	kV
	IEC 61000-4-2 Air-Gap Discharge	± 15	
	IEC 61000-4-2 Contact Discharge	± 8	

RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
I_{off}	Output leakage current	R_{OUT} , receivers disabled		± 0.05	± 10	μA	
V_{OL}	Output voltage low	$I_{OUT} = 1.6\text{ mA}$			0.4	V	
V_{OH}	Output voltage high	$I_{OUT} = -1\text{ mA}$	$V_L - 0.6$	$V_L - 0.1$		V	
V_{IT-}	Input threshold low	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$	0.8	1.2	V	
			$V_L = 3.3\text{ V}$	0.6	1.5		
V_{IT+}	Input threshold high	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$		1.8	2.4	V
			$V_L = 3.3\text{ V}$		1.5	2.4	
V_{hys}	Input hysteresis			0.5		V	
	Input resistance	$T_A = 25^\circ\text{C}$	3	5	7	$\text{k}\Omega$	

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

Switching Characteristics

over operating free-air temperature range, $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$, $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t_{PHL}	Receiver propagation delay	Receiver input to receiver output, $C_L = 150\text{ pF}$	0.15	μs
t_{PLH}			0.15	
$t_{PHL} - t_{PLH}$	Receiver skew		50	ns
t_{en}	Receiver output enable time	From $\overline{\text{PWRDWN}}$	200	ns
t_{dis}	Receiver output disable time	From $\overline{\text{PWRDWN}}$	200	ns

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

DRIVER SECTION

Electrical Characteristics

over operating free-air temperature range, $V_{CC} = V_L = 3\text{ V}$ to 5.5 V , $C1-C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2-C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH} Output voltage swing	All driver outputs loaded with $3\text{ k}\Omega$ to ground	± 5	± 5.4		V
r_o Output resistance	$V_{CC} = V_+ = V_- = 0$, Driver output = $\pm 2\text{ V}$	300	10M		Ω
I_{OS} Output short-circuit current	$V_{T_OUT} = 0$			± 60	mA
I_{OZ} Output leakage current	$V_{T_OUT} = \pm 12\text{ V}$, Driver disabled, $V_{CC} = 0$ or 3 V to 5.5 V			± 25	μA
Driver input hysteresis				0.5	V
Input leakage current	DIN, $\overline{\text{PWRDWN}}$		± 0.01	± 1	μA

(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

Timing Requirements

over operating free-air temperature range, $V_{CC} = V_L = 3\text{ V}$ to 5.5 V , $C1-C4 = 0.1\text{ }\mu\text{F}$ (tested at $3.3\text{ V} \pm 10\%$), $C1 = 0.047\text{ }\mu\text{F}$, $C2-C4 = 0.33\text{ }\mu\text{F}$ (tested at $5\text{ V} \pm 10\%$), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate	$R_L = 3\text{ k}\Omega$, $C_L = 1000\text{ pF}$, One driver switching	250			kbps
Time-to-exit powerdown	$ V_{T_OUT} > 3.7\text{ V}$		100		μs
$ t_{PHL} - t_{PLH} $ Driver skew ⁽²⁾			100		ns
Transition-region slew rate	$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, Measured from 3 V to -3 V or -3 V to 3 V	$C_L = 150\text{ pF}$ to 1000 pF	6	30	V/ μs
		$C_L = 150\text{ pF}$ to 2500 pF	4	30	

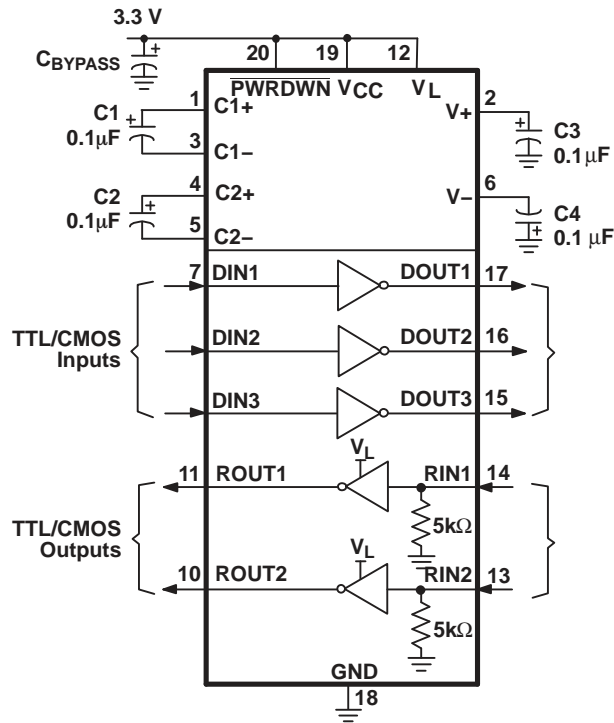
(1) Typical values are at $V_{CC} = V_L = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) Driver skew is measured at the driver zero crosspoint.

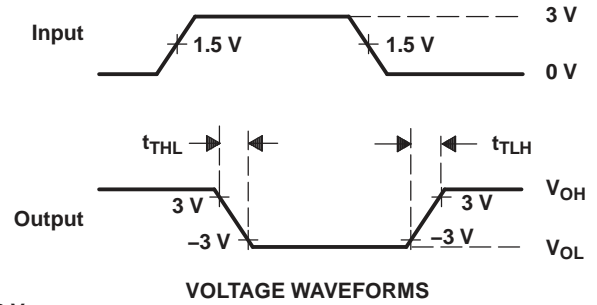
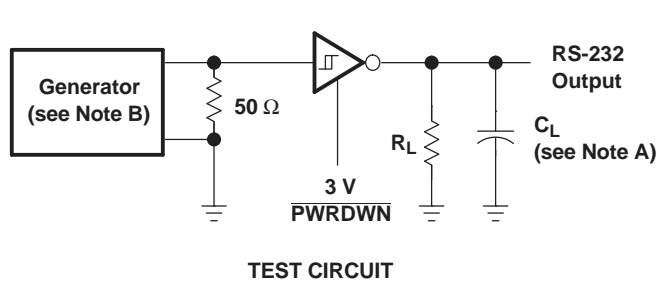
ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	± 15	kV
	IEC 61000-4-2 Air-Gap Discharge	± 15	
	IEC 61000-4-2 Contact Discharge	± 8	

APPLICATION INFORMATION



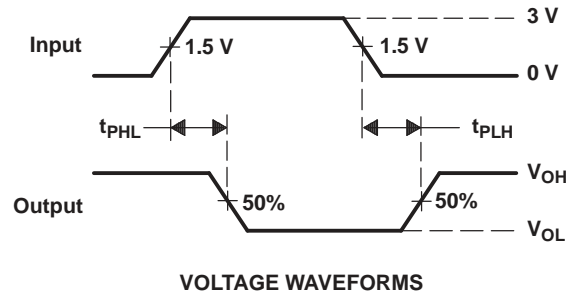
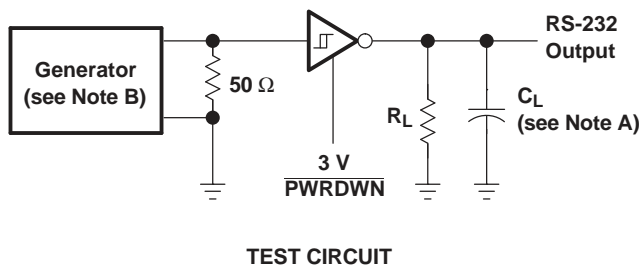
PARAMETER MEASUREMENT INFORMATION



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

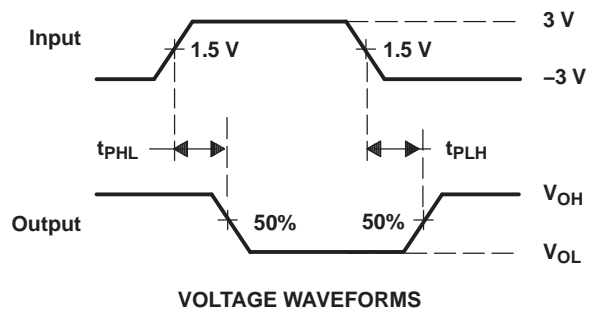
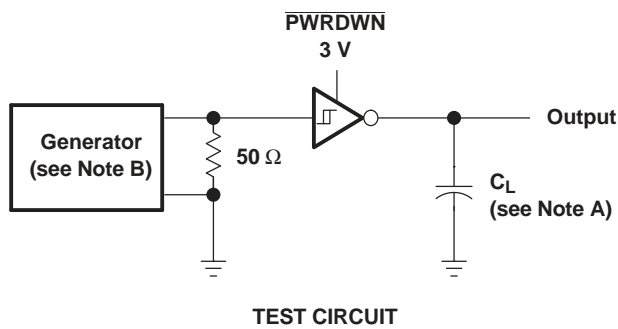
- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

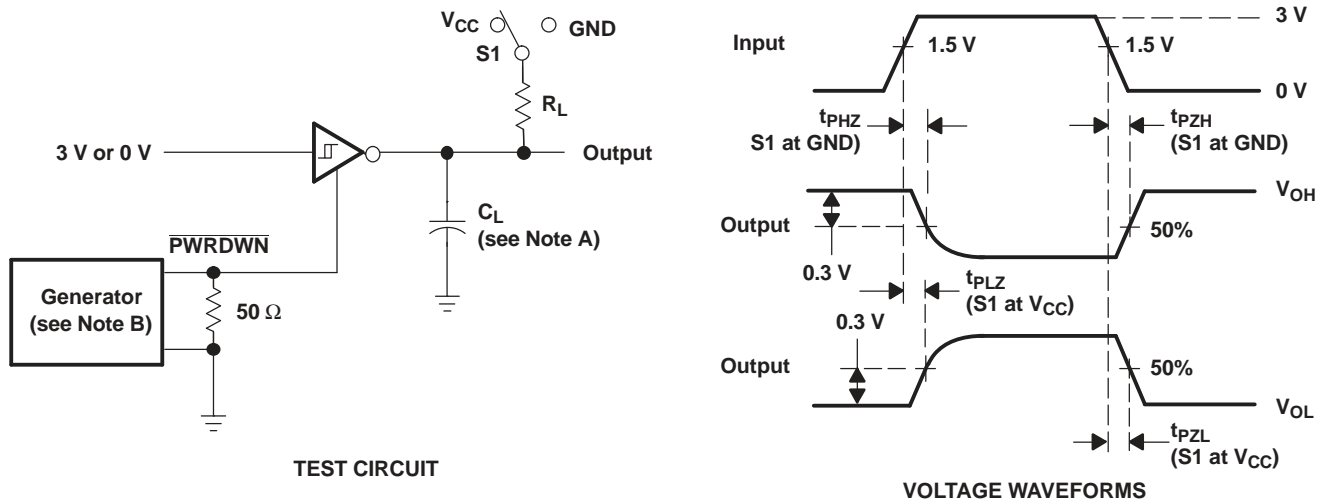
Figure 2. Driver Pulse Skew



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 4. Receiver Enable and Disable Times

REVISION HISTORY

Changes from Revision A (November 2008) to Revision B	Page
• Changed V_L Pin for Compatibility With Mixed-Voltage Systems Down to 2.5 V (originally 1.8 V) on the Logic Side	1
• Changed V_L Supply MIN value from 1.65 V to 2.25 V.	3
• Deleted $V_L = 1.65V$ parameter from Input logic threshold low.	3
• Deleted $V_L = 1.95V$ parameter from Input logic threshold high.	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3386ECDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3386EC	Samples
MAX3386ECPW	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP386EC	
MAX3386ECPWR	LIFEBUY				2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP386EC	
MAX3386EIDW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3386EI	
MAX3386EIDWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3386EI	
MAX3386EIPW	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP386EI	
MAX3386EIPWR	LIFEBUY				2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP386EI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3386ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3386EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



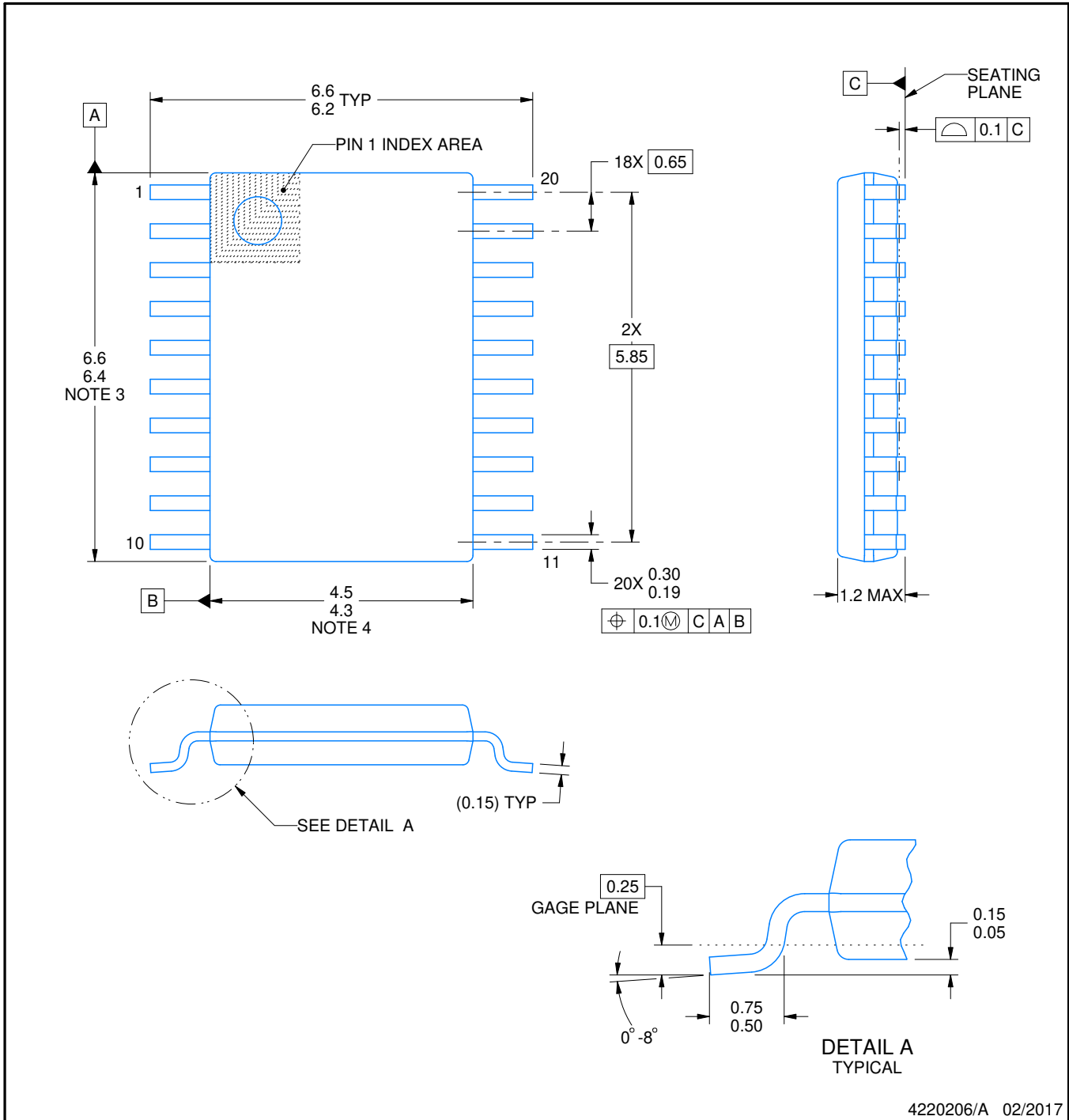
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3386ECDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3386EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX3386ECPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MAX3386EIDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3386EIPW	PW	TSSOP	20	70	530	10.2	3600	3.5



4220206/A 02/2017

NOTES:

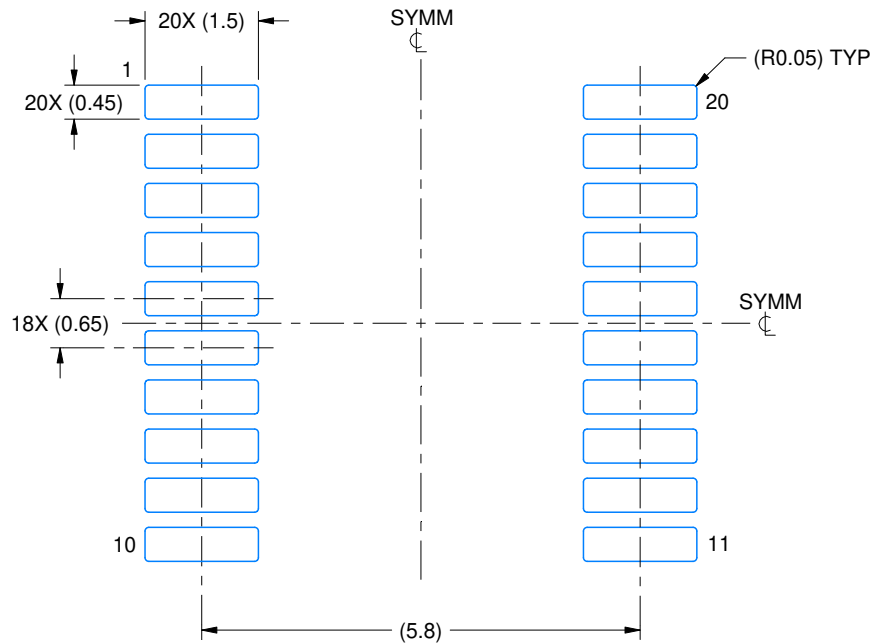
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

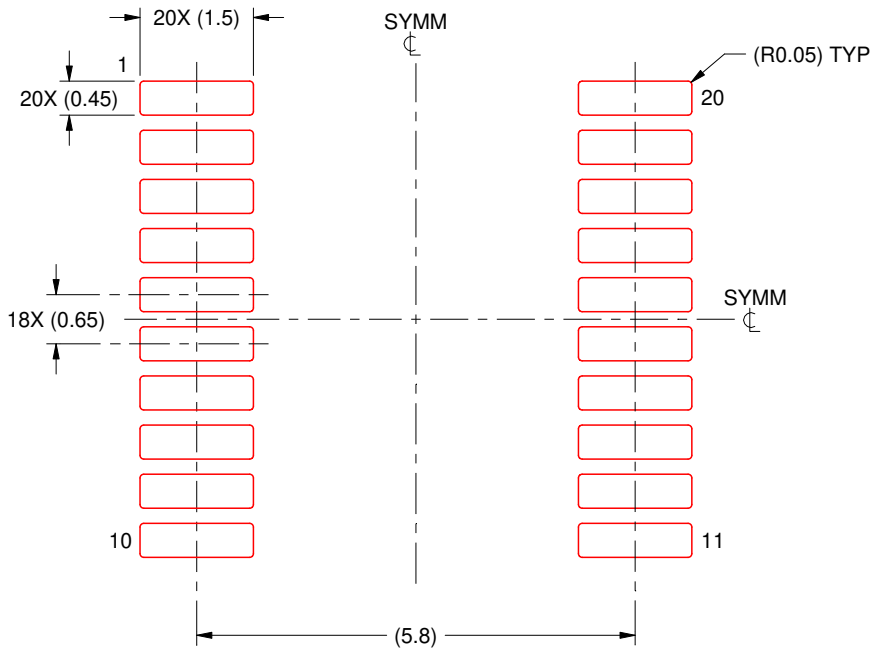
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

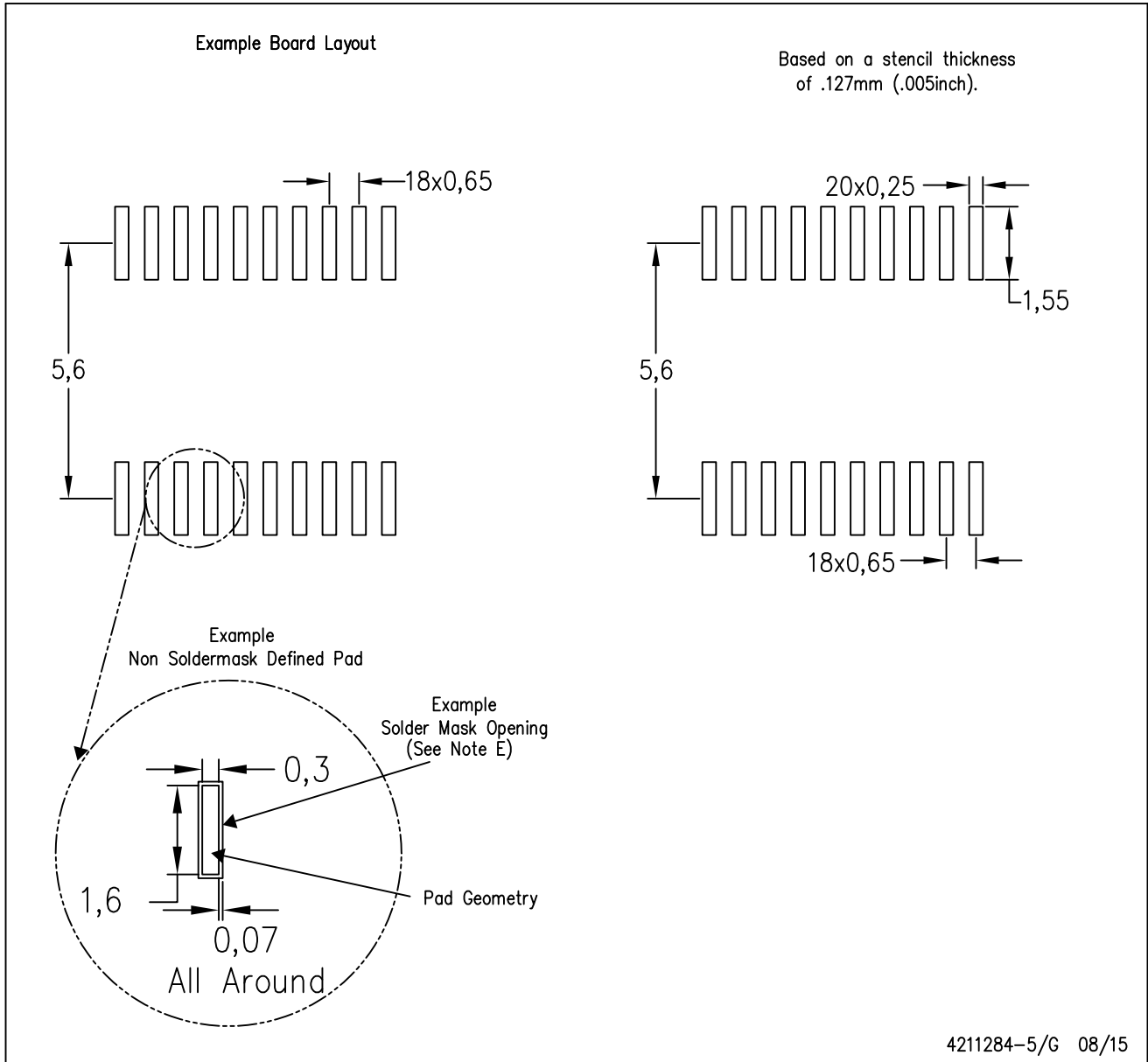
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

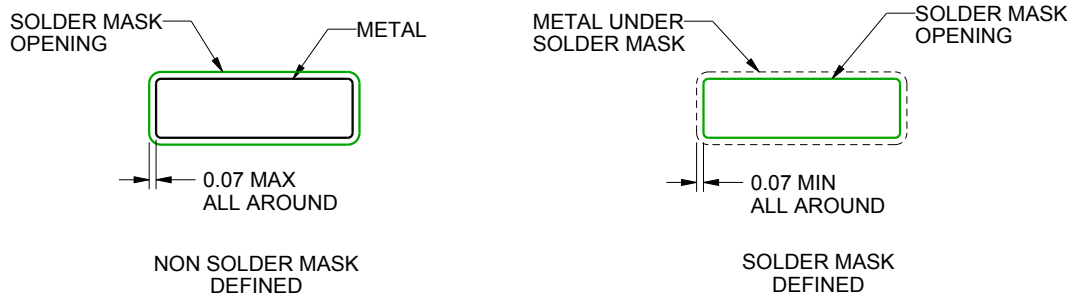
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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