

Single channel high-side driver with analog current sense for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max on-state resistance (per ch.)	R_{ON}	6 m Ω
Current limitation (typ)	I_{LIMH}	90 A
Off-state supply current	I_S	2 $\mu A^{(1)}$

1. Typical value with all loads connected.

- General
 - Very low standby current
 - 3.0 V CMOS compatible inputs
 - Optimized electromagnetic emissions
 - Very low electromagnetic susceptibility
 - Compliance with European directive 2002/95/EC
 - Very low current sense leakage
- Diagnostic functions
 - Proportional load current sense
 - High current sense precision for wide currents range
 - Diagnostic enable pin
 - Off-state open-load detection
 - Output short to V_{CC} detection
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
- Protection
 - Inrush current active management by power limitation

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Overtemperature shutdown with auto restart (thermal shutdown)
- Reverse battery protected with self switch of the Power MOSFET
- Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads

Description

The VN5E006ASP-E is a single channel high-side driver manufactured using ST proprietary VIPower[®] M0-5 technology and housed in PowerSO-10 package. The device is designed to drive 12 V automotive grounded loads delivering protection, diagnostics. It also implements a 3 V and 5 V CMOS-compatible interface for use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, over-temperature indication, short-circuit to V_{CC} diagnosis and on-state and off-state open-load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the DE pin low to share the external sense resistor with similar devices.

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1 Block diagram and pin description

Figure 1. Block diagram

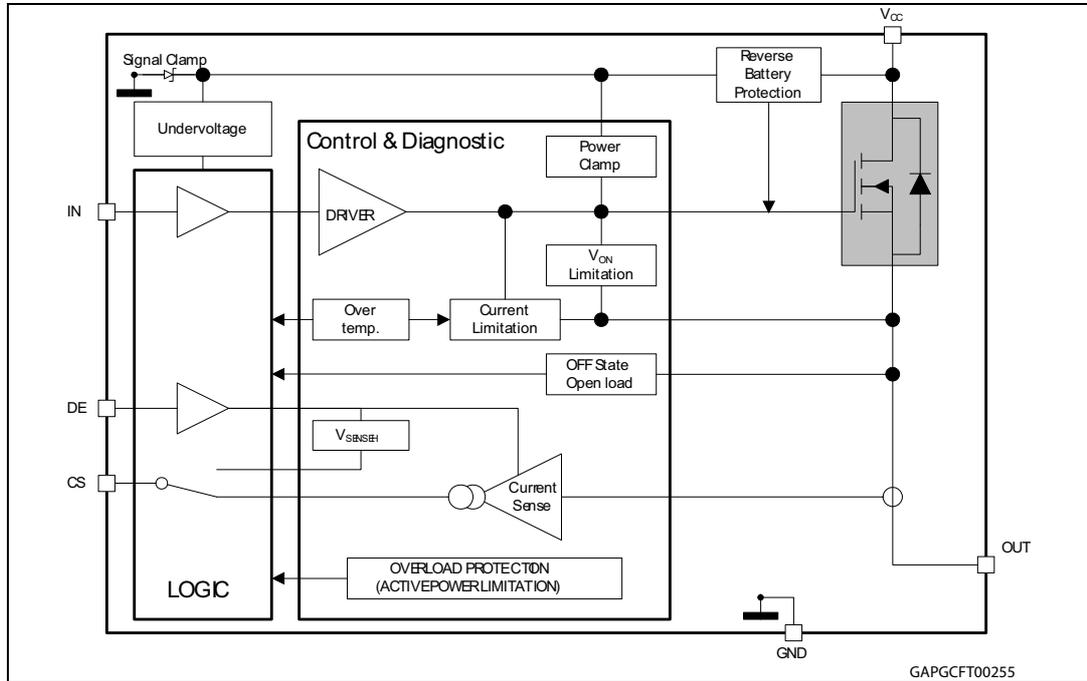


Table 1. Pin function

Name	Function
V _{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection.
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current.
DE	Active high diagnostic enable pin.

Figure 2. Configuration diagram (top view)

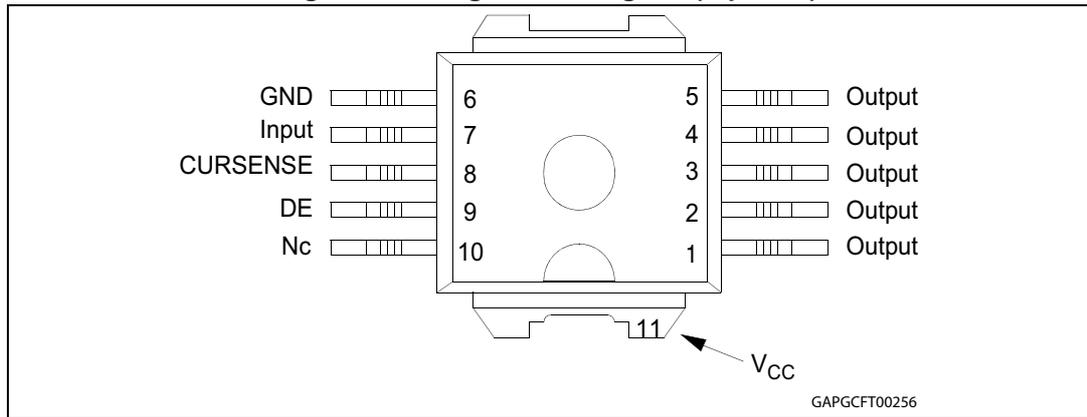
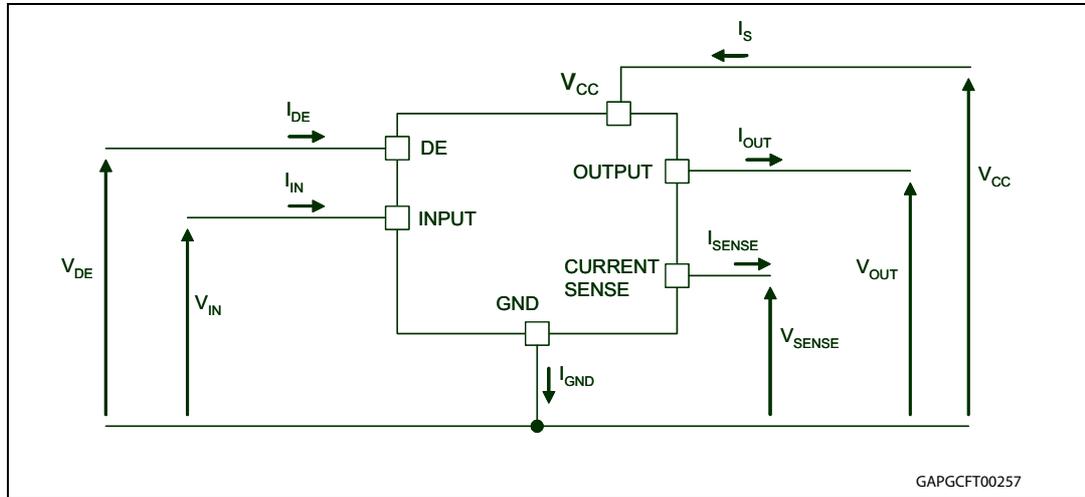


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	DE
Floating	Not allowed	X	X	X	X
To ground	Through 1K Ω resistor	X	Not allowed	Through 10K Ω resistor	Through 10K Ω resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage ($T < 400$ ms, $R_{LOAD} > 0.5 \Omega$)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	60	A
I_{IN}	DC input current	-1 to 10	mA
I_{DE}	DC diagnostic enable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 1.4$ mH; $R_L = 0 \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}(Typ.)$)	600	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5$ K Ω ; $C = 100$ pF)	2000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj-case}$	Thermal resistance junction-case (one channel ON)	0.45	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See Figure 36 in the thermal section	°C/W

2.3 Electrical characteristics

$8\text{ V} < V_{CC} < 28\text{ V}$; $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON state resistance	$I_{OUT} = 10\text{ A}$; $T_j = 25\text{ °C}$		4.5		m Ω
		$I_{OUT} = 10\text{ A}$; $T_j = 150\text{ °C}$			9	
		$I_{OUT} = 10\text{ A}$; $V_{CC} = 5\text{ V}$; $T_j = 25\text{ °C}$			6	
$R_{ON\ REV}$	Reverse battery on state resistance	$V_{CC} = -13\text{ V}$; $I_{OUT} = -10\text{ A}$; $T_j = 25\text{ °C}$			6	m Ω
V_{clamp}	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V
I_S	Supply current	Disable $V_{DE} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$; $V_{IN}=x$; $V_{OUT} = V_{SENSE} = 0\text{ V}$		2	5	μA
		Off state; $V_{CC} = 13\text{ V}$; $V_{DE} = 5\text{ V}$; $T_j = 25\text{ °C}$; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		10 ⁽¹⁾	15 ⁽¹⁾	
		On state; $V_{CC} = 13\text{ V}$; $V_{DE} = 5\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$		2	4	mA
$I_{L(off1)}$	Off state output current ⁽²⁾	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$	0		5	

1. PowerMOS leakage included.

2. For each channel.

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 1.3\ \Omega$ (see Figure 6)	—	30	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 1.3\ \Omega$ (see Figure 6)	—	30	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 1.3\ \Omega$	—	See Figure 27	—	V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 1.3\ \Omega$	—	See Figure 28	—	V/ μs
W_{ON}	Switching energy losses during t_{won}	$R_L = 1.3\ \Omega$ (see Figure 6)	—	3	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 1.3\ \Omega$ (see Figure 6)	—	1.5	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		
V_{DEL}	DE low level voltage				0.9	V
I_{DEL}	DE low level current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{DEH}	DE high level voltage		2.1			V
I_{DEH}	DE high level current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{DE(hyst)}$	DE hysteresis voltage		0.25			V
V_{DECL}	DE clamp voltage	$I_{DE} = 1\text{ mA}$	5.5		7	V
		$I_{DE} = -1\text{ mA}$		-0.7		

Table 8. Protections and diagnostic⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	$V_{CC} = 13\text{ V}$	63.5	90	127	A
		$5\text{ V} < V_{CC} < 24\text{ V}$			127	
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13\text{ V}; T_R < T_j < T_{TSD}$		25		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
T_{RS}	Thermal reset of status		135			$^{\circ}\text{C}$
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)			7		$^{\circ}\text{C}$
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT} = 2\text{ A}; V_{IN} = 0; L = 6\text{ mH}$	$V_{CC} - 28$	$V_{CC} - 31$	$V_{CC} - 35$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 1.2\text{ A}; T_j = -40\text{ }^{\circ}\text{C} \dots 150\text{ }^{\circ}\text{C}$ (see Figure 8)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 5 A; V _{SENSE} = 0.5 V; V _{DE} = 5 V; T _j = -40 °C...150 °C	7350	10700	14590	
dK ₀ /K ₀ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 5 A; V _{SENSE} = 0.5 V; V _{DE} = 5 V; T _j = -40 °C to 150 °C	-12		12	%
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 10 A; V _{SENSE} = 4 V V _{DE} = 5 V T _j = -40 °C...150 °C T _j = 25 °C...150 °C	7490 8240	10500 10500	13930 12815	
dK ₁ /K ₁ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{DE} = 5 V; T _j = -40 °C to 150 °C	-12		12	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 15 A; V _{SENSE} = 4 V V _{DE} = 5 V T _j = -40 °C...150 °C T _j = 25 °C...150 °C	8340 8680	10400 10400	12760 12070	
dK ₂ /K ₂ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 15 A; V _{SENSE} = 4 V; V _{DE} = 5 V; T _j = -40 °C to 150 °C	-8		8	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 25 A; V _{SENSE} = 4 V V _{DE} = 5 V T _j = -40 °C...150 °C T _j = 25 °C...150 °C	8785 8965	10300 10300	11950 11545	
dK ₃ /K ₃ ⁽¹⁾	Current sense ratio drift	I _{OUT} = 25 A; V _{SENSE} = 4 V; V _{DE} = 5 V; T _j = -40 °C to 150 °C	-6		6	%
I _{SENSE0}	Analog sense leakage current	I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{DE} = 0 V; V _{IN} = 0 V; T _j = -40 °C...150 °C	0		1	μA
		I _{OUT} = 0 A; V _{DE} = 5 V; V _{IN} = 5 V; V _{SENSE} = 0 V T _j = -40 °C...150 °C	0		2	
		I _{OUT} = 10 A; V _{DE} = 0 V; V _{SENSE} = 0 V; V _{IN} = 5 V;	0		1	
I _{OL}	Open-load on state current detection threshold	V _{IN} = 0 V, 8 V < V _{CC} < 18 V; I _{SENSE} = 5 μA	10		100	mA
V _{SENSE}	Max analog sense output voltage	I _{OUT} = 25 A; V _{DE} = 5 V; R _{SENSE} = 3.9 KΩ	5			V
V _{SENSEH} ⁽²⁾	Analog sense output voltage in fault conditions	V _{CC} = 13 V; R _{SENSE} = 10 KΩ		8		V
I _{SENSEH} ⁽¹⁾	Analog sense output current in fault conditions	V _{CC} = 13 V; V _{SENSE} = 5 V		9		mA

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t _{DSENSE1H}	Delay response time from falling edge of DE pin	V _{SENSE} < 4 V, 5 A < I _{out} < 25 A I _{SENSE} = 90 % of I _{SENSE max} (see Figure 4)		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of DE pin	V _{SENSE} < 4 V, 5 A < I _{out} < 25 A I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		5	20	μs
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} < 4 V, 5 A < I _{out} < 25 A I _{SENSE} = 90 % of I _{SENSE max} (see Figure 4)		200	600	μs
Δt _{DSENSE2H}	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4 V, I _{SENSE} = 90 % of I _{SENSEMAX} , I _{OUT} = 90 % of I _{OUTMAX} I _{OUTMAX} = 25 A (see Figure 7)			200	μs
t _{DSENSE2L}	Delay response time from falling edge of INPUT pin	V _{SENSE} < 4 V, 5 A < I _{out} < 25 A I _{SENSE} = 10 % of I _{SENSE max} (see Figure 4)		100	250	μs

1. Parameter guaranteed by design; it is not tested.
2. Fault conditions include: power limitation, overtemperature and open load OFF state detection.

Table 10. Open-load detection (8 V < V_{CC} < 18 V, V_{DE} = 5 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{OL}	Open-load off state voltage detection threshold	V _{IN} = 0 V; V _{DE} = 5 V; See Figure 5	2	—	4	V
t _{DSTKON}	Output short circuit to V _{CC} detection delay at turn off	V _{DE} = 5 V; See Figure 5	180	—	1200	μs
I _{L(off2)r}	Off-state output current at V _{OUT} = 4V	V _{IN} = 0 V; V _{SENSE} = 0 V V _{DE} = 5 V; V _{OUT} rising from 0V to 4 V	-120	—	90	μA
I _{L(off2)f}	Off-state output current at V _{OUT} = 2V	V _{IN} = 0 V; V _{SENSE} = V _{SENSEH} V _{DE} = 5 V; V _{OUT} falling from V _{CC} to 2 V	-50	—	90	μA
td_vol	Delay response from output rising edge to V _{SENSE} rising edge in open load	V _{OUT} = 4 V; V _{IN} = 0 V V _{DE} = 5 V; V _{SENSE} = 90 % of V _{SENSEH}		—	20	μs
td_voh	Delay response from output falling edge to V _{SENSE} falling edge in open-load	V _{OUT} = 2 V; V _{IN} = 0 V V _{DE} = 5 V; V _{SENSE} = 10 % of V _{SENSEH}		—	20	μs

Figure 4. Current sense delay characteristics

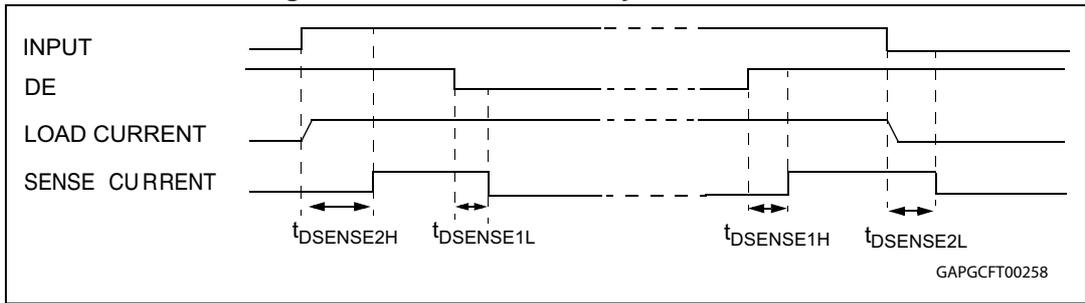


Figure 5. Open load Off-state delay timing

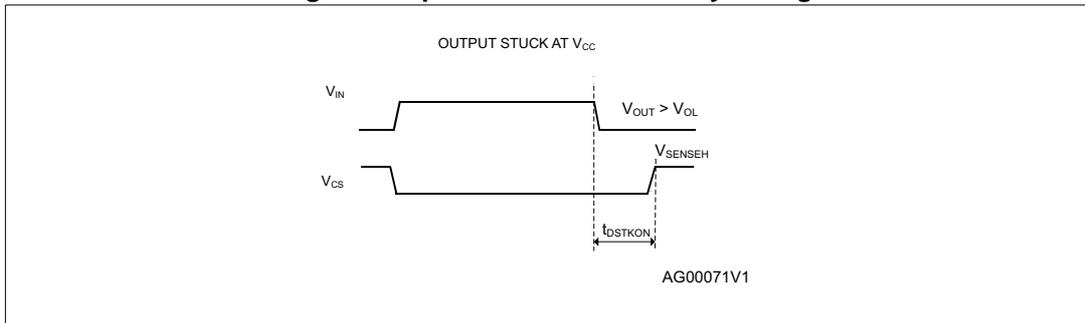


Figure 6. Switching characteristics

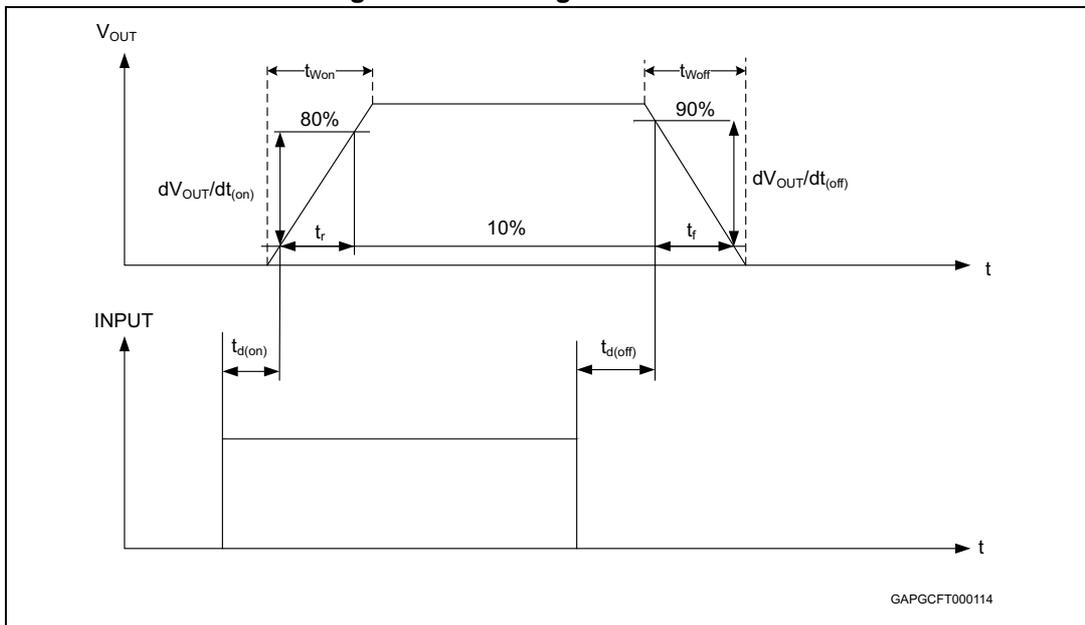


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

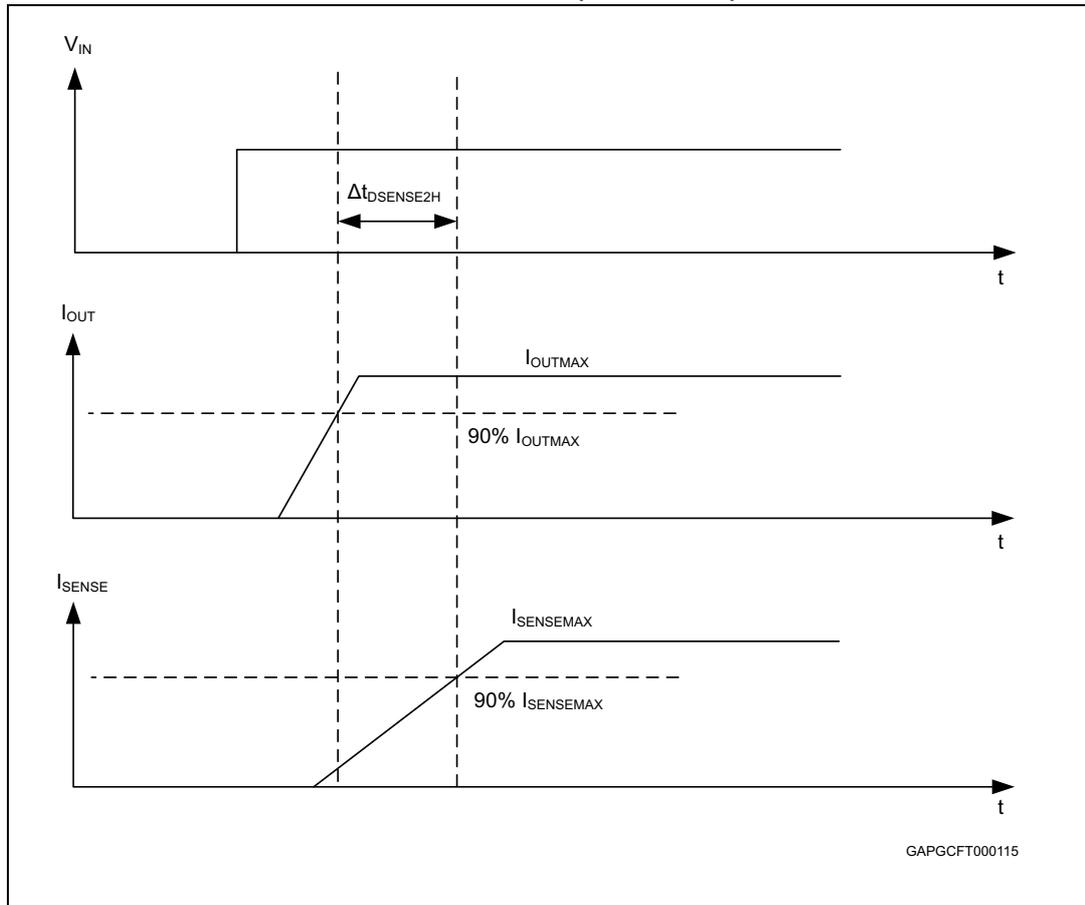


Figure 8. Output voltage drop limitation

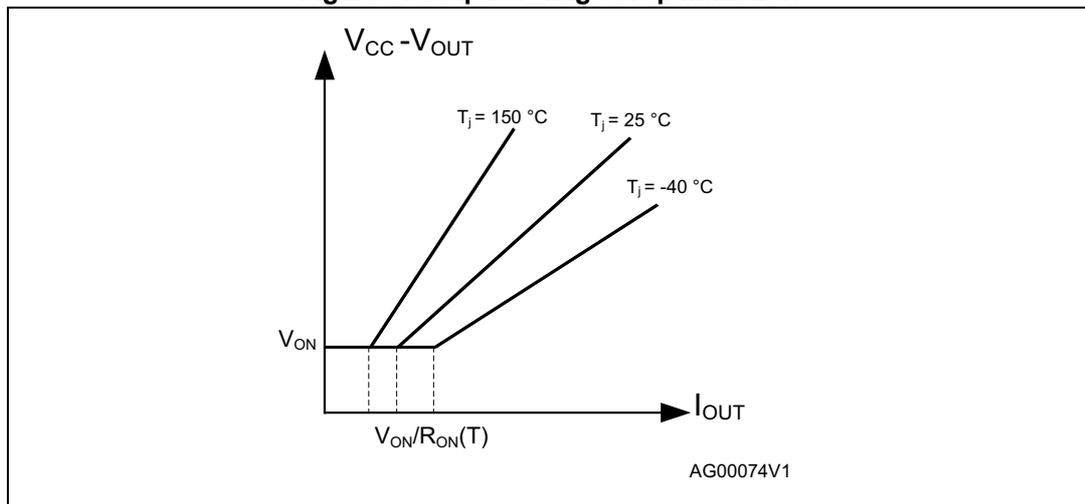


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}

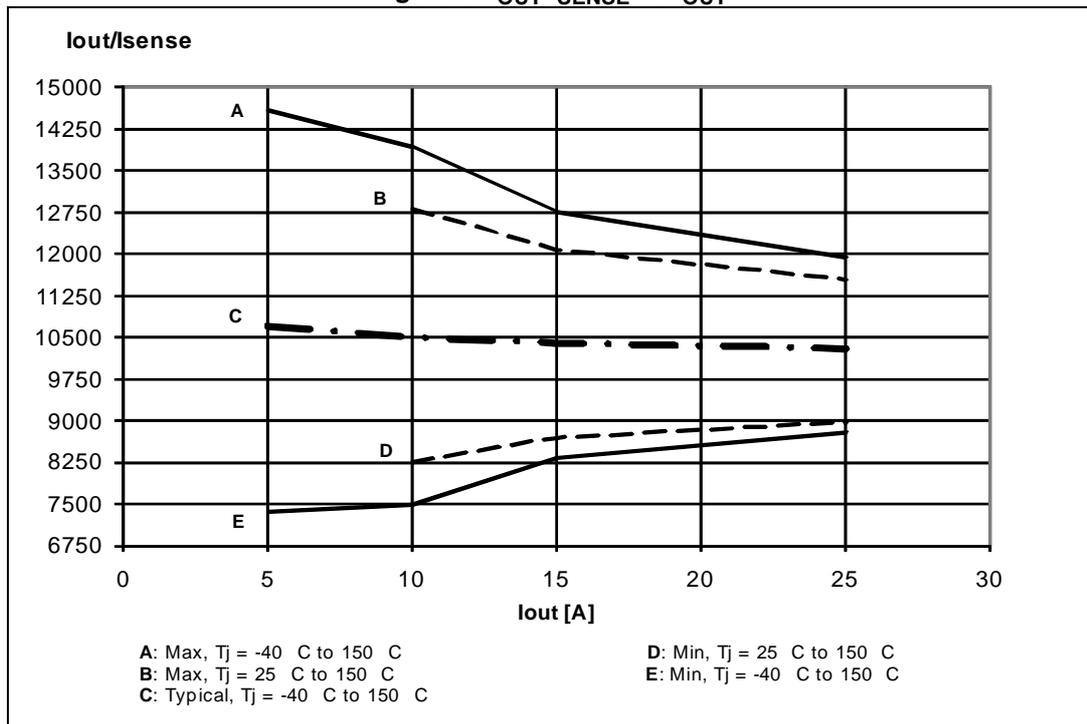


Figure 10. Maximum current sense ratio drift vs load current

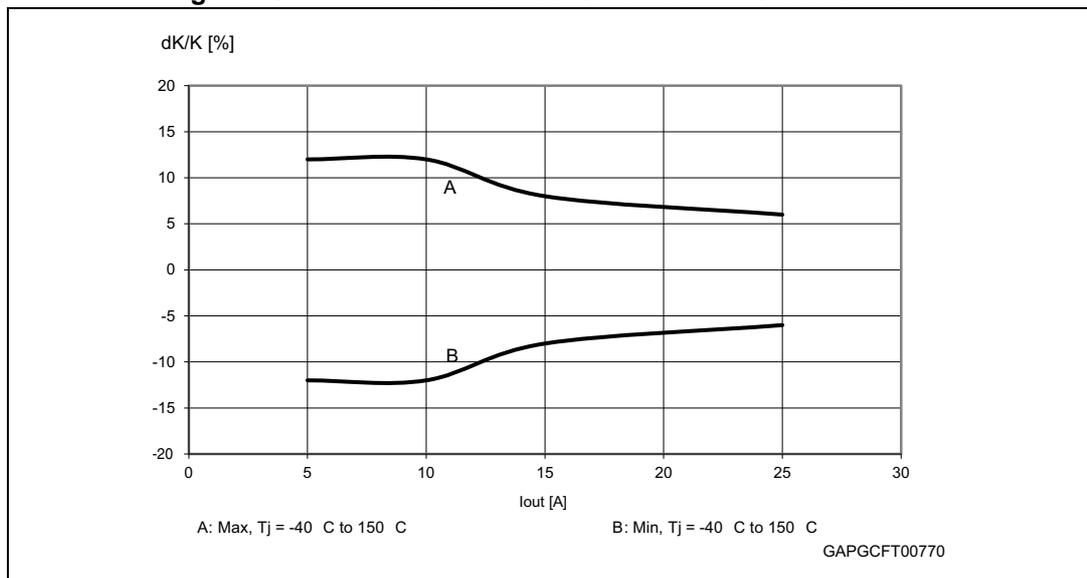


Table 11. Truth table

Conditions	Enable	Input	Output	Sense ($V_{DE} = 5\text{ V}$) ⁽¹⁾
Normal operation	H	L	L	0
	H	H	H	Nominal
Overtemperature	H	L	L	0
	H	H	L	V_{SENSEH}
Undervoltage	H	L	L	0
	H	H	L	0
Overload	H	H	X (no power limitation)	Nominal
	H	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (Power limitation)	H	L	L	0
	H	H	L	V_{SENSEH}
Open load OFF State (with external pull up)	H	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	H	L	H	V_{SENSEH}
	H	H	H	< Nominal
Negative output voltage clamp	H	L	L	0

1. If the V_{DE} is low, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test Pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (2) (3)	C	C

1. The above test levels must be considered referred to $V_{CC} = 13.5V$ except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 3.:](#) *Absolute maximum ratings.*

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

2.4 Waveforms

Figure 11. Normal operation

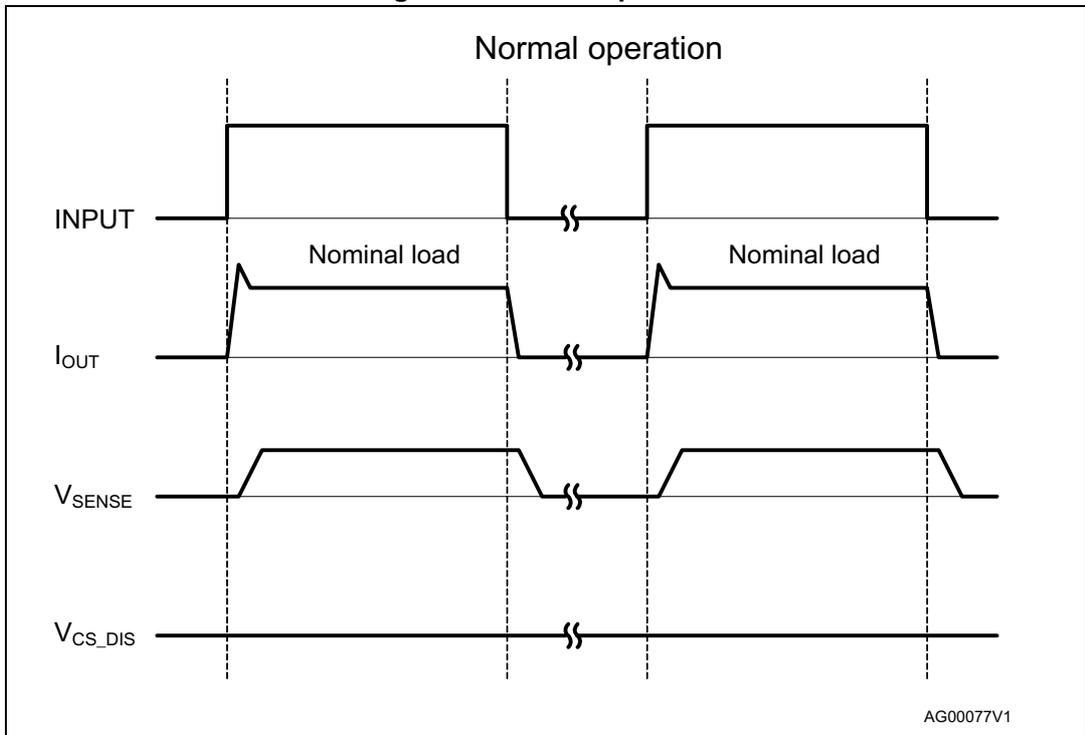


Figure 12. Overload or short to GND

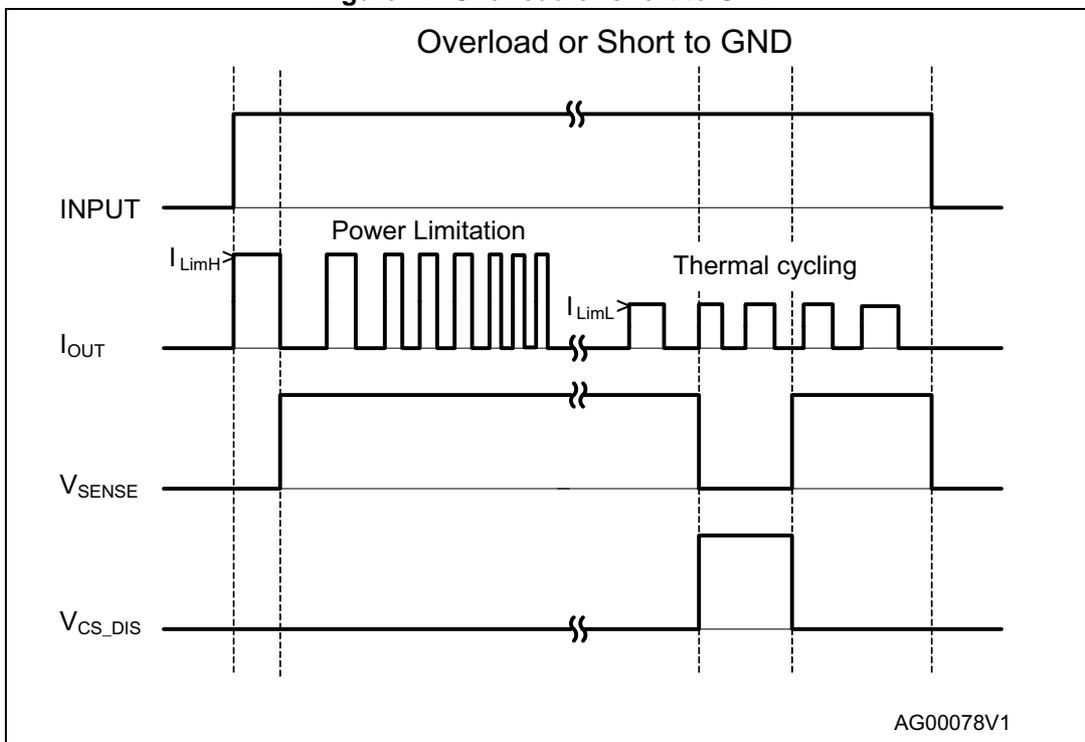
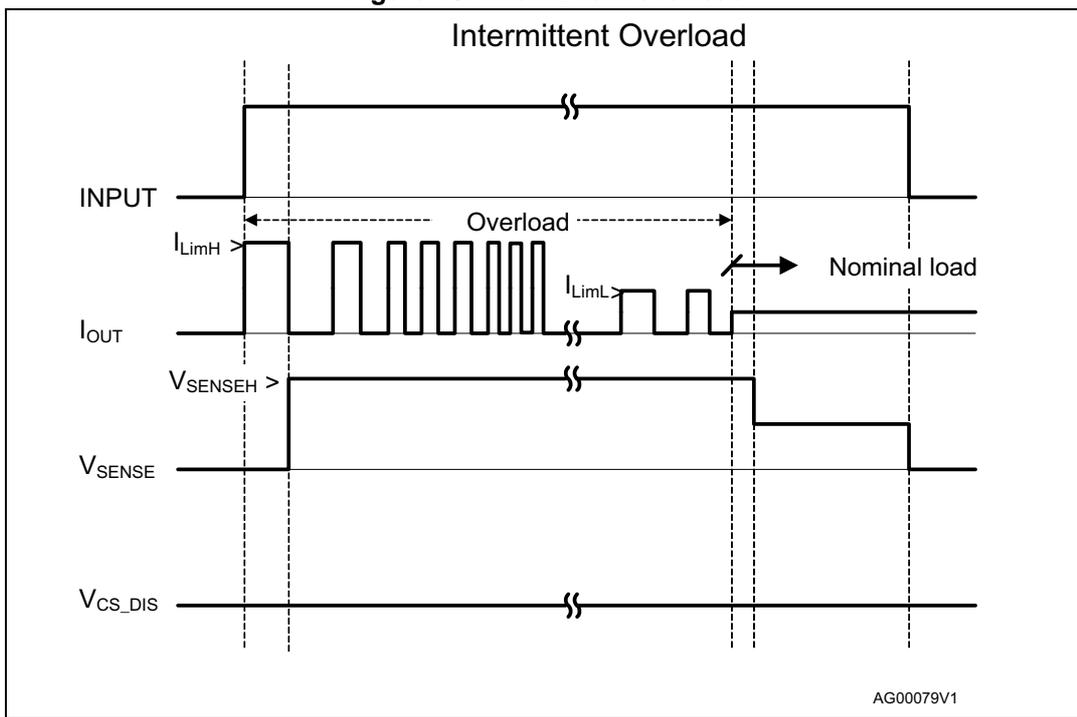
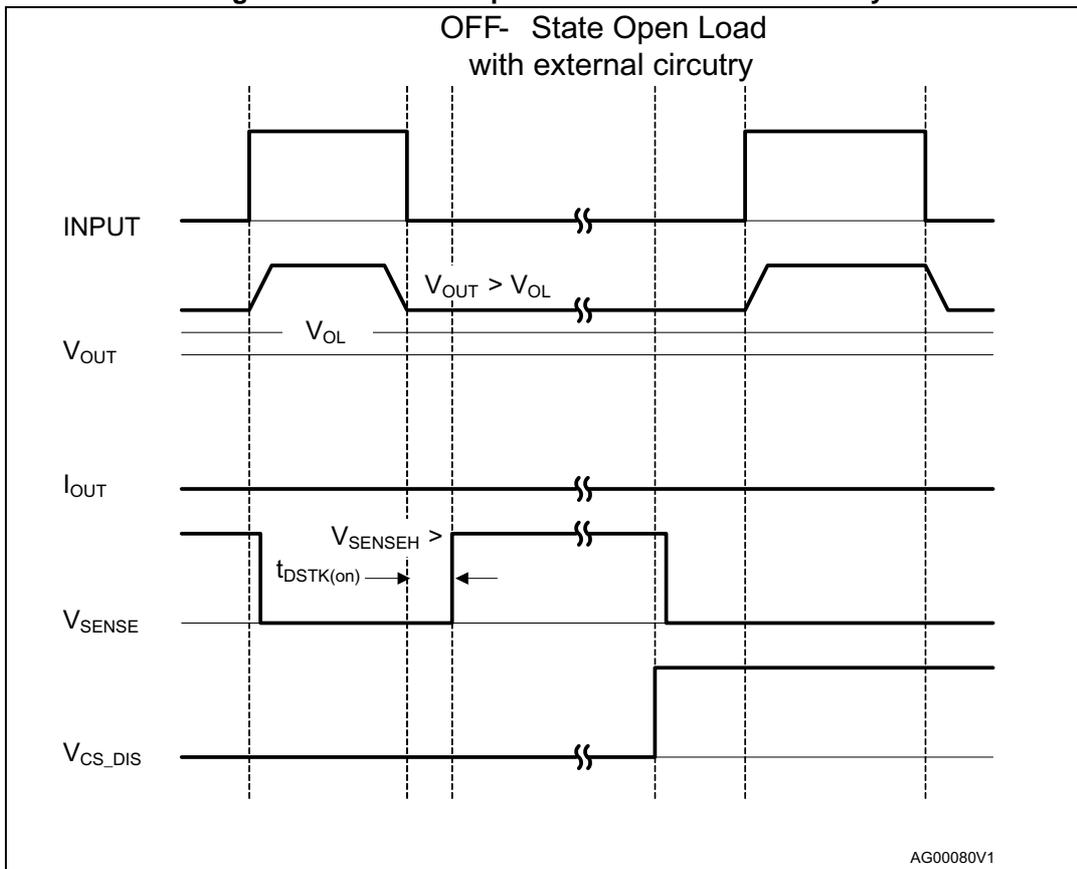


Figure 13. Intermittent overload



AG00079V1

Figure 14. OFF-state open load with external circuitry



AG00080V1

Figure 15. Short to V_{CC}

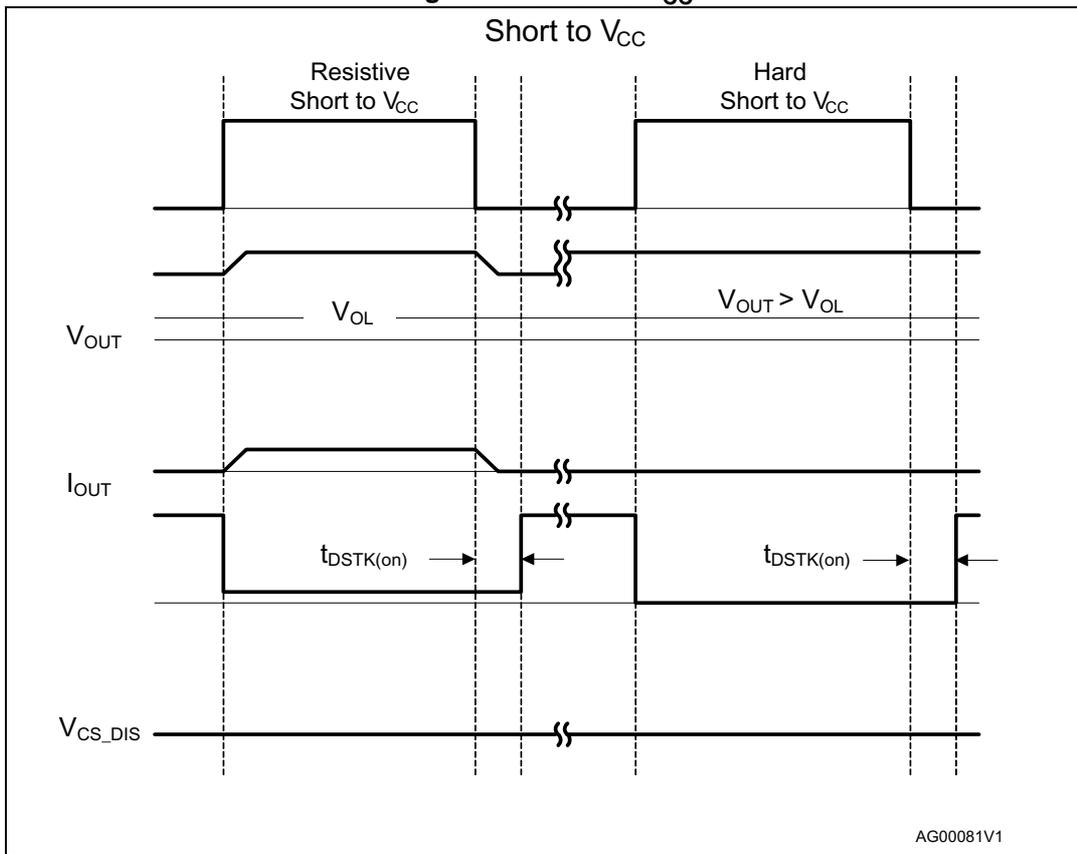
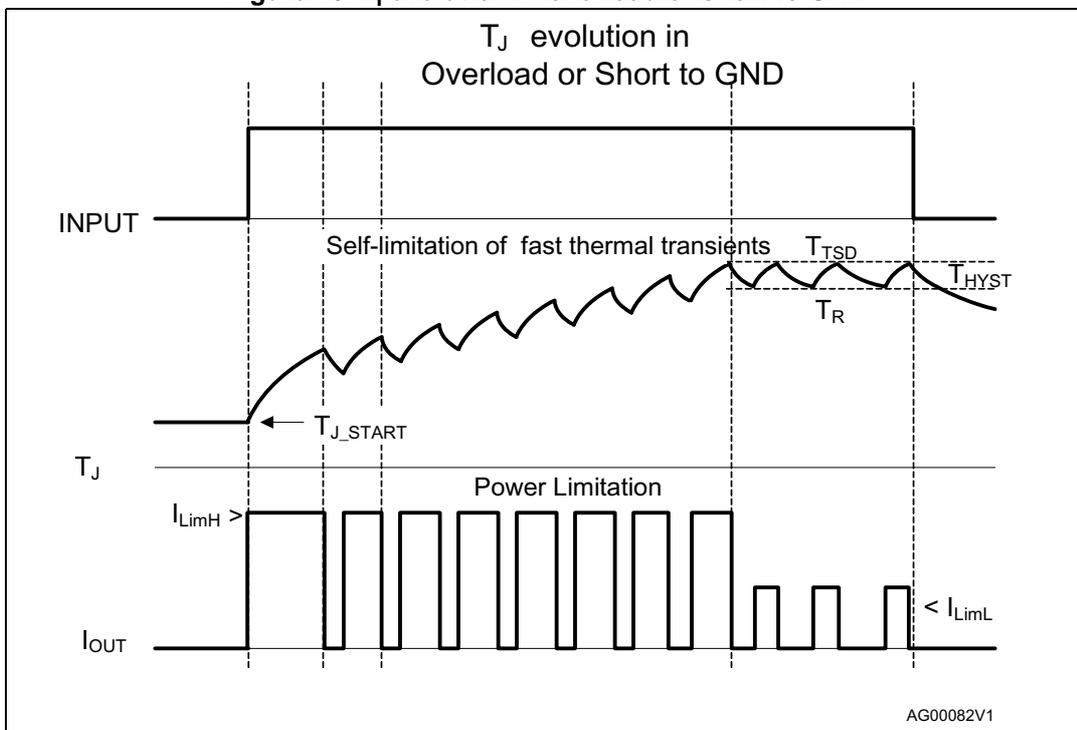


Figure 16. T_i evolution in overload or short to GND



2.5 Electrical characteristics curves

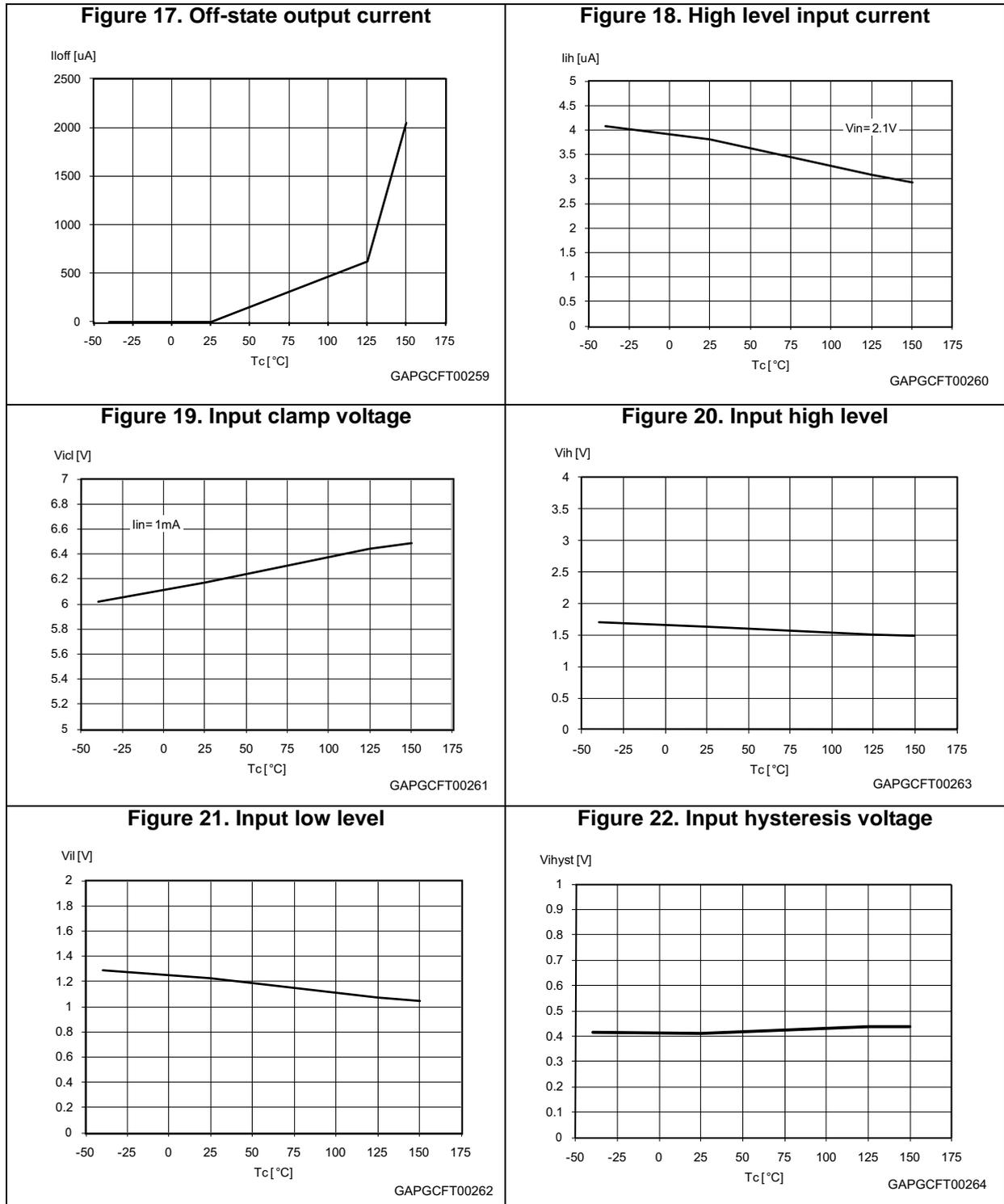


Figure 23. On-state resistance vs T_{case}

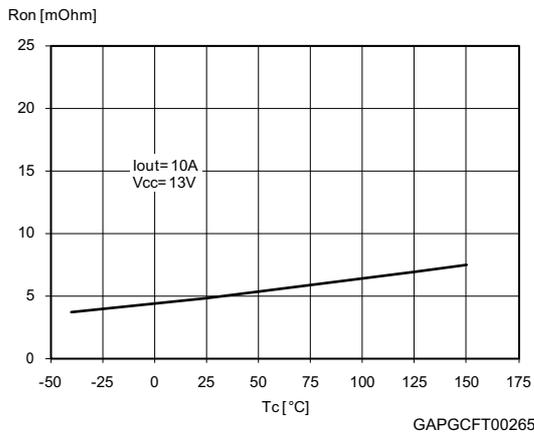


Figure 24. On state resistance vs V_{CC}

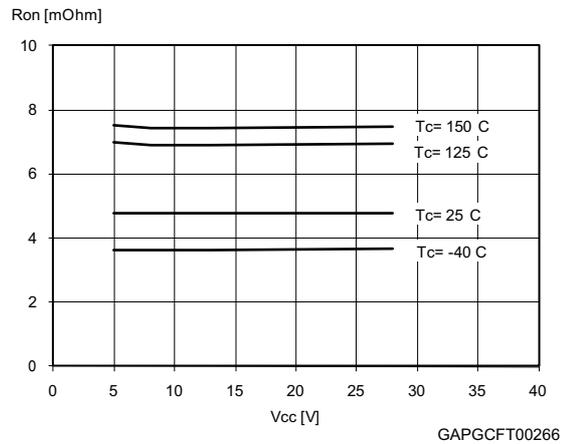


Figure 25. Undervoltage shutdown

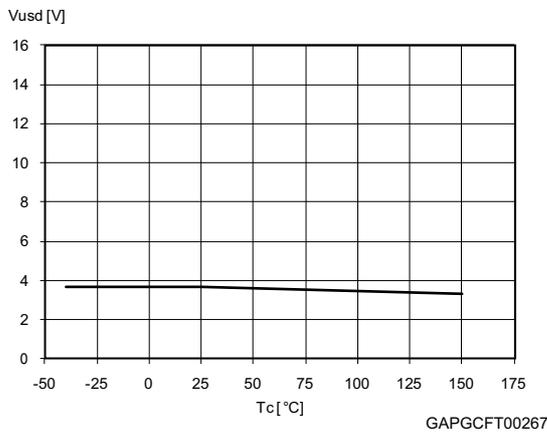


Figure 26. I_{LIMH} vs T_{case}

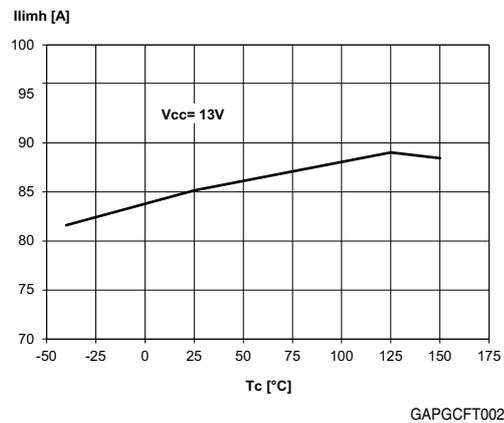


Figure 27. Turn-on voltage slope

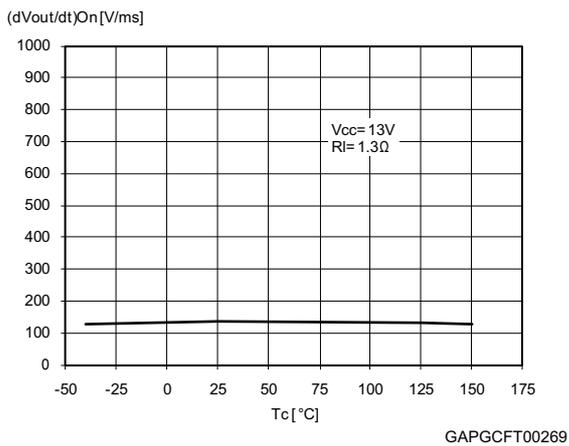


Figure 28. Turn-off voltage slope

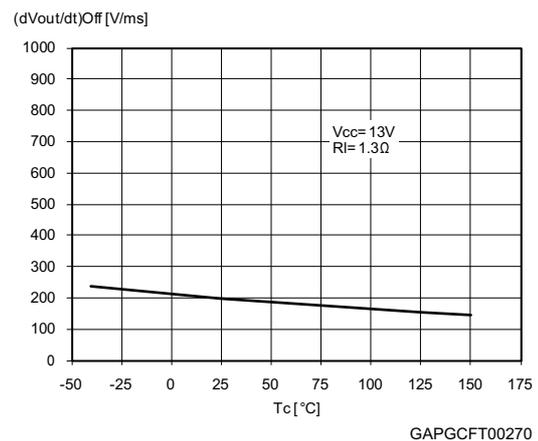


Figure 29. DE clamp voltage

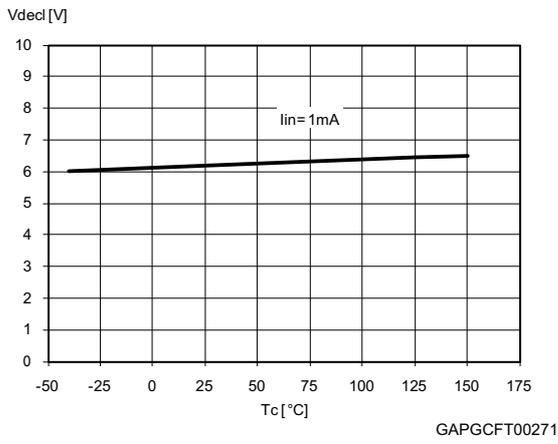


Figure 30. Low level DE voltage

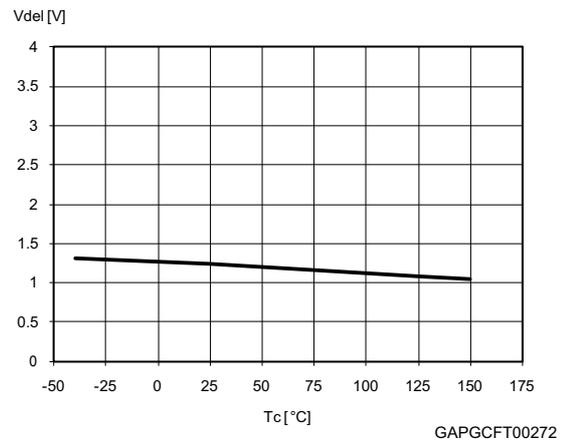
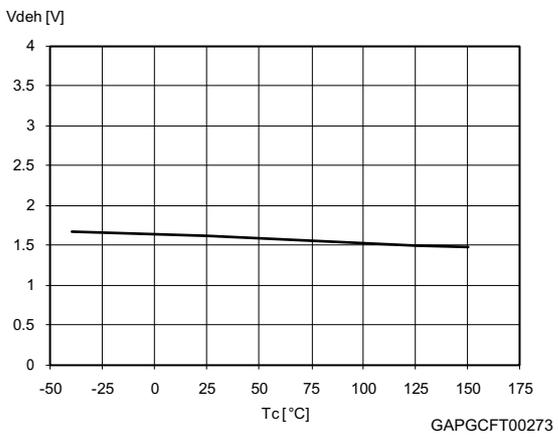
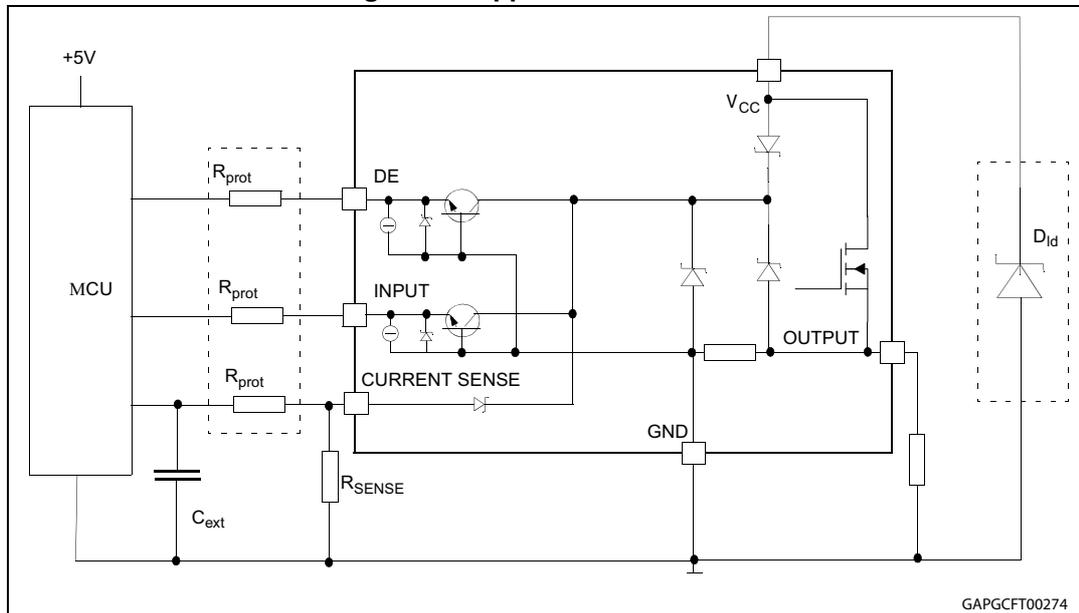


Figure 31. High level DE voltage



3 Application information

Figure 32. Application schematic



3.1 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins are pulled negative to approximately -1.5V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the microcontroller I/O pins from latching up.

The values of these resistors provide a compromise between the leakage current of the microcontroller, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -1.5\text{ V}$ and $I_{latchup} \geq 20\text{ mA}$; $V_{OH\mu C} \geq 4.5\text{ V}$

$$75\ \Omega \leq R_{prot} \leq 240\text{ k}\Omega$$

Recommended values: $R_{prot} = 10\text{ k}\Omega$, $C_{EXT} = 10\text{ nF}$

3.2 Load dump protection

D_{id} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

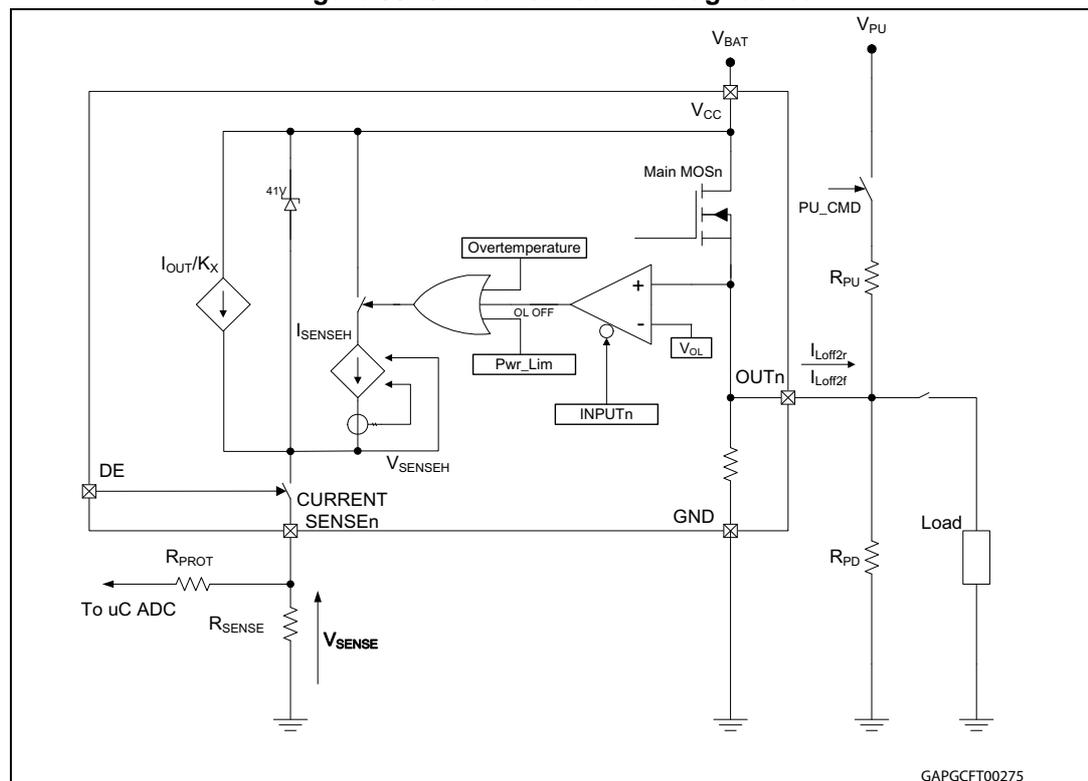
3.3 Current sense and diagnostic

The current sense pin performs a double function (see [Figure 33: Current sense and diagnostics](#)):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load one according to a known ratio K_X .
The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in [Table 9: Current sense \(8 V < \$V_{CC}\$ < 18 V\)](#)). The current sense accuracy depends on the output current (refer to current sense electrical characteristics [Table 9: Current sense \(8 V < \$V_{CC}\$ < 18 V\)](#)).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to [Truth table](#)):
 - Power limitation activation
 - Overtemperature
 - Short to V_{CC} in OFF-state
 - Open-load in OFF-state with additional external components.

A logic level low on DE pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostics



3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off state. Small or no current is delivered by the current sense during the on state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see [Figure 33: Current sense and diagnostics](#)).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled up by the external circuitry:

$$V_{OUT}|_{Pull-up_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22 \text{ K}\Omega$ is recommended.

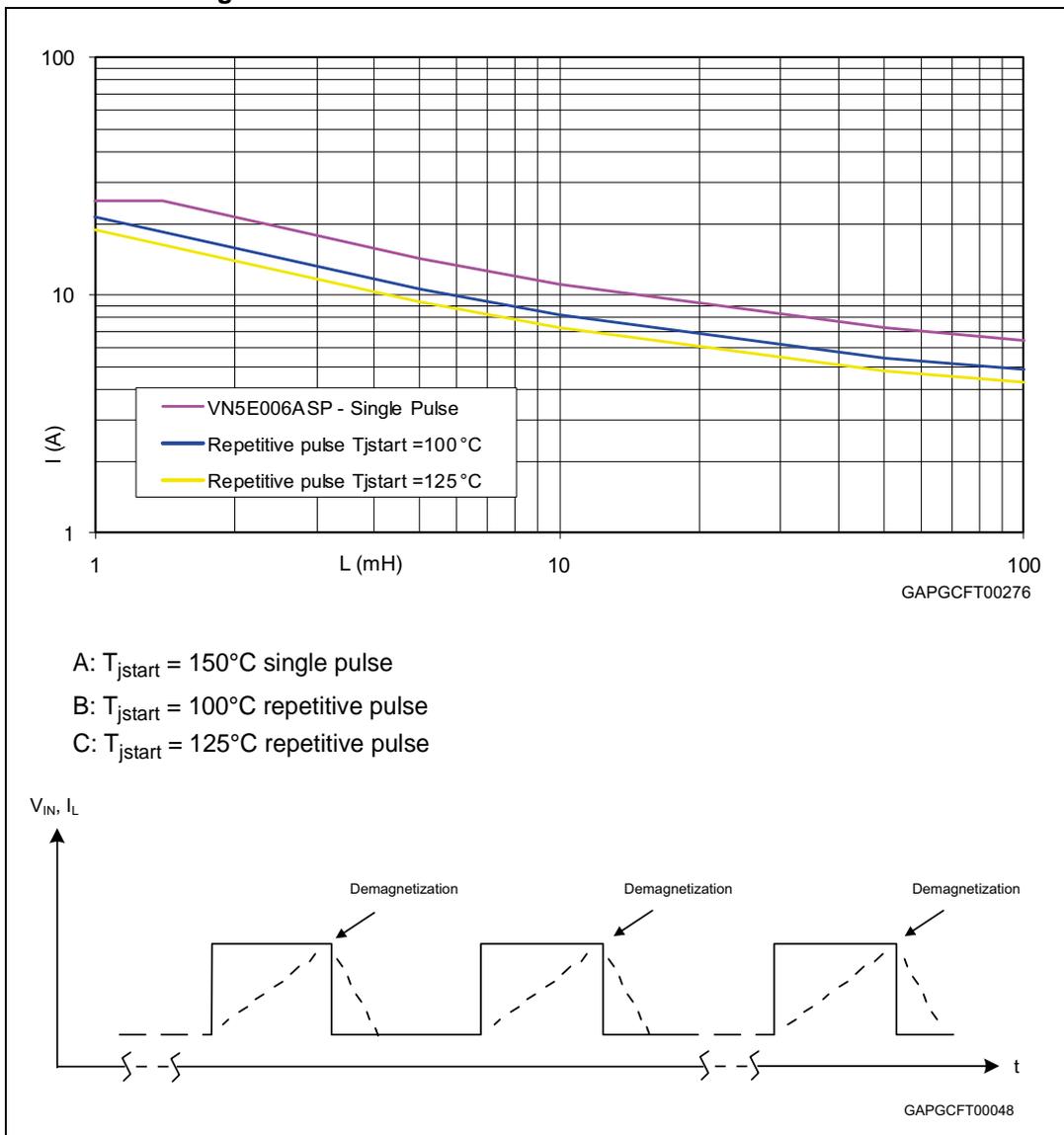
For proper open load detection in off state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}|_{Pull-up_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off2)r}}{R_{PU} + R_{PD}} > V_{OLmax} = 4V$$

For the values of V_{OLmin} , V_{OLmax} , $I_{L(off2)r}$ and $I_{L(off2)f}$ see [Table 10: Open-load detection](#) ($8 \text{ V} < V_{CC} < 18 \text{ V}$, $V_{DE} = 5 \text{ V}$).

3.4 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 34. Maximum turn-off current versus inductance

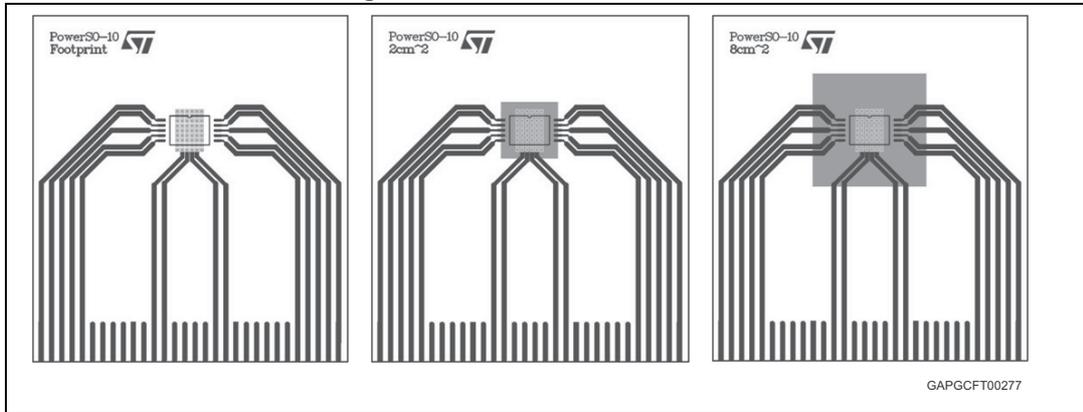


Note: Values are generated with $R_L = 0\ \Omega$.
 In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 35. PowerSO-10 PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 77x86; Board Material FR4; Cu thickness 0.070mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

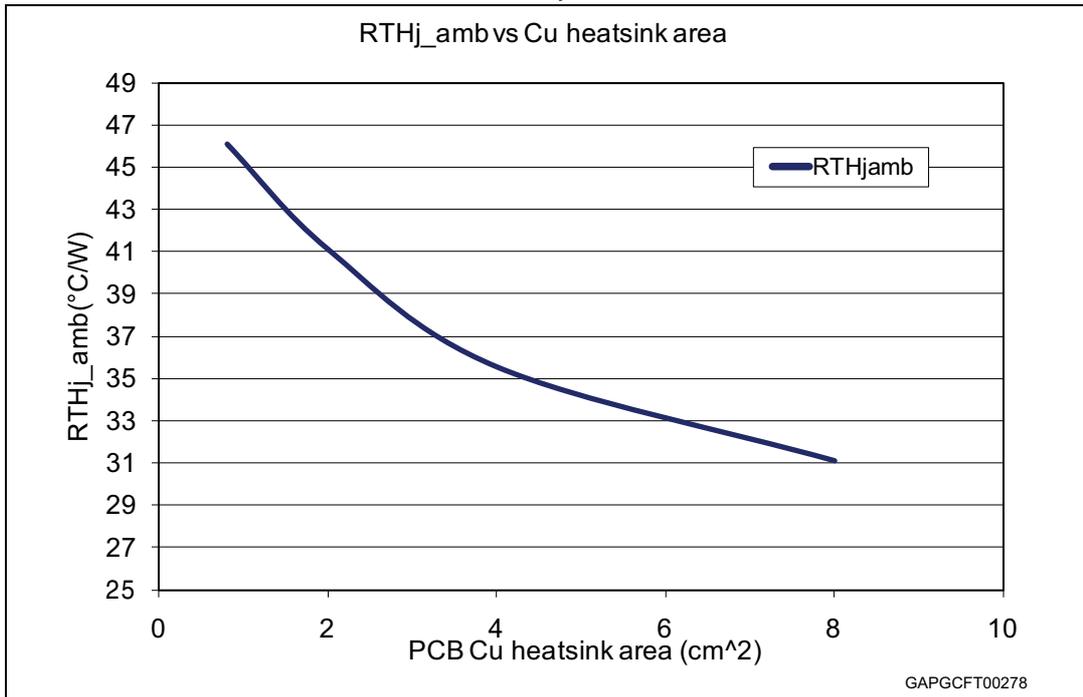


Figure 37. PowerSO-10 thermal impedance junction ambient single pulse (one channel on)

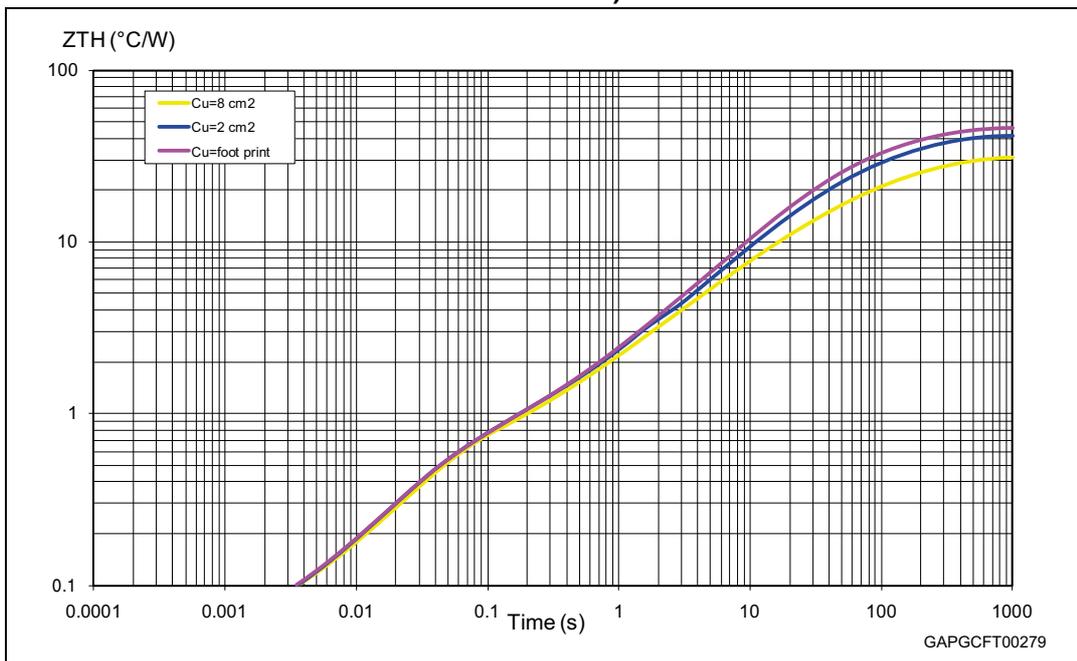
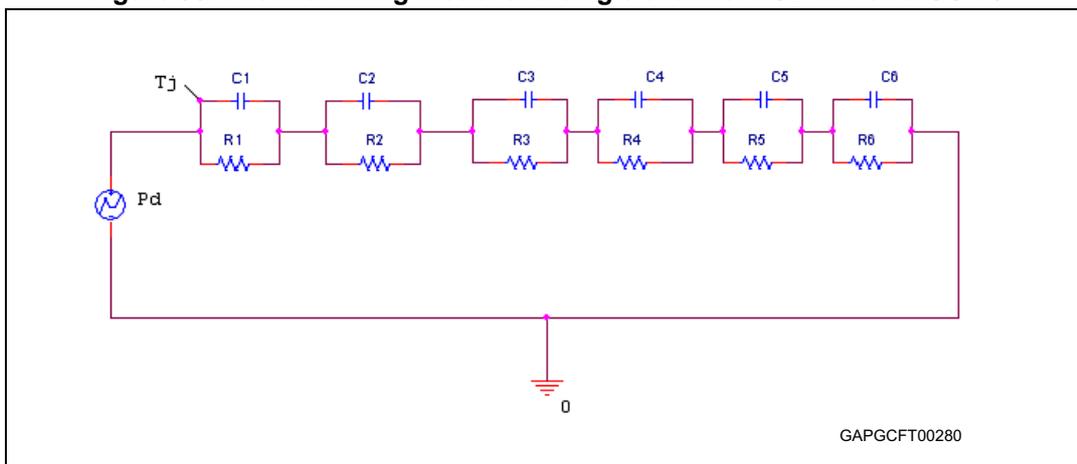


Figure 38. Thermal fitting model of a single channel HSD in PowerSO-10



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.05		
R2 (°C/W)	0.6		
R3 (°C/W)	1.5		
R4 (°C/W)	7		
R5 (°C/W)	13	12	8
R6 (°C/W)	24	20	14
C1 (W.s/°C)	0.1		
C2 (W.s/°C)	0.08		
C3 (W.s/°C)	0.8		
C4 (W.s/°C)	2		
C5 (W.s/°C)	3	4	8
C6 (W.s/°C)	6	8	14

5 Package information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.2 PowerSO-10 mechanical data

Figure 39. PowerSO-10 package dimensions

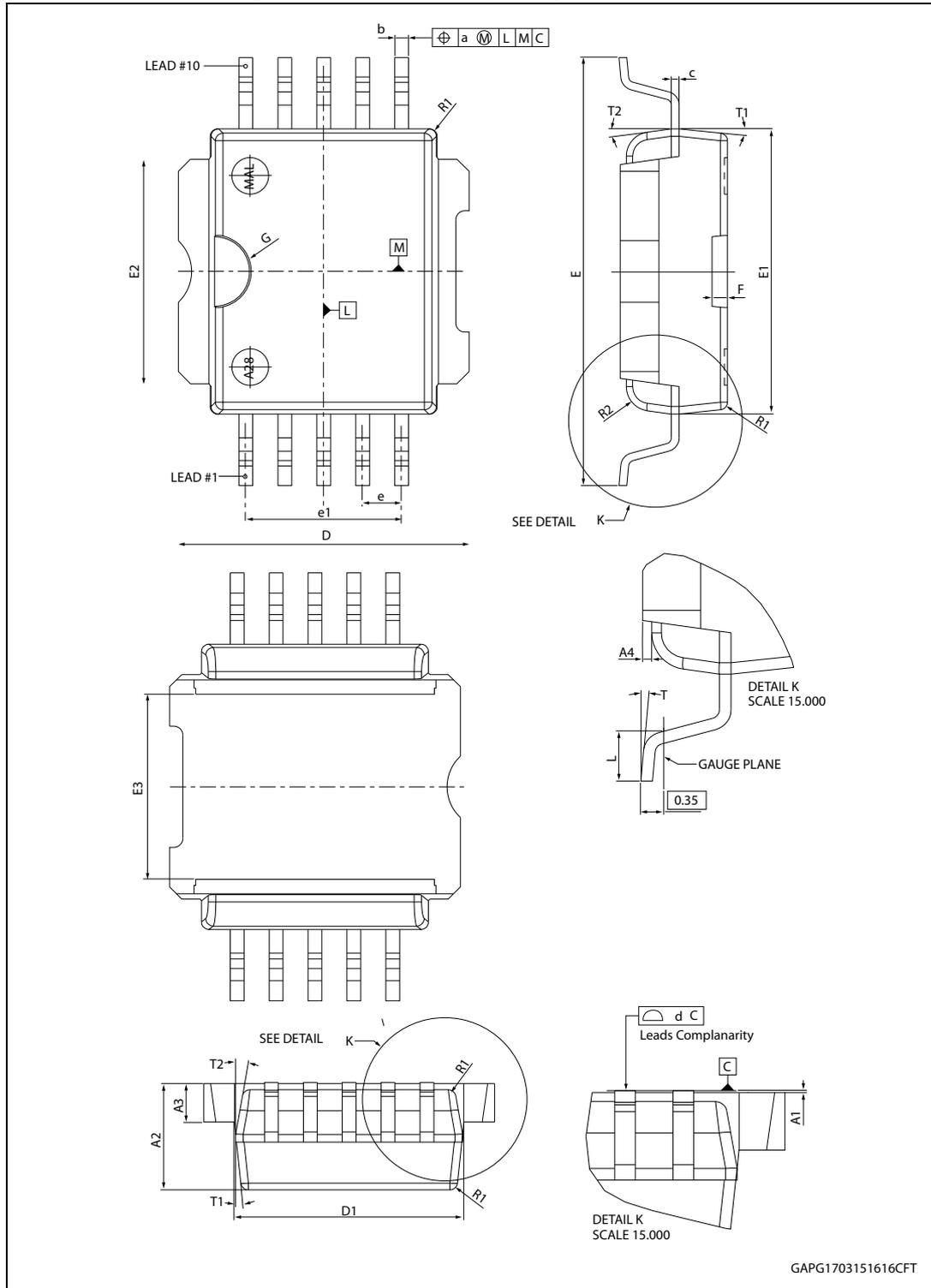


Table 16. PowerSO-10 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A1	0	0.05	0.10
A2	3.40	3.50	3.60
A3	1.20	1.30	1.40
A4	0.15	0.20	0.25
a		0.20	
b	0.37	0.45	0.53
c	0.23	0.27	0.32
D	9.40	9.50	9.60
D1	7.40	7.50	7.60
d	0	0.05	0.10
E	13.85	14.10	14.35
E1 ⁽¹⁾	9.30	9.40	9.50
E2	7.30	7.40	7.50
E3	5.90	6.10	6.30
e		1.27	
e1		5.08	
F		0.50	
G		1.20	
L	0.80	1.00	1.10
R1			0.25
R2		0.80	
T	2°	5°	8°
T1		6°	
T2		10°	

1. Resin protrusions not included (max value: 0.15 mm per side).

5.3 Packing information

Figure 40. PowerSO-10 suggested pad layout and tube shipment (no suffix)

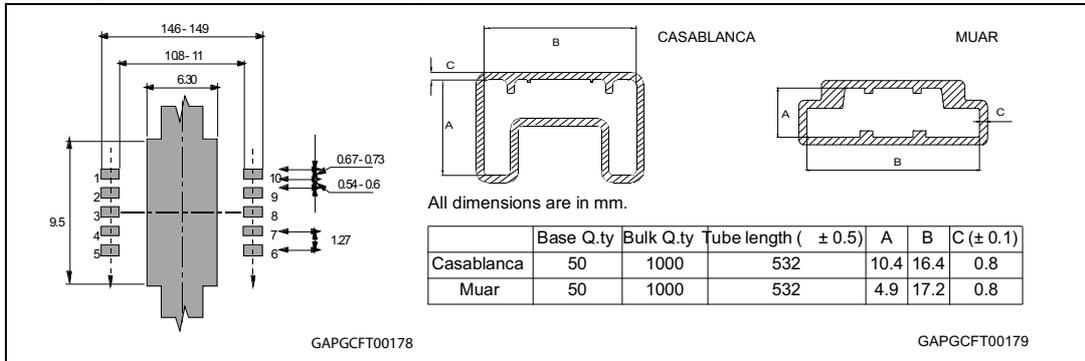
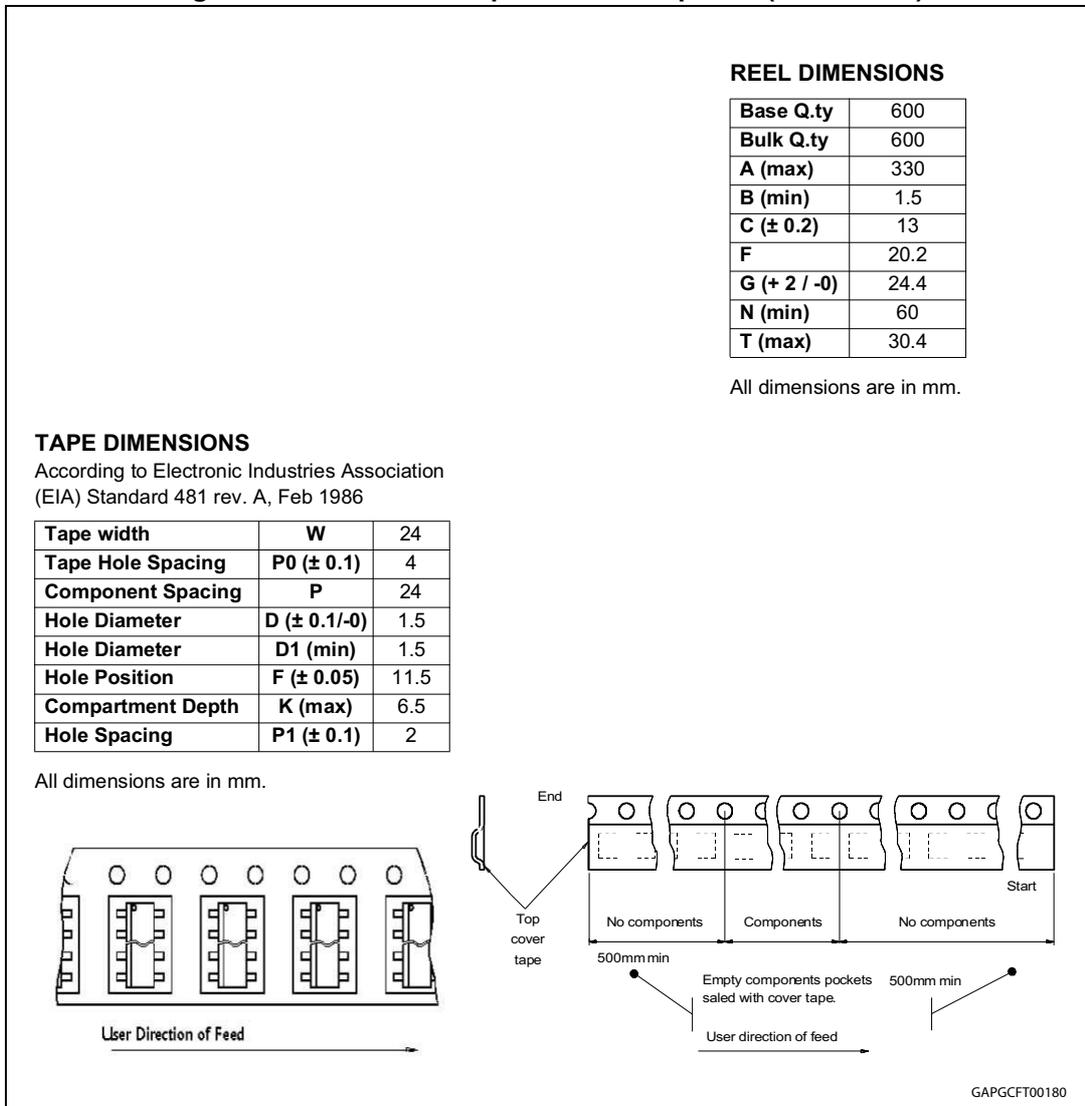


Figure 41. PowerSO-10 tape and reel shipment (suffix “TR”)



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VN5E006ASP-E	VN5E006ASPTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
01-Sep-2010	1	Internal release.
13-Sep-2010	2	<p>Updated document with diagnostic enable pin insertion. Figure 2: Configuration diagram (top view) – changed pinout Changed Figure 4: Current sense delay characteristics Table 3: Absolute maximum ratings E_{MAX}: updated parameters and value Table 4: Thermal data – $R_{thj-case}$: updated maximum value Table 5: Power section – R_{ON}: updated typical and maximum values – I_S: replaced $V_{CE} = 0\text{ V}$ with $V_{DE} = 0\text{ V}$ for test conditions, changed typ/max value (first row), replaced $V_{CE} = 5\text{ V}$ with $V_{DE} = 5\text{ V}$ for test conditions, changed typ/max value (second and third row) Table 6: Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$) – $t_{d(on)}$, $t_{d(off)}$, W_{ON}, W_{OFF}: updated typical value Table 9: Current sense ($8\text{ V} < V_{CC} < 18\text{ V}$) – I_{OL}: added new row – $K_1, dK_1/K_1$: changed V_{SENSE} value (from 0.5 V to 4 V) for test conditions – K_0, K_1, K_2, K_3: added $V_{DE} = 5\text{ V}$ for test conditions – $dK_0/K_0, dK_1/K_1, dK_2/K_2, dK_3/K_3$: replaced $V_{CSD} = 0\text{ V}$ with $V_{DE} = 5\text{ V}$ for test conditions – K_0, K_1, K_2, K_3: updated minimum, typical and maximum values – $dK_0/K_0, dK_1/K_1, dK_2/K_2, dK_3/K_3$: updated minimum and maximum values – I_{SENSE0}: replaced $V_{CSD} = 5\text{ V}$ with $V_{DE} = 0\text{ V}$ (first row), replaced $V_{CSD} = 0\text{ V}$ with $V_{DE} = 5\text{ V}$, added $I_{OUT} = 0\text{ A}$, added $V_{SENSE} = 0\text{ V}$ (second row), replaced $V_{CSD} = 5\text{ V}$ with $V_{DE} = 0\text{ V}$ (third row) for test conditions – V_{SENSE}: replaced $V_{CSD} = 0\text{ V}$ with $V_{DE} = 5\text{ V}$, added R_{SENSE} for test conditions – $t_{DSENSE1H}$, $t_{DSENSE1L}$, $t_{DSENSE2H}$, $t_{DSENSE2L}$: changed typ/max values – $\Delta t_{DSENSE2H}$: changed maximum value Table 10: Open-load detection ($8\text{ V} < V_{CC} < 18\text{ V}$, $V_{DE} = 5\text{ V}$) – V_{OL}: updated typical value – t_{d_voh}: updated maximum value Updated Figure 9: I_{OUT}/I_{SENSE} vs I_{OUT} Updated Figure 10: Maximum current sense ratio drift vs load current</p>

Table 18. Document revision history (continued)

Date	Revision	Changes
13-Sep-2010	2	<p>Changed Figure 11: Normal operation</p> <p>Changed Figure 12: Overload or short to GND</p> <p>Changed Figure 13: Intermittent overload</p> <p>Changed Figure 14: OFF-state open load with external circuitry</p> <p>Changed Figure 15: Short to V_{CC}</p> <p>Updated Chapter 4: Package and PCB thermal data</p> <p>Updated Chapter 5.1: ECOPACK® packages</p>
29-Sep-2010	3	<p>Table 3: Absolute maximum ratings:</p> <ul style="list-style-type: none"> – I_{OUT}: updated value – V_{CCPK}: updated parameter <p>Table 9: Current sense (8 V < V_{CC} < 18 V):</p> <ul style="list-style-type: none"> – K₀, K₁, K₂, K₃: updated minimum, typical and maximum values – Δt_{DSENSE2H}: updated test condition <p>Updated Figure 9: I_{OUT}/I_{SENSE} vs I_{OUT}</p>
20-Dec-2010	4	<p>Added Section 3.4: Maximum demagnetization energy (V_{CC} = 13.5 V)</p> <p>Table 3: Absolute maximum ratings:</p> <ul style="list-style-type: none"> – E_{MAX}: updated value <p>Table 8: Protections and diagnostic</p> <ul style="list-style-type: none"> – I_{limH}: updated minimum, typical and maximum values <p>Table 9: Current sense (8 V < V_{CC} < 18 V)</p> <ul style="list-style-type: none"> – K₀, K₁, K₂, K₃: updated minimum, typical and maximum values <p>Updated Figure 9: I_{OUT}/I_{SENSE} vs I_{OUT}</p>
20-Apr-2011	5	Updated Table 17: Device summary
18-May-2012	6	Updated Figure 26: I_{LIMH} vs T_{case}
19-Sep-2013	7	Updated Disclaimer.
25-Oct-2013	8	Updated footnote 2 into the Table 12: Electrical transient requirements (part 1) and Table 13: Electrical transient requirements (part 2) .
18-Mar-2015	9	Updated Section 5.2: PowerSO-10 mechanical data

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