ADVANCE INFORMATION

82420EX PCISET DATA SHEET
82425EX PCI SYSTEM CONTROLLER (PSC) AND 82426EX ISA BRIDGE (IB)

- Host CPU
  - —25–33 MHz Intel486™ and OverDrive™ Processors
  - —L1 Write-Back Support
- Integrated DRAM Controller
  - —1 to 128 MByte Main Memory
  - —70 ns Fast Page Mode DRAM SIMMs Supported
  - —Supports 256 KByte, 1 MByte, and 4 MByte Double and Single Sided SIMMs
  - —Read Page Hit Timing of 3-2-2-2 at 33 MHz
  - —Burst Mode PCI Master Accesses
  - —Decoupled Refresh Reduces DRAM Latency
  - —Five RAS Lines
- Integrated L2 Cache Controller
  - —Write-Back and Write-Through Cache Policies
  - —Direct Mapped Organization
  - —64, 128, 256 or 512 KByte Cache Sizes
  - —Programmable Zero Wait-State L2 Cache Read and Write Accesses
  - —Two Banks Interleaved or a Single Bank Non-Interleaved Operation
  - —No VALID Bit Required
- 25/33 MHz PCI Bus Interface
  - —Two Bus Masters
  - —PCI Auto Configuration Support
- Host/PCI Bridge
  - —Converts Back-to-Back Sequential Memory Writes to PCI Burst Writes
  - —CPU Memory Write Posting to PCI
- PCI Local Bus IDE Interface
  - —Supports Mode 3 Timing
- Programmable Attribute Map for First 1 MByte of Main Memory
- 100% ISA Compatible
  - —Directly Drives 5 ISA Slots
- Two 8237 DMA Controllers
  - —7 DMA Channels
  - —27-bit Addressability
  - —Compatible DMA Transfers
- One 82C54 Timer/Counter
  - —System Timer
  - —Refresh Request
  - —Speaker Tone
- Two 82C59 Interrupt Controllers
  - —14 Interrupts
  - —Edge/Level Sense is Programmable per Channel
  - —PCI Interrupt Steering for Plug and Play Compatibility
- X-Bus Peripheral Support
  - —RTC, KBC, BIOS Chip Selects
  - —Control for Lower X-Bus Transceiver
  - —Integrates Mouse Interrupt
  - —Coprocessor Error Reporting
- Non-Maskable Interrupts (NMI)
  - —PCI System Errors
  - —Main Memory Parity Errors
  - —ISA Parity Errors
- System Power Management (Intel SMM Support)
  - —Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#
  - —Programmable CPU Clock Control
  - —Fast On/Off Mode
- Generates System Clocks
- 160-Pin QFP Package for IB
- 208-Pin QFP Package for PSC

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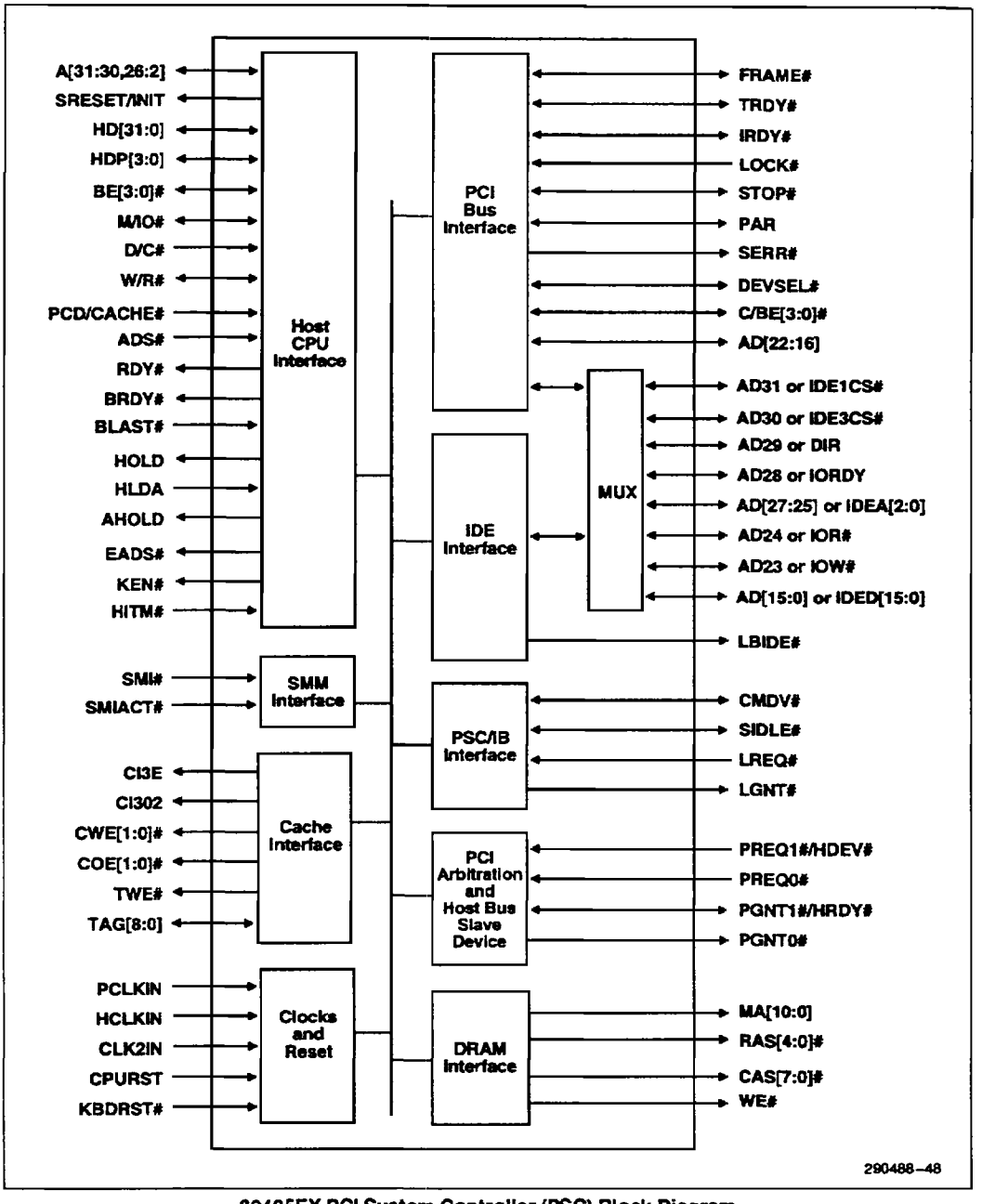
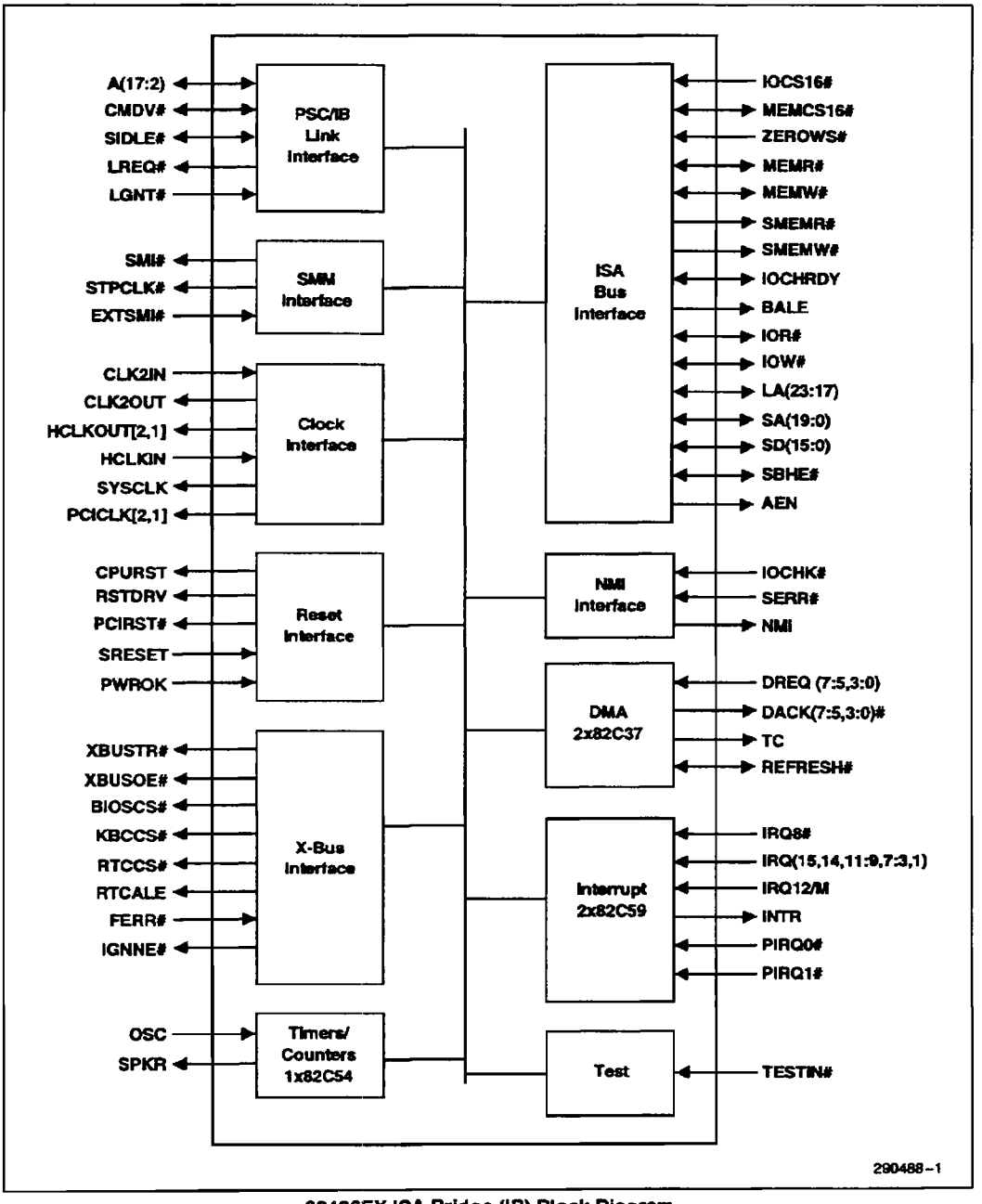
The 82420EX PCIset is the foundation for the **Value Flexible Motherboard** solution for entry-level Intel486™ processor-based PCI systems. The Value Flexible Motherboard solution, including 82420EX, Intel486 processor, 82091AA Advanced Integrated Peripherals, 82C42 Keyboard Controller, Flash BIOS, and Plug & Play software, drives PCI into the mainstream. The 82420EX PCIset is a highly integrated solution enabling low cost, small form factor motherboard designs. All Intel486 processors and upgrades are supported, including L1 write-back and Intel SMM power management. PCI Local Bus IDE is incorporated for higher performance IDE at no additional cost.

The 82420EX was designed from the ground up for PCI performance. It consists of two components—the 82425EX PCI System Controller (PSC) and the 82426EX ISA Bridge (IB). The PSC integrates the L2 cache controller and the DRAM controller. The cache controller supports both write-through and write-back cache policies and cache sizes from 64 KBytes to 512 KBytes in an interleaved or non-interleaved configuration. The DRAM controller interfaces main memory to the Host Bus and the PCI Bus. The PSC supports a two-way interleaved DRAM organization for optimum performance. Up to ten single-sided SIMMs or four double-sided and two single-sided SIMMs provide a maximum of 128 MBytes of main memory. The PSC provides memory write posting to PCI for enhanced CPU-to-PCI memory write performance. In addition, the PSC provides a high performance PCI Local Bus IDE interface.

The IB is the bridge between the ISA Bus and Host Bus, and integrates the common I/O functions found in today's ISA-based PC systems—a seven channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, Intel SMM power management support, and control logic for NMI generation. The IB also provides the decode for external BIOS, real time clock, and keyboard controller. Edge/Level interrupts and interrupt steering are supported for PCI plug and play compatibility. The IB integrates the ISA address and data path, reducing TTL and system cost. In addition, the integration of system clock generation logic eliminates the need for external host and PCI clock drivers.



82425EX PCI System Controller (PSC) Block Diagram



82426EX ISA Bridge (IB) Block Diagram