MC74AC175, MC74ACT175

Quad D Flip–Flop With Master Reset

The MC74AC/ACT175 is a high–speed quad D flip–flop. The device is useful for general flip–flop requirements where clock and clear inputs are common. The information on the D inputs is transferred to storage during the LOW–to–HIGH clock transition. The device has a Master Reset to simultaneously clear all flip–flops, when $\overline{MR}$ is low.

The MC74AC/ACT175 consists of four edge–triggered D flip–flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip–flops. Each D input's state is transferred to the corresponding flip–flop's output following the LOW–to–HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The MC74AC/ACT175 is useful for applications where the Clock and Master Reset are common to all storage elements.

- Outputs Source/Sink 24 mA
- ′ACT175 Has TTL Compatible Inputs

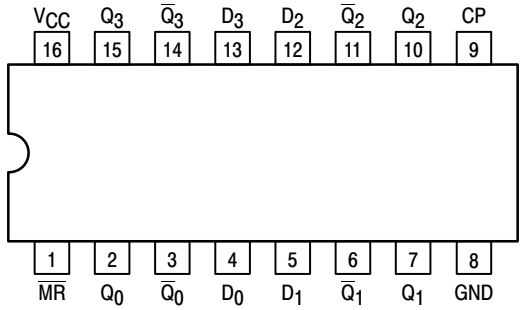

Figure 1. Pinout: 16–Lead Packages
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
$D_0 – D_3$	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
$Q_0 – Q_3$	Outputs
$\overline{Q}_0 – \overline{Q}_3$	Outputs

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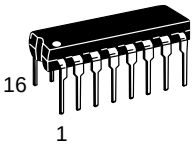
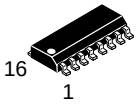
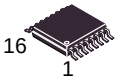


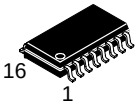
DIP–16
N SUFFIX
CASE 648



SO–16
D SUFFIX
CASE 751B



TSSOP–16
DT SUFFIX
CASE 948F



EIAJ–16
M SUFFIX
CASE 966

ORDERING INFORMATION

Device	Package	Shipping
MC74AC175N	PDIP–16	25 Units/Rail
MC74ACT175N	PDIP–16	25 Units/Rail
MC74AC175D	SOIC–16	48 Units/Rail
MC74ACT175D	SOIC–16	48 Units/Rail
MC74AC175DR2	SOIC–16	2500 Tape & Reel
MC74ACT175DR2	SOIC–16	2500 Tape & Reel
MC74AC175DT	TSSOP–16	96 Units/Rail
MC74ACT175DT	TSSOP–16	96 Units/Rail
MC74AC175DTR2	TSSOP–16	2500 Tape & Reel
MC74ACT175DTR2	TSSOP–16	2500 Tape & Reel
MC74AC175M	EIAJ–16	50 Units/Rail

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 176 of this data sheet.

TRUTH TABLE

Inputs			Outputs	
$\overline{MR}$	CP	D	Qn	$\overline{Qn}$
L	X	X	L	H
H	⎍	H	H	L
H	⎍	L	L	H
H	L	X	Qn	$\overline{Qn}$

NOTE: H = HIGH Voltage Level,
L = LOW Voltage Level
X = Immaterial
⎍ = LOW–to–HIGH Transition of Clock

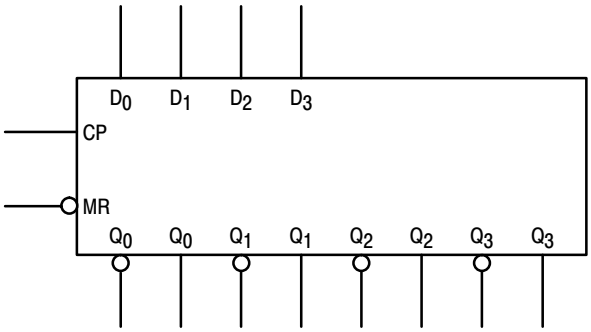
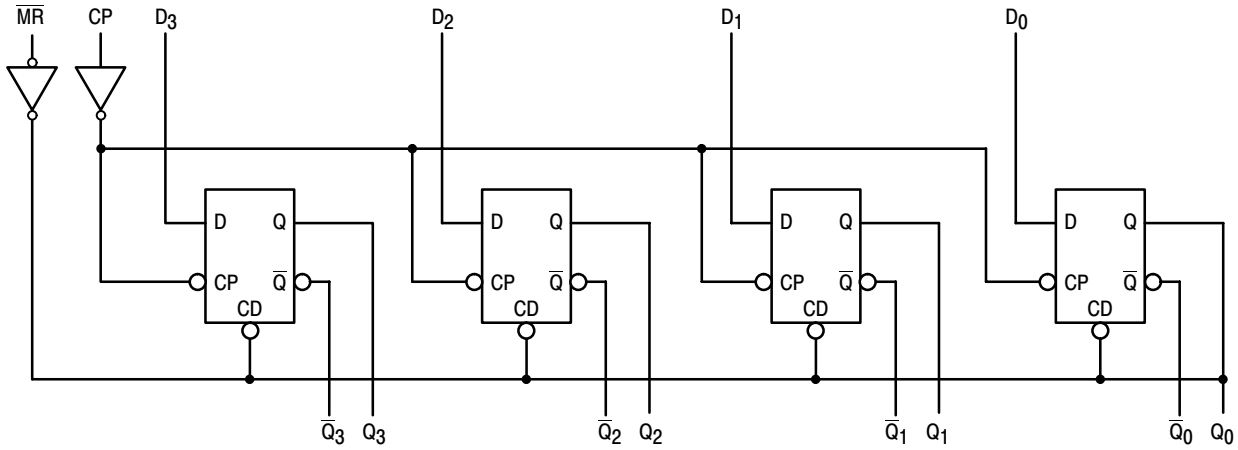


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Min	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – HIGH		–	–	–24	mA
I_{OL}	Output Current – LOW		–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = – 50 μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} – 12 mA I_{OH} – 24 mA – 24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OH} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

DC CHARACTERISTICS (continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = –40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	149 187	– –	– –	139 187	– –	MHz	3–3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0	2.0 1.5	– –	12.0 9.0	2.0 1.0	13.5 9.5	ns	3–6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0	2.5 1.5	– –	13.0 9.5	2.0 1.5	14.5 10.5	ns	3–6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	12.5 9.0	2.5 1.5	13.5 10.0	ns	3–6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	3.0 2.0	– –	11.0 8.5	2.5 1.5	12.5 9.0	ns	3–6

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = –40°C to +85°C, C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set–up Time, HIGH or LOW D_n to CP	3.3 5.0	– –	4.5 3.0	4.5 3.0	ns	3–9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	– –	1.0 1.0	1.0 1.0	ns	3–9
t_w	$\overline{MR}$ Pulse Width Low	3.3 5.0	– –	4.5 3.5	4.5 3.5	ns	3–6
t_w	CP Pulse Width	3.3 5.0	– –	4.5 3.5	5.0 3.5	ns	3–6
t_{rec}	Recovery TIme $\overline{MR}$ to CP	3.3 5.0	– –	0 0	0 0	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT		74ACT	Unit	Conditions
			T_A = +25°C		T_A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = – 50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} – 24 mA I_{OH} – 24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} 24 mA I_{OH} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V_{CC}* (V)	74ACT			74ACT		Unit	Fig. No.
			T_A = +25°C C_L = 50 pF			T_A = –40°C to +85°C C_L = 50 pF			
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	175	–	–	145	–	MHz	3–3
t_{PLH}	Propagation Delay CP to Q_n	5.0	2.0	–	10.0	1.5	11.0	ns	3–6
t_{PHL}	Propagation Delay CP to Q_n	5.0	2.0	–	11.0	1.5	12.0	ns	3–6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	5.0	2.0	–	9.5	1.5	10.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT		74ACT	Unit	Fig. No.
			T_A = +25°C C_L = 50 pF		T_A = –40°C to +85°C C_L = 50 pF		
			Typ	Guaranteed Minimum			
t_s (H) (L)	Set–up Time, HIGH or LOW D_n to CP	5.0	–	2.0 2.5	2.0 2.5	ns	3–9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	–	1.0	1.0	ns	3–9
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	–	3.0	4.0	ns	3–6
t_w	CP Pulse Width, HIGH or LOW	5.0	–	3.0	3.5	ns	3–6
t_{rec}	Recovery TIme $\overline{MR}$ to CP	5.0	–	0	0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

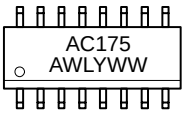
CAPACITANCE

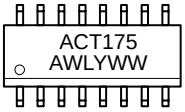
Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0 V

MARKING DIAGRAMS

DIP–16

SO–16





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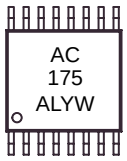
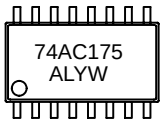


EIAJ–16



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week