NST3946DXV6T1, NST3946DXV6T5

Dual General Purpose Transistor

The NST3946DXV6T1 device is a spin-off of our popular SOT-23/SOT-323 three-leaded device. It is designed for general purpose amplifier applications and is housed in the SOT-563 six-leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low-power surface mount applications where board space is at a premium.

- h_{FE}, 100-300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Lead-Free Solder Plating

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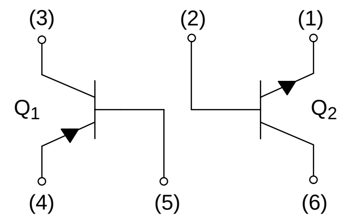
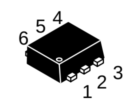


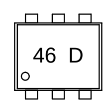
NST3946DXV6T1*

*Q1 PNP
Q2 NPN



SOT-563
CASE 463A
PLASTIC

MARKING DIAGRAM



46 = Specific Device Code
D = Date Code

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (NPN) (PNP)	V_{CEO}	40 -40	Vdc
Collector-Base Voltage (NPN) (PNP)	V_{CBO}	60 -40	Vdc
Emitter-Base Voltage (NPN) (PNP)	V_{EBO}	6.0 -5.0	Vdc
Collector Current - Continuous (NPN) (PNP)	I_C	200 -200	mAdc
Electrostatic Discharge	ESD	HBM>16000, MM>2000	V

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25°C$ Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation $T_A = 25°C$ Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/°C

1. FR-4 @ Minimum Pad

ORDERING INFORMATION

Device	Package	Shipping
NST3946DXV6T1	SOT-563	4 mm pitch 4000/Tape & Reel
NST3946DXV6T5	SOT-563	2 mm pitch 8000/Tape & Reel

Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector - Emitter Breakdown Voltage (Note 2)		$V_{(BR)CEO}$			Vdc
(I_C = 1.0 mAdc, I_B = 0)	(NPN)		40	-	
(I_C = -1.0 mAdc, I_B = 0)	(PNP)		-40	-	
Collector - Base Breakdown Voltage		$V_{(BR)CBO}$			Vdc
(I_C = 10 μAdc, I_E = 0)	(NPN)		60	-	
(I_C = -10 μAdc, I_E = 0)	(PNP)		-40	-	
Emitter - Base Breakdown Voltage		$V_{(BR)EBO}$			Vdc
(I_E = 10 μAdc, I_C = 0)	(NPN)		6.0	-	
(I_E = -10 μAdc, I_C = 0)	(PNP)		-5.0	-	
Base Cutoff Current		I_{BL}			nAdc
(V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	(NPN)		-	50	
(V_{CE} = -30 Vdc, V_{EB} = -3.0 Vdc)	(PNP)		-	-50	
Collector Cutoff Current		I_{CEX}			nAdc
(V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	(NPN)		-	50	
(V_{CE} = -30 Vdc, V_{EB} = -3.0 Vdc)	(PNP)		-	-50	
ON CHARACTERISTICS (Note 2)					
DC Current Gain		h_{FE}			-
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	(NPN)		40	-	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)			70	-	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			60	-	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			30	-	
(I_C = -0.1 mAdc, V_{CE} = -1.0 Vdc)	(PNP)		60	-	
(I_C = -1.0 mAdc, V_{CE} = -1.0 Vdc)			80	-	
(I_C = -10 mAdc, V_{CE} = -1.0 Vdc)			100	300	
(I_C = -50 mAdc, V_{CE} = -1.0 Vdc)			60	-	
(I_C = -100 mAdc, V_{CE} = -1.0 Vdc)			30	-	
Collector - Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	(NPN)		-	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			-	0.3	
(I_C = -10 mAdc, I_B = -1.0 mAdc)	(PNP)		-	-0.25	
(I_C = -50 mAdc, I_B = -5.0 mAdc)			-	-0.4	
Base - Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	(NPN)		0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			-	0.95	
(I_C = -10 mAdc, I_B = -1.0 mAdc)	(PNP)		-0.65	-0.85	
(I_C = -50 mAdc, I_B = -5.0 mAdc)			-	-0.95	

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

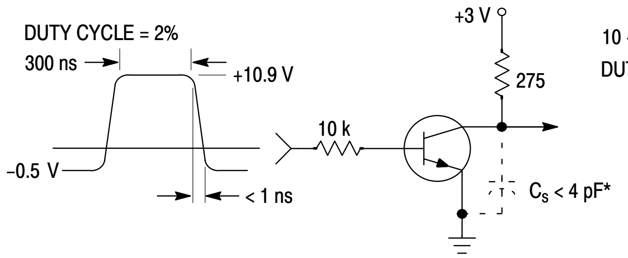
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

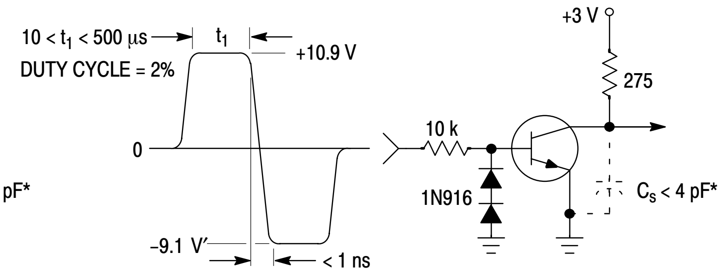
Characteristic		Symbol	Min	Max	Unit
SMALL- SIGNAL CHARACTERISTICS					
Current- Gain - Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	(NPN)		300	-	
(I_C = -10 mAdc, V_{CE} = -20 Vdc, f = 100 MHz)	(PNP)		250	-	
Output Capacitance		C_{obo}			pF
(V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	(NPN)		-	4.0	
(V_{CB} = -5.0 Vdc, I_E = 0, f = 1.0 MHz)	(PNP)		-	4.5	
Input Capacitance		C_{ibo}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	(NPN)		-	8.0	
(V_{EB} = -0.5 Vdc, I_C = 0, f = 1.0 MHz)	(PNP)		-	10.0	
Input Impedance		h_{ie}			k Ω
(V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	(NPN)		1.0	10	
(V_{CE} = -10 Vdc, I_C = -1.0 mAdc, f = 1.0 kHz)	(PNP)		2.0	12	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	(NPN)		0.5	8.0	
(V_{CE} = -10 Vdc, I_C = -1.0 mAdc, f = 1.0 kHz)	(PNP)		0.1	10	
Small- Signal Current Gain		h_{fe}			-
(V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	(NPN)		100	400	
(V_{CE} = -10 Vdc, I_C = -1.0 mAdc, f = 1.0 kHz)	(PNP)		100	400	
Output Admittance		h_{oe}			μmhos
(V_{CE} = 10 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	(NPN)		1.0	40	
(V_{CE} = -10 Vdc, I_C = -1.0 mAdc, f = 1.0 kHz)	(PNP)		3.0	60	
Noise Figure		NF			dB
(V_{CE} = 5.0 Vdc, I_C = 100 μAdc, R_S = 1.0 k Ω, f = 1.0 kHz)	(NPN)		-	5.0	
(V_{CE} = -5.0 Vdc, I_C = -100 μAdc, R_S = 1.0 k Ω, f = 1.0 kHz)	(PNP)		-	4.0	

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = -0.5 Vdc)	(NPN)	t_d	-	35	ns
	(V_{CC} = -3.0 Vdc, V_{BE} = 0.5 Vdc)	(PNP)		-	35	
Rise Time	(I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	(NPN)	t_r	-	35	
	(I_C = -10 mAdc, I_{B1} = -1.0 mAdc)	(PNP)		-	35	
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc)	(NPN)	t_s	-	200	ns
	(V_{CC} = -3.0 Vdc, I_C = -10 mAdc)	(PNP)		-	225	
Fall Time	(I_{B1} = I_{B2} = 1.0 mAdc)	(NPN)	t_f	-	50	
	(I_{B1} = I_{B2} = -1.0 mAdc)	(PNP)		-	75	

(NPN)





* Total shunt capacitance of test jig and connectors

Figure 1. Delay and Rise Time Equivalent Test Circuit

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

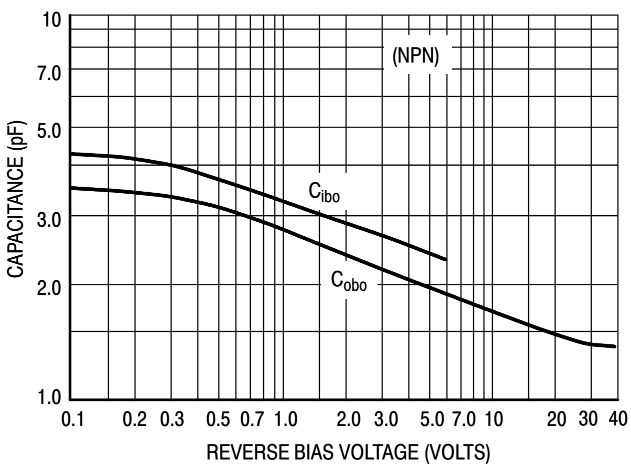


Figure 3. Capacitance

(NPN)

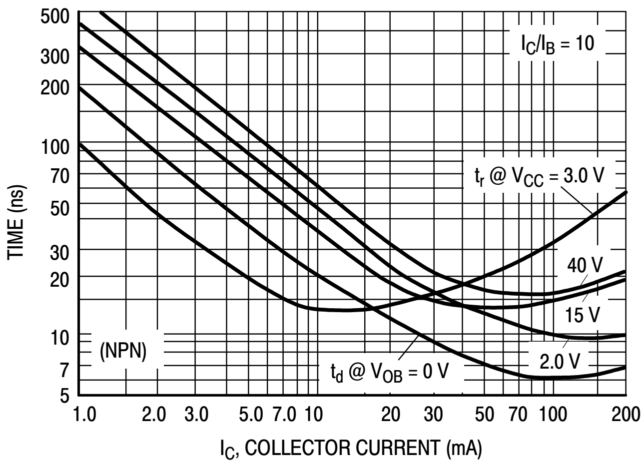


Figure 4. Turn- On Time

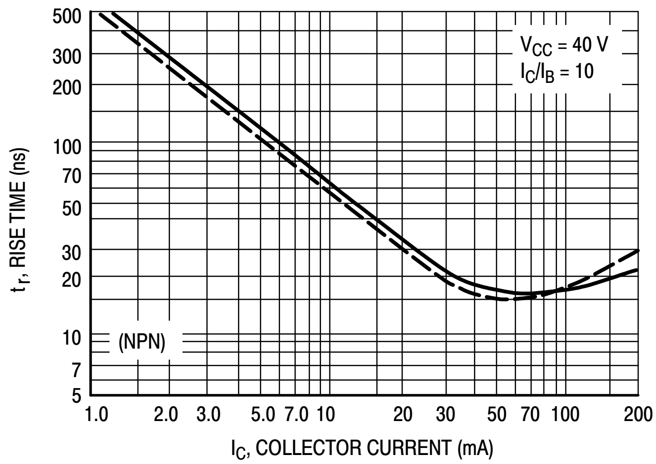


Figure 5. Rise Time

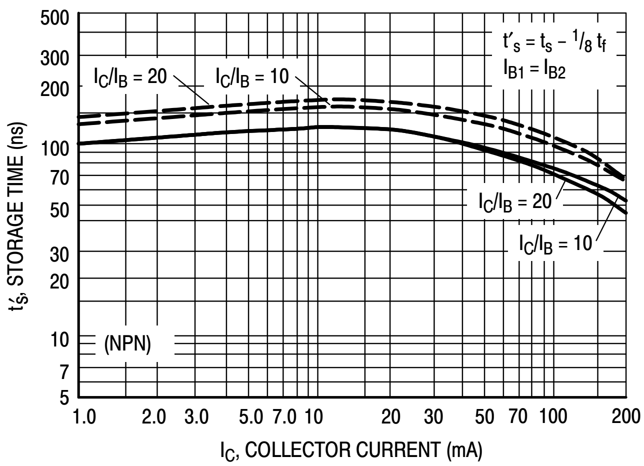


Figure 6. Storage Time

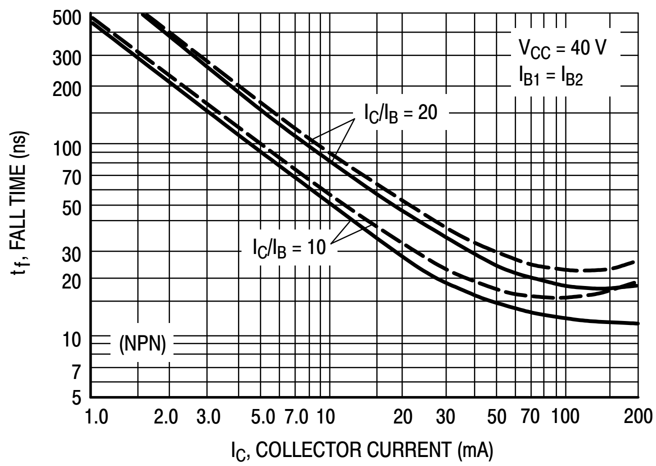


Figure 7. Fall Time

TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS

(V_{CE} = 5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

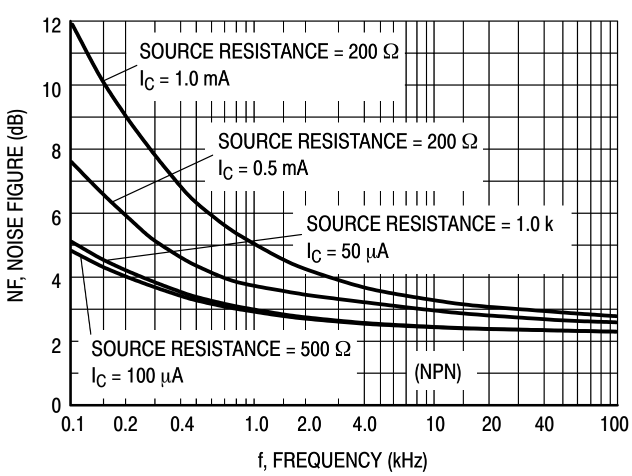


Figure 8. Noise Figure

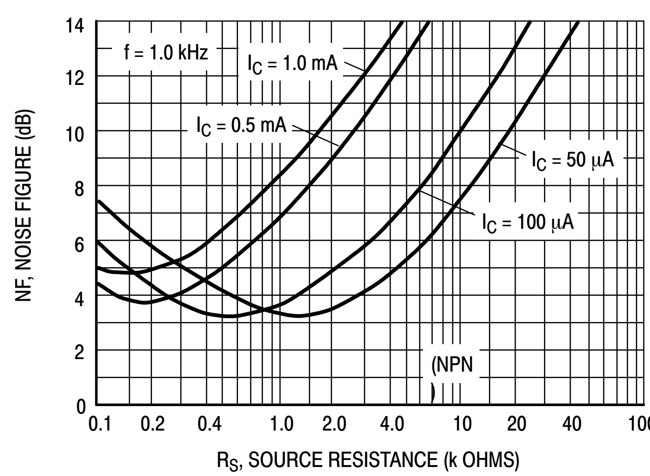


Figure 9. Noise Figure

(NPN)

h PARAMETERS

(V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C)

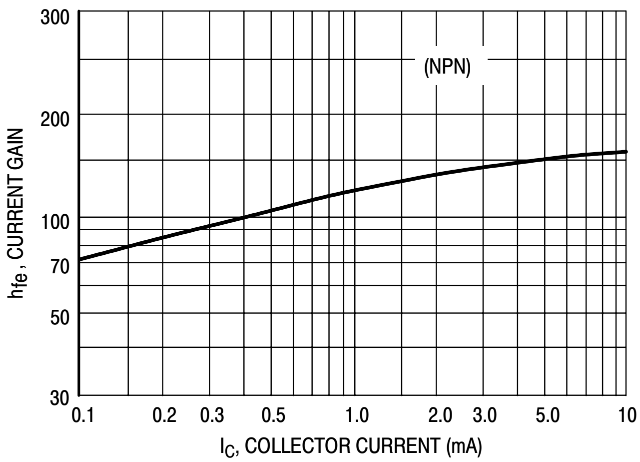


Figure 10. Current Gain

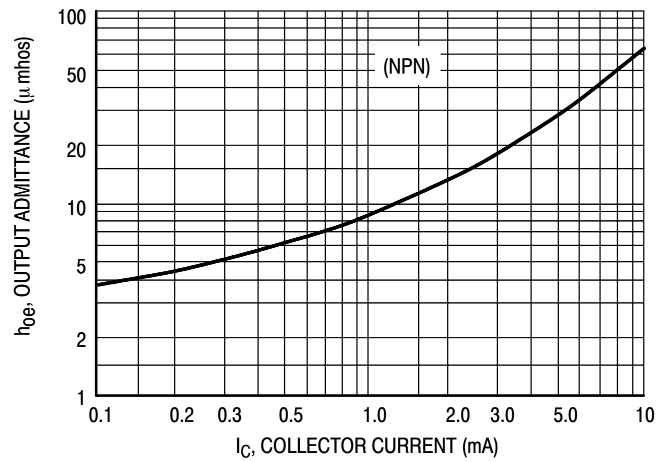


Figure 11. Output Admittance

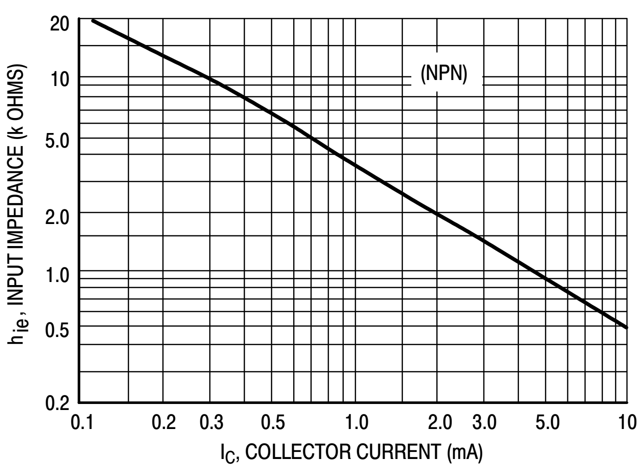


Figure 12. Input Impedance

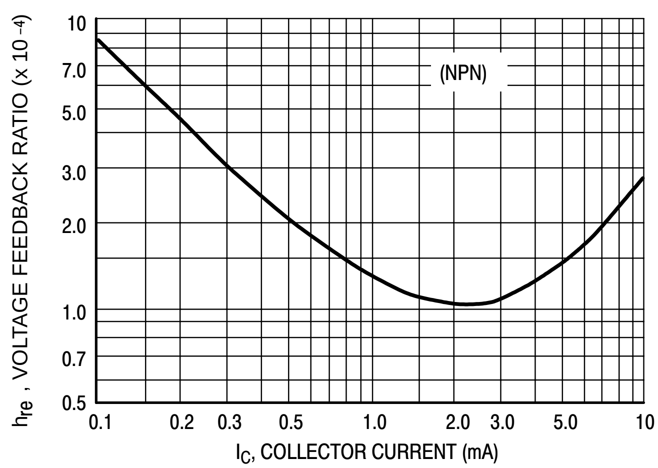


Figure 13. Voltage Feedback Ratio

(NPN)

TYPICAL STATIC CHARACTERISTICS

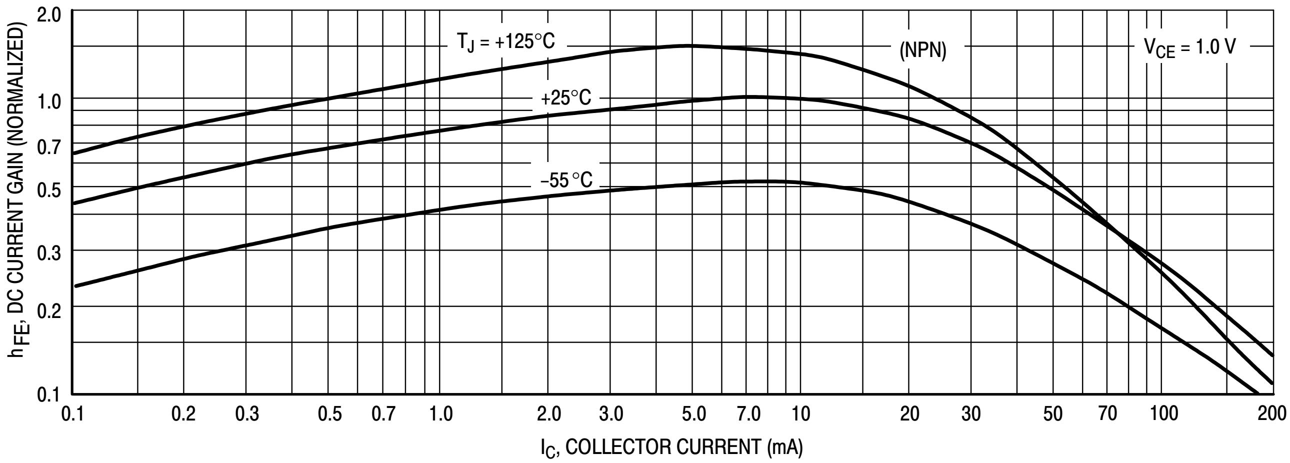


Figure 14. DC Current Gain

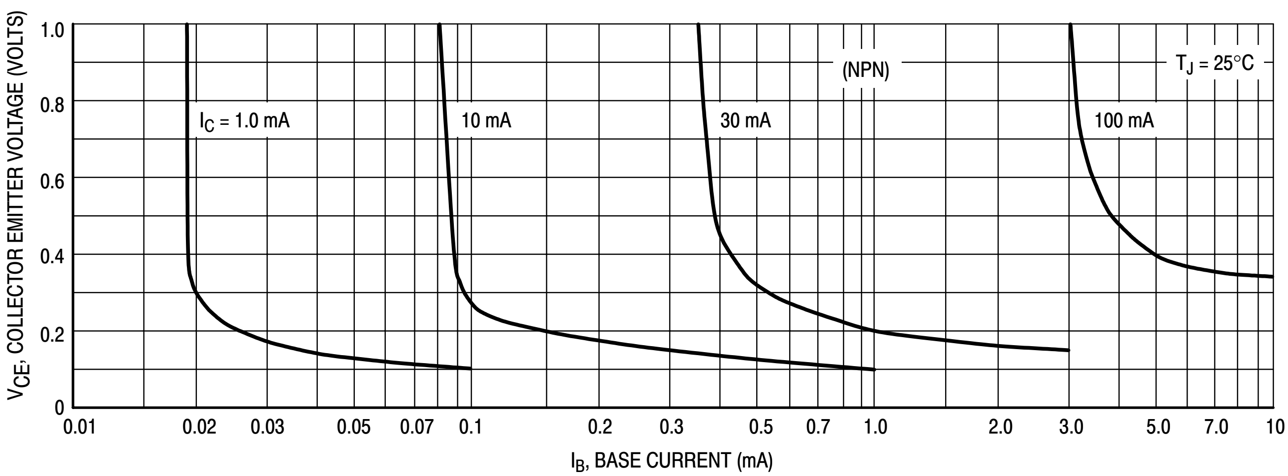


Figure 15. Collector Saturation Region

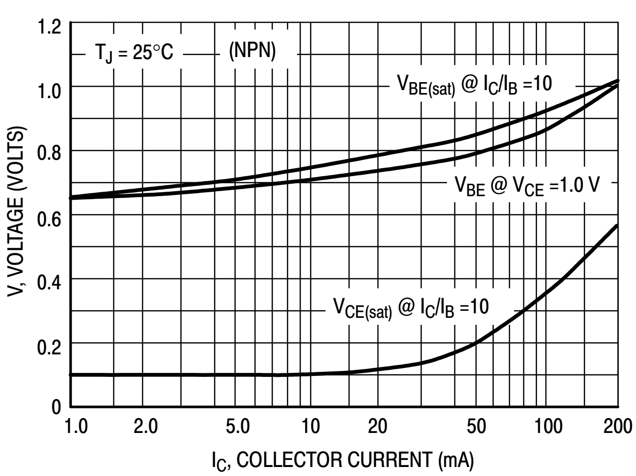


Figure 16. “ON” Voltages

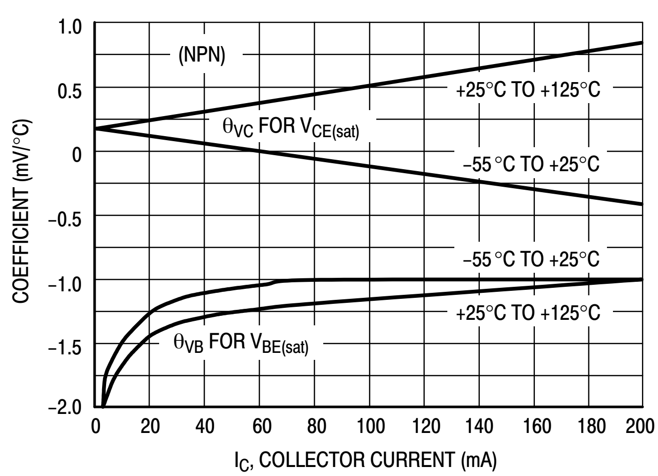
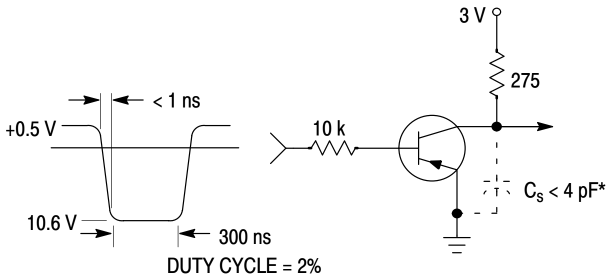
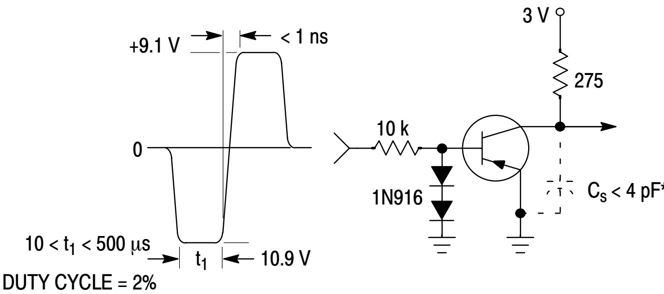


Figure 17. Temperature Coefficients

(PNP)





* Total shunt capacitance of test jig and connectors

Figure 18. Delay and Rise Time Equivalent Test Circuit

Figure 19. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

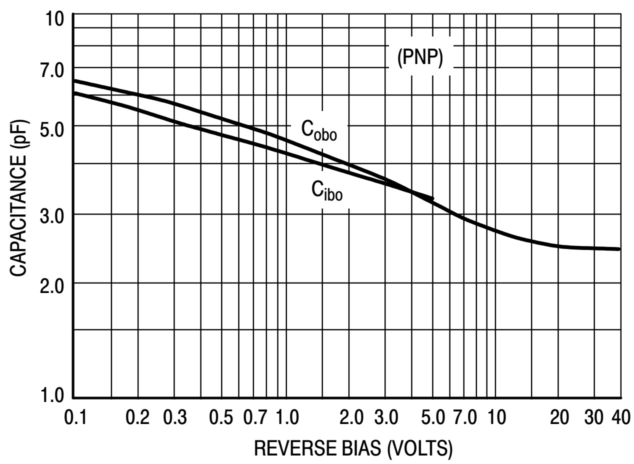


Figure 20. Capacitance

T_J = 25°C
T_J = 125°C

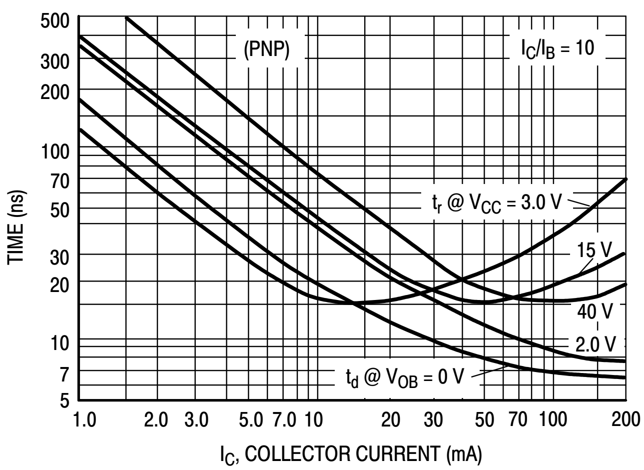


Figure 21. Turn‐On Time

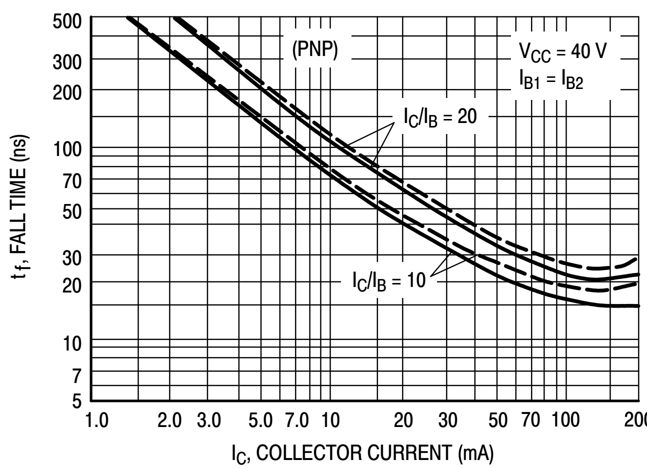


Figure 22. Fall Time

(PNP)

TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS

(V_{CE} = -5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

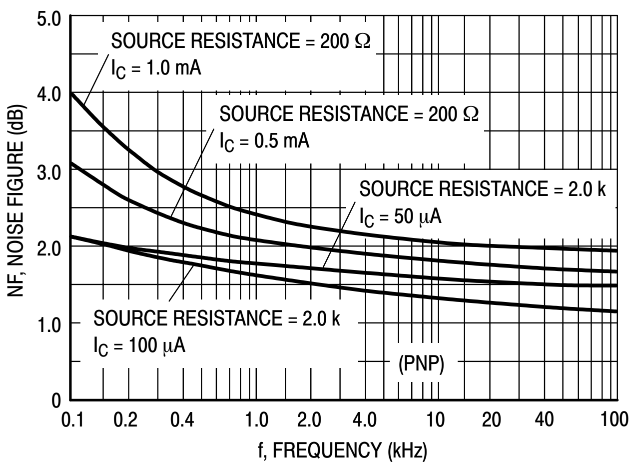


Figure 23.

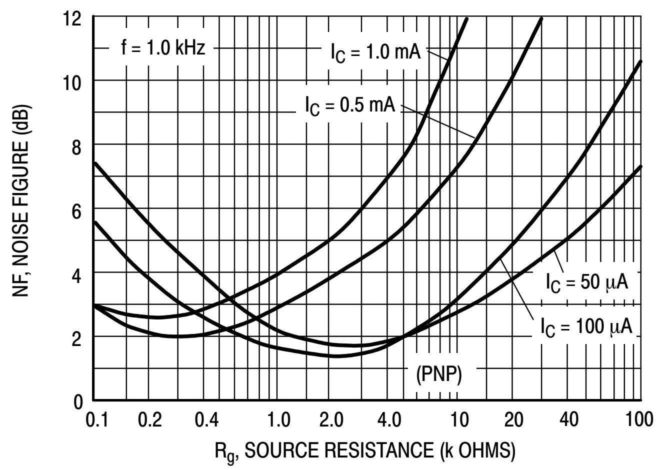


Figure 24.

h PARAMETERS

(V_{CE} = -10 Vdc, f = 1.0 kHz, T_A = 25°C)

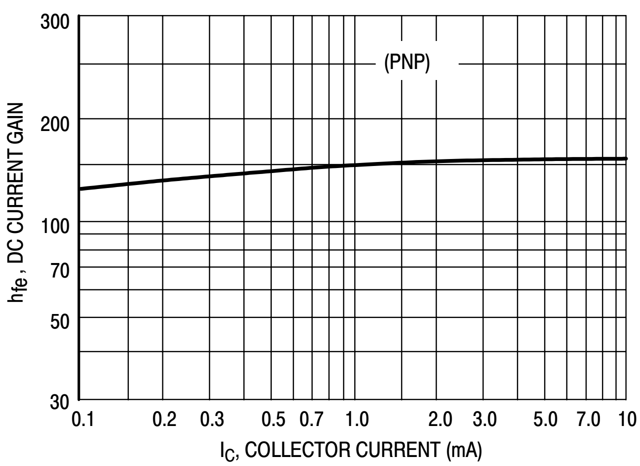


Figure 25. Current Gain

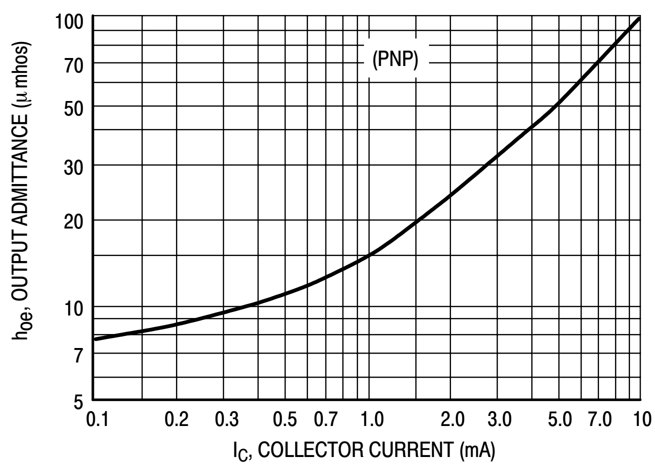


Figure 26. Output Admittance

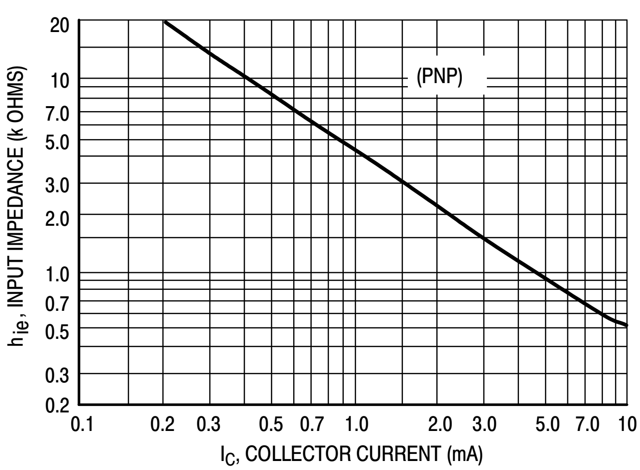


Figure 27. Input Impedance

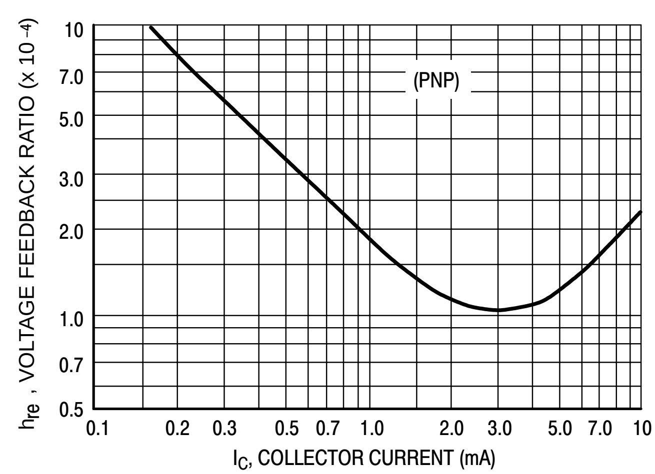


Figure 28. Voltage Feedback Ratio

(PNP)

TYPICAL STATIC CHARACTERISTICS

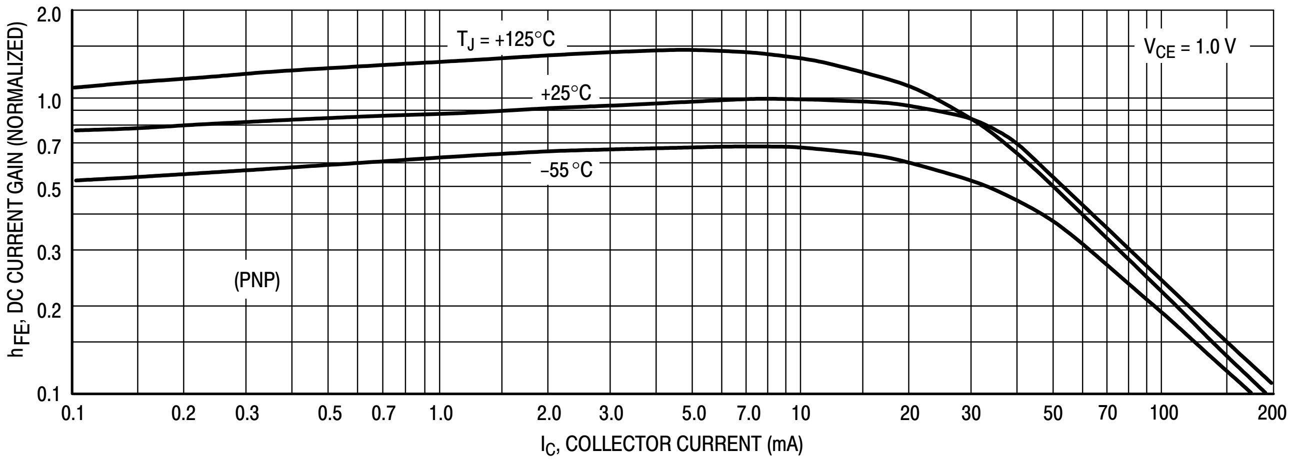


Figure 29. DC Current Gain

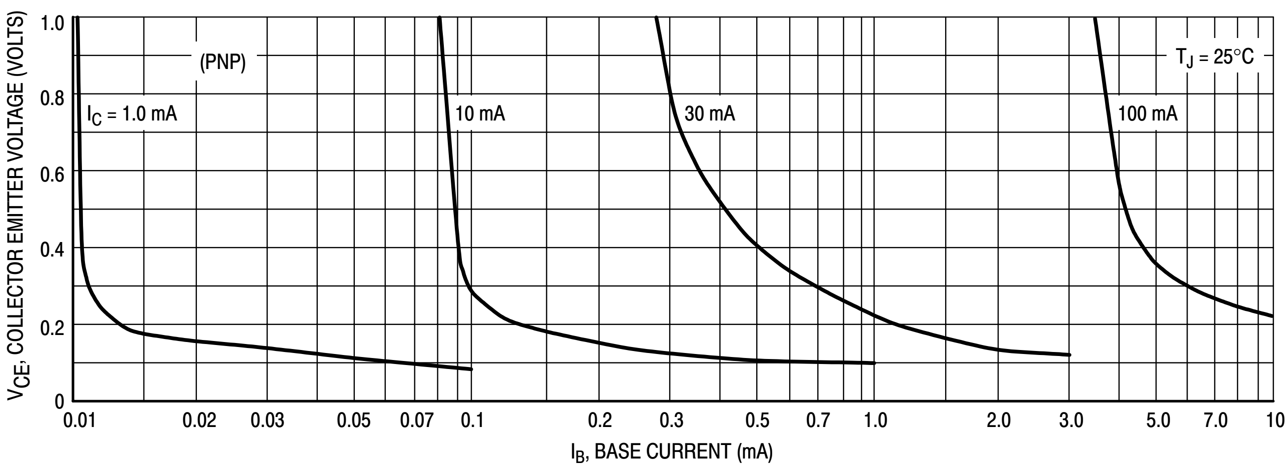


Figure 30. Collector Saturation Region

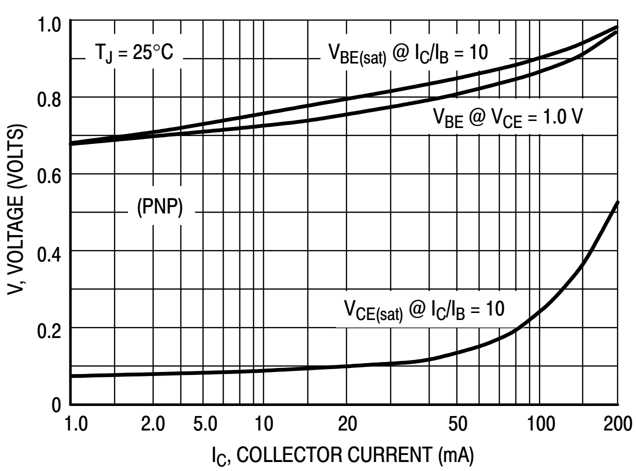


Figure 31. “ON” Voltages

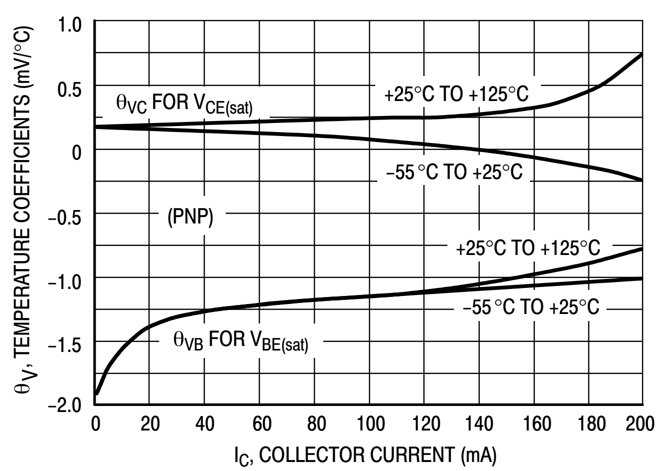
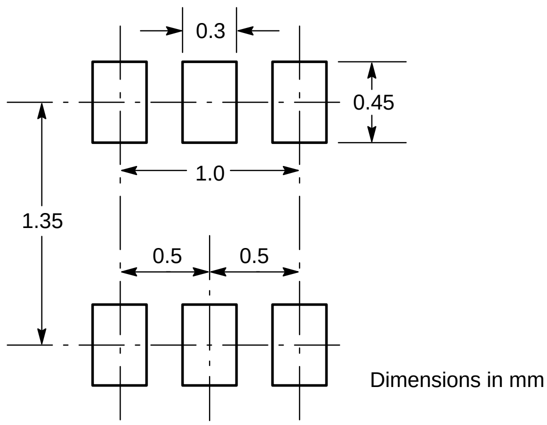


Figure 32. Temperature Coefficients

INFORMATION FOR USING THE SOT-563 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-563

SOT-563 POWER DISSIPATION

The power dissipation of the SOT-563 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT-563 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-563 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-563 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

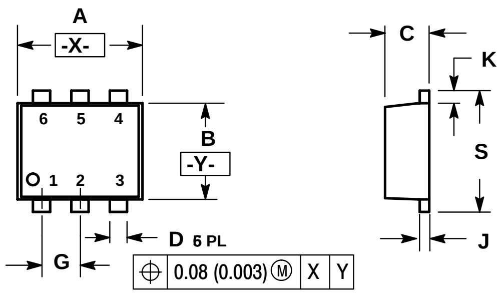
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

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