

DESCRIPTION

The EV2760-VT-00A evaluation board is designed to demonstrate the capabilities of the MP2760, a buck-boost, narrow voltage DC (NVDC) charger IC designed for applications with 1-cell to 4-cell series battery packs.

The MP2760 can accept a wide 4V to 22V operating input voltage (V_{IN}) range to charge the battery and power the load connected on SYS. The device also supplies a wide 3V to 21V voltage at the IN pin in source mode, which

is compliant with USB powered device (PD) specifications.

When input power is present, the EV2760-VT-00A charges the battery with a maximum 6A charge current. It can also supply voltage at the input when source mode is enabled. In source mode, the output current (I_{OUT}) is limited to 6A.

The MP2760 is available in a TQFN-30 (4mmx5mm) package.

PERFORMANCE SUMMARY (1)

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V _{IN}) range		4V to 22V
Battery charge regulation voltage (VBATT_REG)	2 cells	8.4V (I ² C-configurable)
Fast charge current (Icc)	V _{IN} = 9V to 22V	2A (I ² C-configurable)
System voltage (Vsys_min_reg)	2 cells	6.5V (I ² C-configurable)
Output voltage in source mode (V _{IN_SRC}) range		3V to 21V
Output voltage in source mode (VIN_SRC)		4.98V (I ² C-configurable)
Output current limit in source mode (IIN_SRC)		2A (I ² C-configurable)
Charge typical efficiency	V _{IN} = 20V, V _{BATT} = 8V, I _{CC} = 5A	93.49%
Charge peak efficiency	V _{IN} = 12V, V _{BATT} = 8V, I _{CC} = 3A	96%
Source mode typical efficiency	VBATT = 7.4V, VIN_SRC = 20V, IIN_SRC = 1.5A	93.5%
Source mode peak efficiency	VBATT = 8.4V, VIN_SRC = 12V, IIN_SRC = 1.5A	96.37%
Switching frequency (fsw)		600kHz (I ² C-configurable)

Note:

1) Refer to the MP2760 datasheet for details.

MPL Optimized Performance with MPS Inductor MPL-AL5030-1R5



EVALUATION BOARD



LxWxH (8.9cmx8.9cmx0.8cm)

Board Number	MPS IC Number				
EV2760-VT-00A	MP2760GVT-0000				



QUICK START GUIDE

The EV2760-VT-00A evaluation board is designed for the MP2760, a buck-boost NVDC charger, when the device is used to charge a 2-cell battery. The board layout accommodates most commonly used resistors and capacitors. The board's default function is preset for charger mode, and the full charge voltage is preset to 8.4V. In charge mode, the MP2760 can work automatically in buck or buck-boost mode according to the input and battery voltages.

Follow the steps below to prepare the evaluation board.

- 1. Ensure that the computer has at least one USB port and a USB cable. The MP2760 evaluation software must be properly installed.
- 2. Connect the USB-to-I²C communication kit (EVKT-USBI2C-02) (see Figure 1).



Figure 1: USB-to-I²C Communication Kit

3. To enable the software, double-click on the "MP2651 Evaluation Kit" .exe file to run the MP2651 evaluation software. The software supports Windows 7 and Windows 10 operating systems.

The MP2760 evaluation kit.exe file can be downloaded from the MPS website.

Original Test Set-Up for the MP2760

- 1. Connect the battery terminals to:
 - a. Positive (+): VBATT
 - b. Negative (-) GND
- 2. If using a battery simulator, preset the battery voltage between 0V and 8.4V, then turn off the battery voltage.
- 3. Connect the battery simulator output to the VBATT and GND pins, respectively.
- 4. Turn on the battery simulator before starting the test.
- 5. For charge mode testing, connect the input terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND

Figure 2 on page 4 shows the charge mode testing set-up.





Figure 2: Charge Mode Test Set-Up

- 6. Connect the system load terminals to:
 - a. Positive (+): VSYS
 - b. Negative (-): GND
- 7. For source mode testing, connect the load terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND

Table 1 shows the jumper connection settings.

Table 1: Jumper Connections

Jack	Description	Default Setting
	To select the pull-voltage, pull JP1 up to VCC or an external	Pullup IP1 to VCC
JEIV	power source.	
	For the TS/IMON pin's connection, connect TS/IMON to different	Open
JFZ	external circuitry depending on the TS/IMON selection.	Open

Notes:

- 2) If EXT is selected, add an external power source (e.g. 3.3V) at EXT to AGND. If VCC is selected, no other action is required.
- 3) TS/IMON has different external circuits. Connect TS/IMON to the corresponding circuit using the I²C.
- 8. Launch the MP2760 evaluation software (see Figure 3).



MP276	i 0									C	MONITO	R	R/W		
BASIC CON	IFIG	REGISTER N	۱۸P		DEBUG						💿 Status			🛞 Fault	
											MD_STAT	10-Standby 0-Not Power		BFET_OC_FAULT TS_FAULT	0-Nom
General Setting	-		-		5 Source Mo	le Param	eter Setting				PG_SIAI	Good		VIN_SRC_OV	0-Norr
PWM Frequency	0	600		kHz	SRC Mode Enal		0-Disable Di	ischarge	-		BATTMISS STAT	0-Normal		VIN_SRC_UV	0-Norn
Battery Cell Count	0	2		Cell	SRC Output Vol	age n	4980		v mV		Address Setting	0-Single port		VADP_OV	0-Norn
Charge Enable	0	1-Charge Enable	•		SRC Ouput Cur Limit	ent O	2000		▼ mA		CHG_STAT	000-No Charging		VSYS_OV VSYS_UV	0-Norr 0-Norr
DC/DC Enable	0	1-Enable	-		A NTC JEITA	etting			$ \rightarrow $		VIN_MIN_STAT	0-Not in input		VBATT_OV	0-Nom
Safety Timer Enable	0	1-Enable	•		Hot Threshold	0	10-23.0%	;(60°C)	•		IIN_LIM_STAT	0-Not in input current limit		WTD_EXP	0-Norn 0-Norn
Charge Paramet	ers			=	Warm Threshol	0	01-32.6%	;(45°C)	•		TJREG_STAT	0-Not in thems	al	THERM SHDN	0-Norm
Rattery Full Vieltage		8400		1 mit	Cool Threshold	0	10-64.8%	;(10°C)	¥		IIN_DPM	6350	mA	NTC_FAULT	000-Nom
Fast Charge Current	0	2000		mA	Cold Threshold	0	01-74.2	%;(0°C)	*		ADC				
Pre-charge Threshold	0	6		v	Warm	men 0	01-VBAT	T_REG	*						
Recharge Threshold	0	200	+	mV	Charge Action	hen 0	10-IC	с	*						
Trickle Charge Current	0	100	-	mA	VBATT_REG Set when Warm/Co	ing O	320		▼ mV	1					
Pre-charge Current	0	400		mA	ICC Setting who	n ()	01-1/4	4 times	-						
Termination Current	0	200	•	mA	Warm/Cool NTC Protection	0	1-Ena	able		-					

Figure 3: MP2760 Evaluation Software

9. Turn on the input voltage (V_{IN}) to charge the battery and power the system load with the default settings.

Modifying Parameters via the GUI

To use MPS's GUI, ensure that all connections are successful, such as the connections between the computer, USB-to-I²C communication kit, and the evaluation board.

Figure 4 shows the MP2760's basic settings.

	'IG	REGISTER N	(AP		DEBUG
General Settin	8				Source Mode Parameter Setting
PWM Frequency	0	600	÷	kHz	SRC Mode Enable 🗿 0-Disable Dischar 👻
Battery Cell Count	0	2	•	Cell	SRC Output Voltage 🕦 4980 👻 mV
Charge Enable	0	1-Charge Enable	٠		SRC Ouput Current 2000 mA
DC/DC Enable	0	1-Enable	٠		
Safety Timer	0	20 hours	•	10	(NTC JEITA Setting
Safety Timer Enable	0	1-Enable	*	R .	
111111					

Figure 4: Basic Settings

Figure 5 on page 6 shows how to configure the general settings. These settings include the pulse-width modulation (PWM) frequency, battery cell count, safety timer, basic controls in charge mode (such as enabling the DC/DC converter), and charge enabling.

Note that the recommended PWM frequency is between 500kHz and 800kHz.



General Setting				
PWM Frequency	0	600	•	kHz
Battery Cell Count		2	•	Cell
Charge Enable	0	1-Charge Enable	•	
DC/DC Enable	0	1-Enable	•	
Safety Timer		20 hours	•	
Safety Timer Enable		1-Enable	•	

Figure 5: General Settings

Figure 6 shows how to configure the charge parameters, including the battery-full voltage, fast charge current, pre-charge threshold, recharge threshold, trickle charge current, pre-charge current, and termination current.

The charge parameters also provide the parameters for power path management, including the input minimum voltage limit and input current limit. All the parameters can be input directly by keyboard.

	11		
Battery Full Voltage 🕥	8400	•	m۷
Fast Charge Current 🕚	2000		mA
Pre-charge Threshold 🕦	6		۷
Recharge Threshold 🕚	200		m١
Trickle Charge	100	•	mA
Pre-charge Current 👩	400		m/
Termination Current 🕥	200	•	mA
Input Minimum Voltage Limit	4560] m\
Input Current Limit	500		mA

Figure 6: Charge Parameters

Figure 7 shows how to configure the negative temperature coefficient (NTC) JEITA settings for battery thermal protection.

Hot Threshold	10-23.0%;(60°C)	•	
Warm Threshold	01-32.6%;(45°C)	*	
Cool Threshold	10-64.8%;(10°C)	•	
Cold Threshold	01-74.2%;(0°C)	*	
Charge Action when Warm	01-VBATT_REG	•	
Charge Action when Cool	10-ICC	•	
VBATT_REG Setting when Warm/Cool	320	•	mV
ICC Setting when Warm/Cool	01-1/4 times	•	
NTC Protection Enable	1-Enable	*	

Figure 7: NTC JEITA Settings

Figure 8 on page 7 shows how to configure the source mode settings. In source mode, the battery supplies power to the IN pin. The discharge parameters include the SRC mode (enabled or disabled), SRC output voltage, and SRC output current limit.



Source Mode Setting			
SRC Mode Enable	0-Disable Discharge	•	
SRC Output Voltage	4980	•	mV
SRC Ouput Current Limit	2000	•	mA

Figure 8: Source Mode Settings

Figure 9 shows the MP2760's configuration settings.

ASIC	CONFIG	REGISTER A	AAP.	DEBUG					
🕤 Gen	eral Setting				Narrow VDC PF	PM Ser	tting	_	_
Input Cur Resistor	rent Sense 🗿	0-10mohm	•	Min Volt	imum System age Threshold	0	6400	•	mV
Battery C	urrent 0	0-10mohm	*	Vtra	ick Per Cell	0	150		mV
O all	212201	-		Virti Enal	ual Diode ble	0	1-Enable	٠	
Char	ge Parameters	Setting		Syst	em OVP enable	0	1-Enable SYS OV	+	
Safety Tir Extension	mer O	1-Extend by 2X	*	Syst	em OVP	0	11-110%	-	
Charge Te	ermination 🕜	1-Enable	-	Syst	em UVP	0	00-75%;	٠	
Input Cur Disable	rent Limit 🕕	1-IIN_LIM Enable	•	0	Watchdog Time	er			
Battery O	VP Enable 🚺	1-Enable BATT O	*	0	Other Protection	ons			
Batt	ery Impedance	Compensation		50	Temperature S	ense			
Mode	e Configuration	1		50	ADC				
SRC	Mode			5					

Figure 9: Configuration Settings

Figure 10 shows how to configure and select the current-sense resistors.

General Setting		
Input Current Sense Resistor	0-10mΩ	-
Battery Current Sense Resistor	0 - 10mΩ	•

Figure 10: Current-Sense Resistor Settings

Figure 11 shows how to configure the charge protection parameters. These parameters include the safety timer extension, as well as options to enable charge termination, the input current limit, and battery over-voltage protection (OVP).

Charge Parameters	Setting
Safety Timer Extension	1-Extend by 2X 💌
Charge Termination 🕦	1-Enable -
Input Current Limit Disable	1-IIN_LIM Enable -
Battery OVP Enable 🕦	1-Enable BATT O' 🔻

Figure 11: Charge Parameters Setting

Figure 12 on page 8 shows how to configure the battery impedance compensation, including the battery impedance and voltage compensation limit.



Batter Impeda	ance Comper	nsation	
Battery Impedance	0	-	mΩ
Voltage			
Compensation	0	-	mV
Limit			

Figure 12: Battery Impedance Compensation

Figure 13 shows how to configure the external MOSFET control. ACGATE can be set to drive the input MOSFET between the ADP pin and the input current-sense resistor. BGATE can be set to control the battery MOSFET between the SYS pin and the battery current-sense resistor.

Mode Configur	ation		
BGATE Driver Enabl	e	1-Enable BGATE	Ŧ
BGATE Force Off	0	0-Not force BGAT	•
ACGATE Force On	0	0-Not force ACGA	•
ACGATE Driver Enable	0	1-Enable ACGAE	•

Figure 13: External MOSFET Configuration

Figure 14 shows how to configure the SRC mode control, which includes the SRC output voltage configuration and protections.

SRC Mode	
SRC Output Voltage Configuration	0-By register bit 💌
SRC Output Voltage Offset	0 - V
Battery Low Voltage Protection Enable	1-Enable 👻
Battery Low Voltage Threshold	6 🗸 V
DC/DC Action when Battery Low Voltage	0-INT 👻
Battery Discharge Current Limit	6400 v mA
Battery Discharge Current Limit Enable	0-Disable 🔻

Figure 14: SRC Mode Configuration

Figure 15 shows how to configure the NVDC power path management (PPM).

Narrow VDC P	PM Se	tting			
Minimum System Voltage Threshold	0		6400	Ŧ	mV
Vtrack Per Cell	0		100	•	mV
Virtual Diode Enabl	e		1-Enable	•	
System OVP enable	0	1-Er	hable SYS OV	•	
System OVP	0		11-110%	•	
System UVP	0		00-75%;	•	

Figure 15: NVDC PPM Settings

Figure 16 on page 9 shows how to configure the watchdog timer.



Watchdog Tim	ner
Watchdog Timer	00-Disable Tim
Watchdog Feed Bit	0-Normal 🔻
Watchdog Timer Setting when Input Absent	1-Enable 💌

Figure 16: Watchdog Timer

Figure 17 shows how to configure additional protections, including the input under-voltage (UV) threshold, input over-voltage (OV) threshold, and input OV deglitch time.

Other Protections	i		
Input Under Voltage Threshold	0	3.2	▼ V
Input Over Voltage Threshold	0	22.4	▼ V
Input Over Voltage Deglitch Time	0	0-100ns	•

Figure 17: Additional Protections

Figure 18 shows how to configure temperature-sense control. The TS/IMON pin can be set as either the temperature-sense pin (TS) or the battery current monitor pin (IMON).

Temperature S	ense	
TS/IMON Pin Function	0-TS	•
TS Sense Point	1-Battery FET	•
TS Function Enable	1-Enable	•
TS Function Action Enable when Fault	1-INT and TS a	•
TS Temperature Threshold	100-14.3%;(80°	•
Thermal loop Enable	1-Enable	•
Thermal Loop Temperature Threshold	111-120°C	•

Figure 18: Temperature Sense

Figure 19 shows how to configure the ADC operation mode.

ADC	
ADC Conversion Behavior	0-One-shot Cor 🔻
ADC Conversion One-shot Enable	1-Enable ADC 🔻

Figure 19: ADC Operation Mode

Figure 20 on page 10 shows the register map, which matches all the register results displayed on the BASIC and CONFIG pages.



	INFIG REGISTER MAP DEBUG	
Command cod	e Command name	Register
05H	Device Address Setting	0209
06H	Input Minimum Voltage Limit Setting	0039
07H	System Minimum Voltage Setting	0020
08H	Input Current Limit Setting	0030
09H	Output Voltage Setting	00F9
OAH	Battery Impedance Compensation and Output Current Limit Setting	0028
OBH	Battery Low Voltage Setting and Battery Discharge Current Regulation	3080
0CH	JEITA Action Setting	3410
0DH	Temperature Protection Setting	F399
OEH	Configuration Register 0	0010
OFH	Configuration Register 1	F244
10H	Configuration Register 2	0A7E
11H	Configuration Register 3	60E
12H	Configuration Register 4	3C7
	Charge Current Setting	0400

Figure 20: MP2760 Register Map

Figure 21 shows the monitor view.

MONITOR	R/W	
Status		
⊘ ADC		

Figure 21: Monitor View

Figure 22 shows how to configure the status.

Status		
MD_STAT	01-Operation Mode	
PG_STAT	1-Power Good	
SWITCH_STAT	11-BOOST	
BATTMISS_STAT	0-Normal	
Address Setting STAT	0-Single port	
CHG_STAT	011-CC charge	
VIN_MIN_STAT	0-Not in input voltage limit	
IIN_LIM_STAT	1-In input current limit	
TJREG_STAT	0-Not in thermal regulation loop	
IIN_DPM	500	mA

Figure 22: Status Setting



Figure 23 shows how the fault statuses are displayed.

→ Fault	
BFET_OC_FAULT	0-Normal
TS_FAULT	0-Normal
VIN_SRC_OV	0-Normal
VIN_SRC_UV	0-Normal
VIN_CHG_OV	0-Normal
VADP_OV	0-Normal
VSYS_OV	0-Normal
VSYS_UV	0-Normal
VBATT_OV	0-Normal
VBATT LOW	0-Normal
WTD_EXP	0-Normal
CHG TMR_EXP	0-Normal
THERM_SHDN	0-Normal
NTC_FAULT	000-Normal

Figure 23: Fault Settings

Figure 24 shows how to configure the analog-to-digital converter (ADC).

ADC		
VIN	4980	mV
IIN	212.5	mA
VBATT	3990	mV
VSYS	6540	mV
IBATT	62.5	mA
NTC	48.044	%
TS	48.825	%
TJ	30.561	°C
IBATT_DIS	175	mA
VIN_SRC	0	mV
IIN_SRC	0	mA

Figure 24: ADC Settings



EVALUATION BOARD SCHEMATIC



Figure 25: Evaluation Board Schematic



EV2760-VT-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	L2, L3, L4, L5	NC				
6	R1, R3, R4, R11, R20, R25	0	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
6	R5, R6, R12, R17, R18, R19	2Ω	Film resistor, 5%	0603	Liz	CR0603JA02R0G
4	R7, R8, R16, R27	20mΩ	Film resistor, 1%, 1/4W	1206	Cyntec	RL1632H-R020-FN
1	R9	1mΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML
1	R10	150kΩ	Film resistor, 5%, 1/10W	0603	Yageo	RC0603JR-07150KL
5	R13, R14, R21, R22, R26	10kΩ	Film resistor, 1%, 1/10W	0603	Yageo	RC0603FR-0710KL
2	R15, R23	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
1	R24	5.1kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-075K1L
4	R28, R29, R30, R31	NC				
11	C1, C3, C15, C16, C17, C22, C29, C34, C36, C37, C39	NC				
4	C2, C4, C18, C33	100nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206071
2	C5, C27	1µF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E105KA12
6	C6, C8, C10, C12, C28, C31	22µF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
9	C7, C9, C11, C13, C14, C19, C20, C30, C32	NC				
5	C21, C23, C25, C38, C40	10µF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC7E106KE11L
1	C35	4.7µF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R61E475KE11D
1	LED1	Red	Red LED	0805	Bright LED	BL-HUE35A-AV-TRB
2	D1, D2	NC				
1	M1	8.5mΩ	N-channel MOSFET, 30V, 20A	PowerPAK 1212-8	Vishay	SISA14DN-T1-GE3
13	ACOK, ADDR, AGND, AGND, EXT, IMON, INT, NTC, TS, VCC, VNTC, SCL, SDA	2.54mm	Pin header	DIP	Any	



EV2760-VT-00A BILL OF MATERIALS (continued)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
11	TP1, TP2, TP3, TP4, TP5, TP6 (GND), TP7 (GND), TP8 (GND), TP9 (GND), TP11, TP12	1mm	Test point, φ = 1mm	DIP	Any	
10	VIN, VINEMI, VBATT, VSYS, VSYSEMI, GND, GND, GND, VIGND, VBGND	2mm	Test point, φ = 2mm	DIP	Any	
2	JP1, JP2	2.54mm	Pin header	DIP	Any	
1	JP1	2.54mm	Jumper	DIP	Any	
1	L1	1.5µH	Inductor, 9.7mΩ, 9A	SMD	MPS	MPL-AL5030-1R5
1	U1	MP2760	1-cell to 4-cell buck- boost charger	TQFN-30 (4mmx 5mm)	MPS	MP2760GVT-0000



EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, $C_{IN} = 10\mu F \times 5 + 1\mu F \times 1$, $C_{SYS} = 22\mu F \times 4 + 1\mu F \times 1$, $C_{BATT} = 22\mu F \times 2$, L = 1.5µH (10m Ω), $f_{SW} = 600$ kHz, 2-cell battery. $T_A = 25^{\circ}$ C, unless otherwise noted.



Thermal Performance

Charge mode, $V_{IN} = 20V$, $I_{INLIMIT} = 3A$, $V_{BATT} = 8.2V$, $I_{CC} = 5A$



Efficiency vs. Source Current in Source Mode $V_{BATT} = 8.4V, f_{SW} = 600$ kHz, 2-cell battery, $V_{IN SRC} = 5V/9V/12V/15V/20V$ 100% € 95% EFFICIENCY 90% VIN SRC=5V VIN SRC=9V VIN SRC=12V 85% VIN SRC=15V VIN SRC=20V 80% 1 2 0.5 2.5 3 1.5 CURRENT (A)

Thermal Performance

Source mode, V_{BATT} = 8.4V, V_{IN_SRC} = 20V, I_{IN_SRC} = 1.8A





EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, $C_{IN} = 10\mu F \times 5 + 1\mu F \times 1$, $C_{SYS} = 22\mu F \times 4 + 1\mu F \times 1$, $C_{BATT} = 22\mu F \times 2$, L = 1.5µH (10m Ω), $f_{SW} = 600$ kHz, 2-cell battery. $T_A = 25^{\circ}$ C, unless otherwise noted.



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EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, $C_{IN} = 10\mu F x 5 + 1\mu F x 1$, $C_{SYS} = 22\mu F x 4 + 1\mu F x 1$, $C_{BATT} = 22\mu F x 2$, L = 1.5 μ H (10m Ω), $f_{SW} = 600$ kHz, 2-cell battery. $T_A = 25^{\circ}$ C, unless otherwise noted.





PCB LAYOUT



Figure 26: Top Silk



Figure 28: Mid-Layer 1



Figure 30: Bottom Layer



Figure 27: Top Layer



Figure 29: Mid-Layer 2



Figure 31: Bottom Silk



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-
1.1	6/30/2023	 Updated the following in Figure 25 to be consistent with the EVB images and BOM: C14 = NC C19 = NC C21 = 10μF C25 = 10μF R9 = 1MΩ R14 = 10kΩ R20 = 0Ω Updated the PGND connector to GND Updated the ACGATE pin to AGND on the TP10 connector Removed T9 Added R28 = R29 = R30 = R31 = NC Removed AGND14 	12

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