ESD7102, SZESD7102

ESD Protection Diodes

Low Capacitance ESD Protection Diodes for High Speed Data Line

The ESD7102 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The small form factor, flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI.

Features

- Low Capacitance (0.3 pF Typical, I/O to GND)
- Short to Battery Survivability
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4 (ESD)
- Low ESD Clamping Voltage (34 V Typical, +8 A TLP, I/O to GND)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- USB2.0/3.0
- LVDS
- HDMI
- High Speed Differential Pairs

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact IEC 61000−4−2 Air ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	ESD	±8 ±15 ±8 ±20 ±27	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
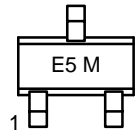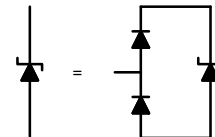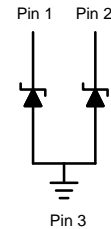
ON Semiconductor®

MARKING DIAGRAM

SC−75
CASE 463

E5 M
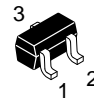
E5 = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATIC

Pin 1   Pin 2

Pin 3

ORDERING INFORMATION

ESD7102, SZESD7102

ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V$_{RWM}$	I/O Pin to GND			16	V
Breakdown Voltage	V$_{BR}$	I$_T$ = 1 mA, I/O Pin to GND	16.5			V
Reverse Leakage Current	I$_R$	V$_{RWM}$ = 5 V, I/O Pin to GND			1	μA
Clamping Voltage (Note 1)	V$_C$	IEC61000−4−2, ±8 kV Contact	See Figures 1 and 2			
Clamping Voltage TLP (Note 2)	V$_C$	I$_{PP}$ = 8 A I$_{PP}$ = 16 A I$_{PP}$ = −8 A I$_{PP}$ = −16 A		34 55 −5.3 −10		V
Dynamic Resistance (Note 2)	I$_R$	TLP Pulse		1.5		Ω
Junction Capacitance	C$_J$	V$_R$ = 0 V, f = 1 MHz between I/O Pins V$_R$ = 0 V, f = 1 MHz between I/O Pins and GND		0.2 0.3	0.4 0.5	pF
Junction Capacitance Match	ΔC$_J$	V$_R$ = 0 V, f = 1 MHz between I/O1 to GND and I/O 2 to GND		5	10	%
Insertion Loss		f = 1 GHz f = 3 GHz		0.1 0.2		dB
3dB Bandwidth	f$_{BW}$	R$_L$ = 50 Ω		5		GHz

1. For test procedure see Figures 5 and 6 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z$_0$ = 50 Ω, t$_p$ = 100 ns, t$_r$ = 4 ns, averaging window; t$_1$ = 30 ns to t$_2$ = 60 ns.
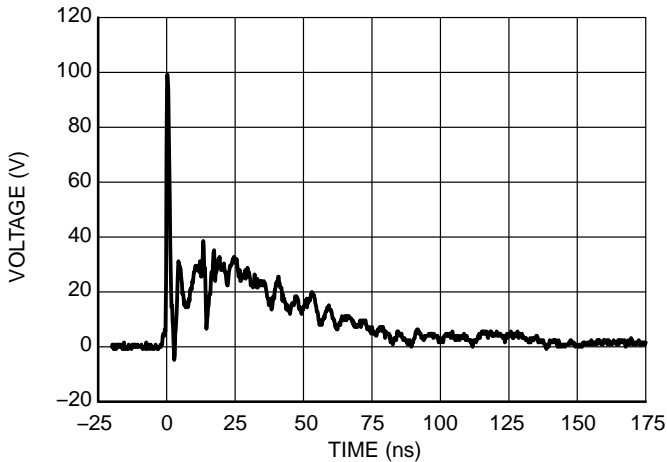

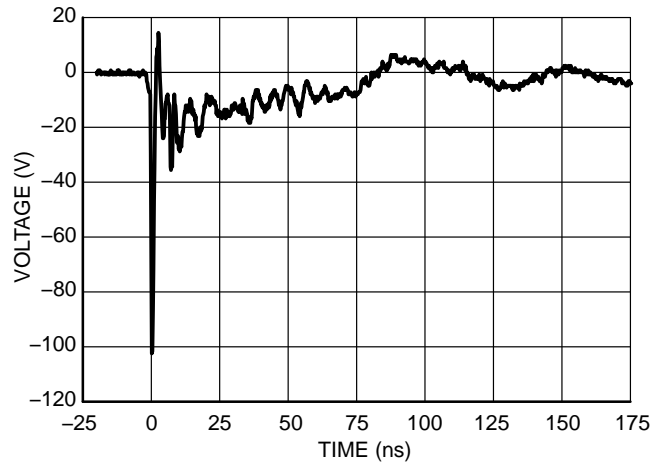**Figure 1. IEC61000−4−2 +8 kV Contact ESD Clamping Voltage**

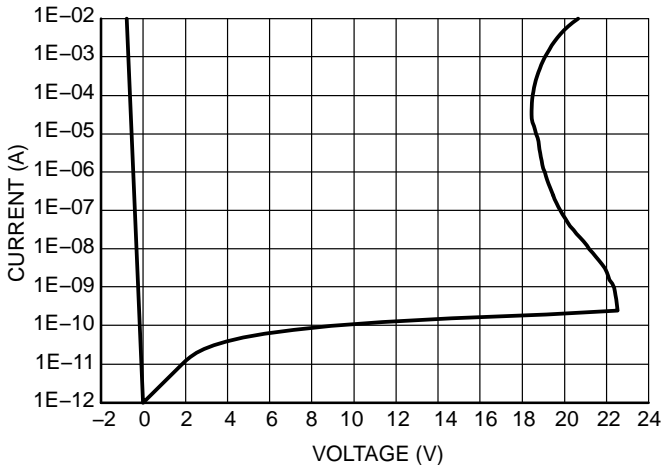**Figure 2. IEC61000−4−2 −8 kV Contact ESD Clamping Voltage**
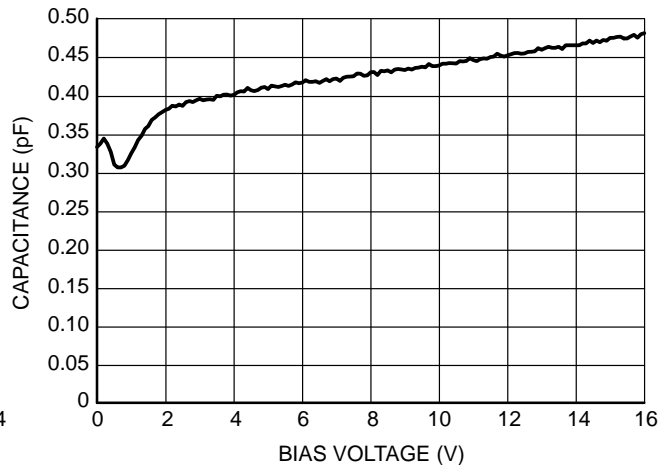

Figure 3. Typical IV Characteristic Curve

Figure 4. Typical CV Characteristic Curve

IEC 61000−4−2 Spec.

Level	Test Volt-age (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

IEC61000−4−2 Waveform

I_{peak}
100%
90%
I @ 30 ns
I @ 60 ns
10%
t_P = 0.7 ns to 1 ns
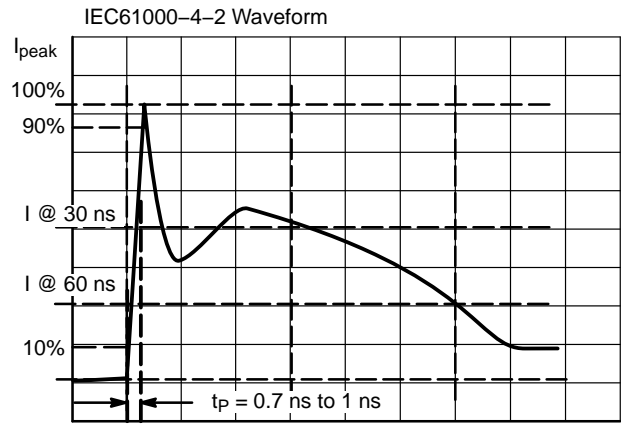
Figure 5. IEC61000−4−2 Spec

ESD Gun   DUT   Oscilloscope

50 Ω Cable   50 Ω
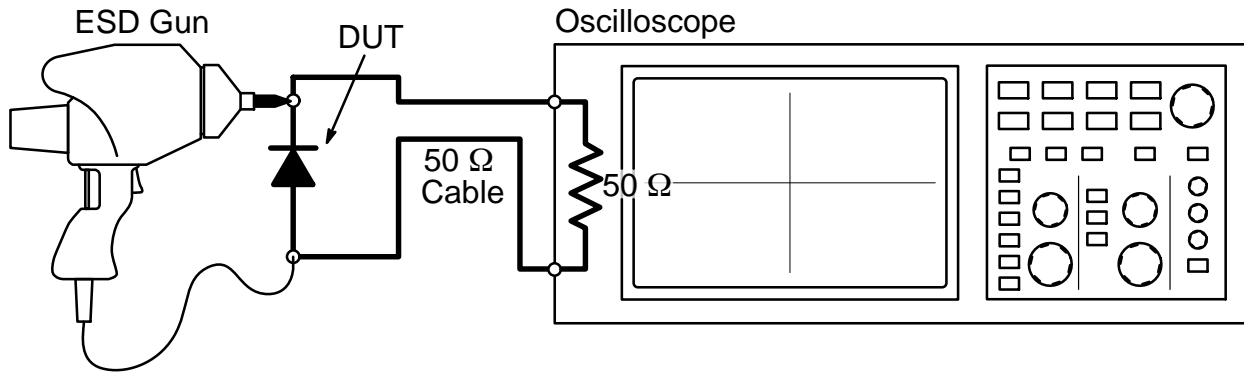
Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.
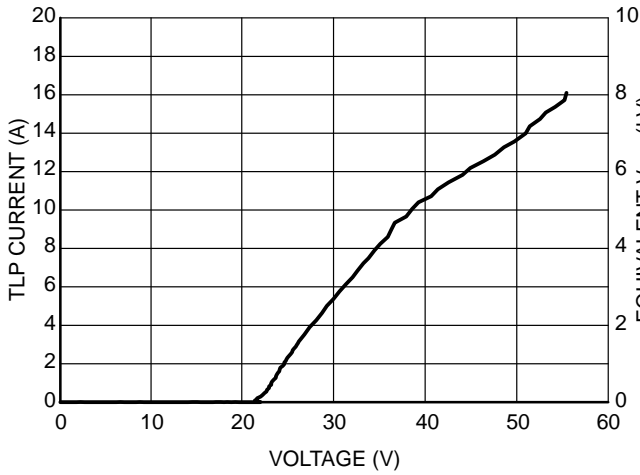
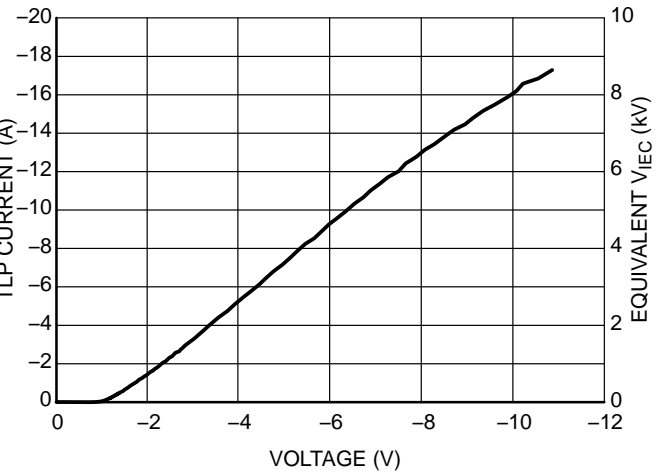# ESD7102, SZESD7102

Figure 7. Positive TLP IV Curve

Figure 8. Negative TLP IV Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I–V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I–V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I–V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.
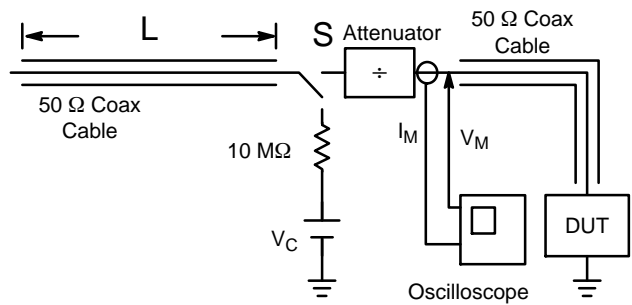
Figure 9. Simplified Schematic of a Typical TLP System
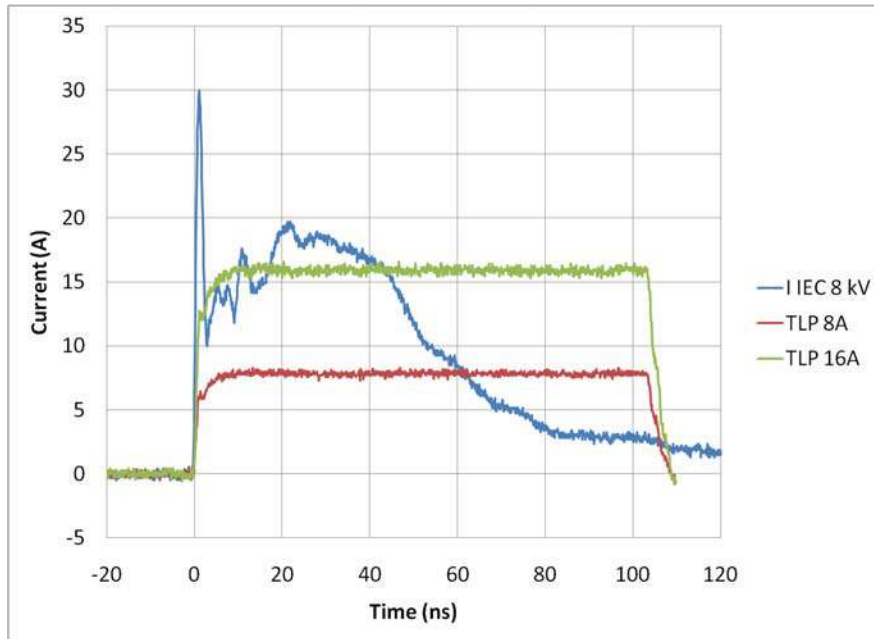
Figure 10. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

Without ESD7102 | With ESD7102
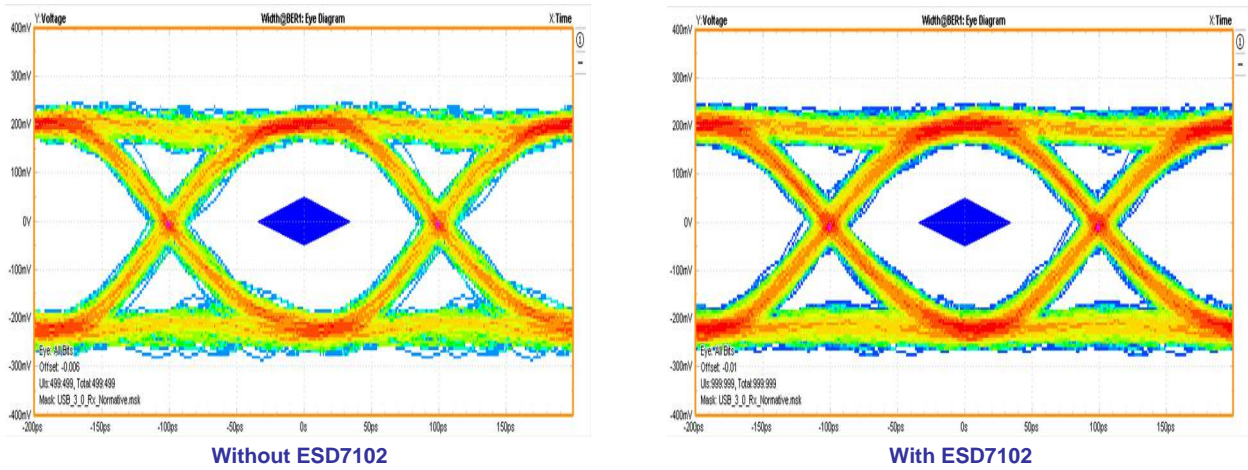
Figure 11. USB3.0 Eye Diagram with and without ESD7102 at 5 Gb/s
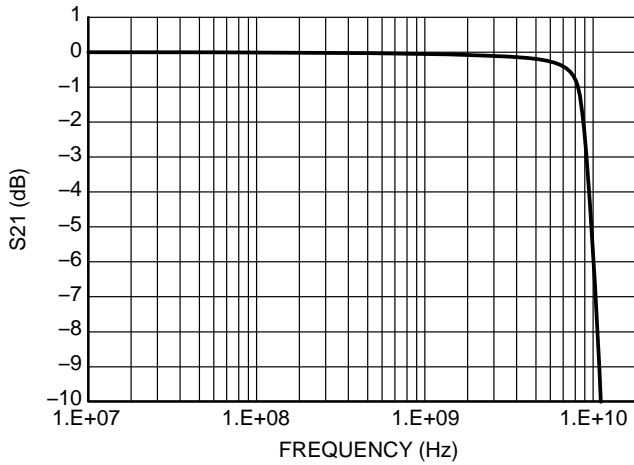
Figure 12. Typical Insertion Loss
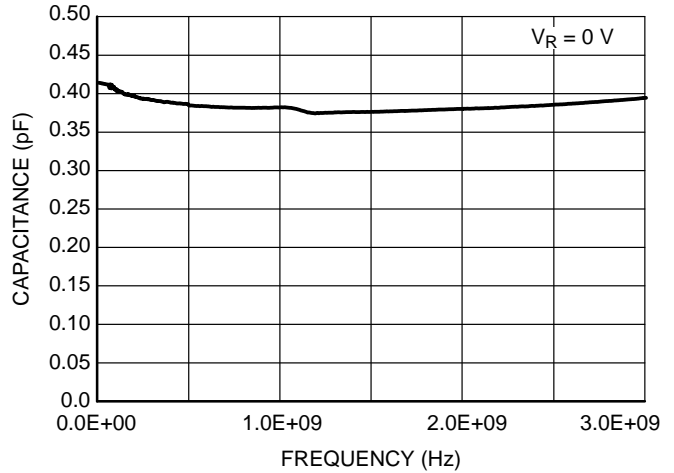
Figure 13. Typical Capacitance over Frequency

ORDERING INFORMATION

Device	Package	Shipping†
ESD7102BT1G	SC−75 (Pb−Free)	3000 / Tape & Reel
SZESD7102BT1G*	SC−75 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®
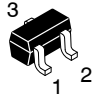
SC−75/SOT−416
CASE 463−01
ISSUE G

DATE 07 AUG 2015

SCALE 4:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.061	0.063	0.065
E	0.70	0.80	0.90	0.027	0.031	0.035
e	1.00 BSC			0.04 BSC		
L	0.10	0.15	0.20	0.004	0.006	0.008
H_E	1.50	1.60	1.70	0.060	0.063	0.067

$\oplus$ 0.20 (0.008) Ⓜ D

$=$ 0.20 (0.008) E

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

GENERIC
MARKING DIAGRAM*
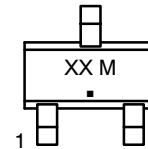
XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*

$\dfrac{0.356}{0.014}$

$\dfrac{1.803}{0.071}$

$\dfrac{0.787}{0.031}$

$\dfrac{0.508}{0.020}$

$\dfrac{1.000}{0.039}$
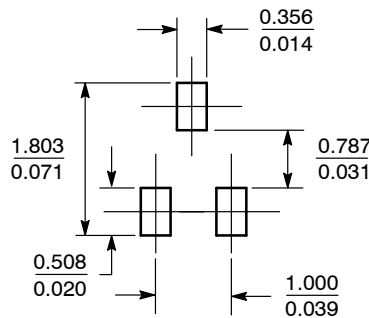
SCALE 10:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASB15184C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−75/SOT−416		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊