



RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 63 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2110 to 2200 MHz.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance:
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 500 \text{ mA}$, $V_{GSB} = 0.7 \text{ Vdc}$, $P_{out} = 63 \text{ W Avg.}$,
 Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	16.6	49.2	7.9	-30.5
2140 MHz	16.8	49.7	7.9	-31.0
2170 MHz	16.7	49.0	7.9	-32.8
2200 MHz	16.3	47.2	7.9	-36.1

Features

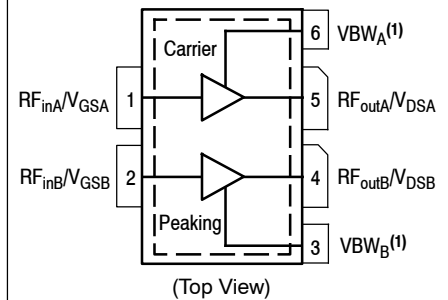
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2T21H360-23NR6

2110-2200 MHz, 63 W AVG., 28 V
 AIRFAST RF POWER LDMOS
 TRANSISTOR



OM-1230-4L2S
 PLASTIC



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

- Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 72°C, 63 W Avg., W-CDMA, 28 Vdc, $I_{DQA} = 500$ mA, $V_{GSB} = 0.7$ Vdc, 2140 MHz	$R_{\theta JC}$	0.19	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics (4)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μAdc

On Characteristics - Side A, Carrier

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 140$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DD} = 28$ Vdc, $I_D = 500$ mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.4	1.9	2.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1.4$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

On Characteristics - Side B, Peaking

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 240$ μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 2.4$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2) (In Freescale Doherty Production Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 500\text{ mA}$, $V_{GSB} = 0.5\text{ Vdc}$, $P_{out} = 63\text{ W Avg.}$, $f = 2140\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	16.2	16.8	19.2	dB
Drain Efficiency	η_D	45.4	48.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.1	7.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	-29.6	-26.0	dBc

Load Mismatch ⁽²⁾ (In Freescale Doherty Production Test Fixture, 50 ohm system) $I_{DQA} = 500\text{ mA}$, $V_{GSB} = 0.5\text{ Vdc}$, $f = 2140\text{ MHz}$

VSWR 10:1 at 32 Vdc, 316 W CW Output Power (3 dB Input Overdrive from 229 W CW Rated Power)	No Device Degradation
------------------------------------------------------------------------------------------------	-----------------------

Typical Performance ⁽²⁾ (In Freescale Doherty Characterization Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 500\text{ mA}$, $V_{GSB} = 0.7\text{ Vdc}$, 2110–2200 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	229	—	W
P_{out} @ 3 dB Compression Point ⁽³⁾	P3dB	—	373	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2200 MHz bandwidth)	Φ	—	-29	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Gain Flatness in 90 MHz Bandwidth @ $P_{out} = 63\text{ W Avg.}$	G_F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.009	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.002	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T21H360-23NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L2S

- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

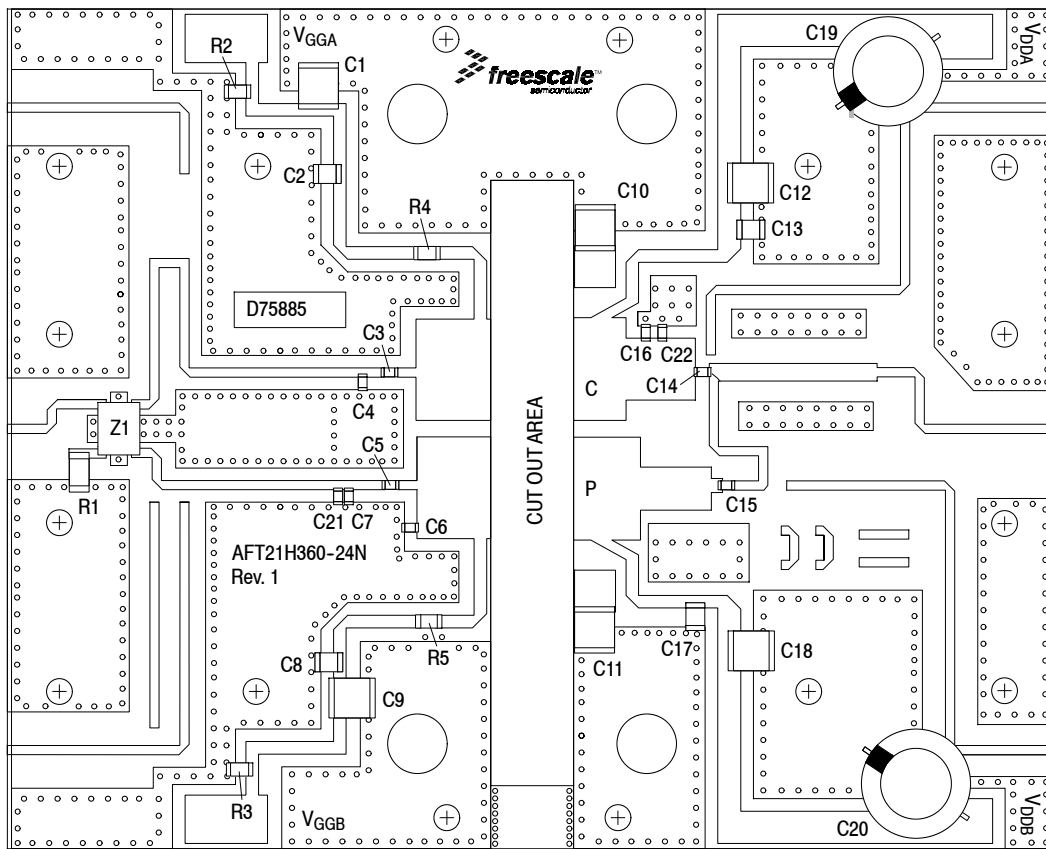


Figure 2. A2T21H360-23NR6 Test Circuit Component Layout

Table 7. A2T21H360-23NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C10, C11, C12, C18	10 μ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C8, C13, C17	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C3, C5	9.1 pF Chip Capacitors	ATC600F9R1BT250XT	ATC
C4	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C6	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
C7	1.1 pF Chip Capacitor	ATC600F1R1BT250XT	ATC
C14	4.7 pF Chip Capacitor	ATC600F4R7BT250XT	ATC
C15 ⁽¹⁾ C15 ⁽²⁾	3.9 pF Chip Capacitor 9.1 pF Chip Capacitor	ATC600F3R9BT250XT ATC600F9R1BT250XT	ATC ATC
C16	1.0 pF Chip Capacitor	ATC600F1R0BT250XT	ATC
C19, C20	470 μ F, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C21	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C22	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
R1	50 Ω , 4 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	5.6 k Ω , 1/4 W Chip Resistors	CRCW12065K60FKEA	Vishay
R4, R5	6.2 Ω , 1/4 W Chip Resistors	CRCW12066R20FKEA	Vishay
Z1	2000–2300 MHz Band, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D75885	MTL

1. On characterization board only.

2. On production board only.

TYPICAL CHARACTERISTICS — 2110–2200 MHz

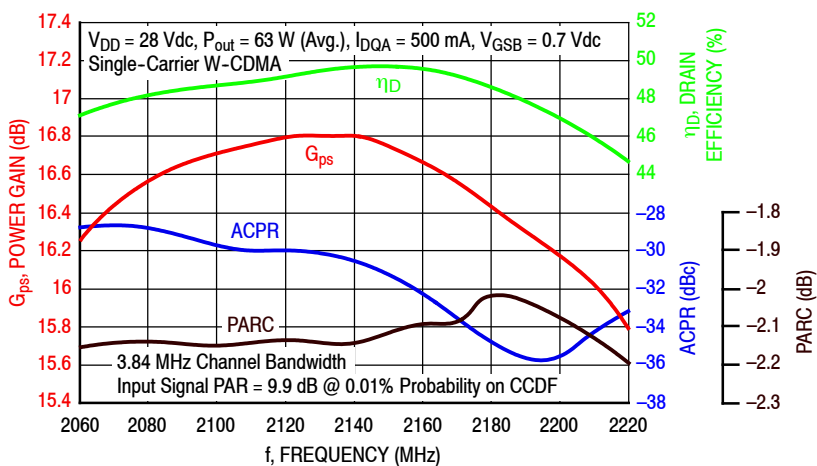


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 63$ Watts Avg.

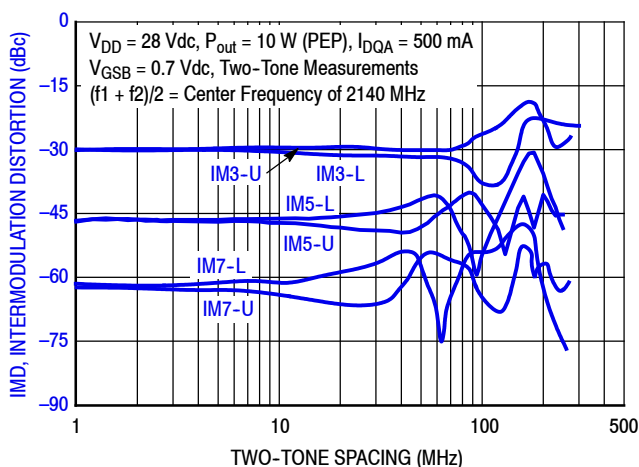


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

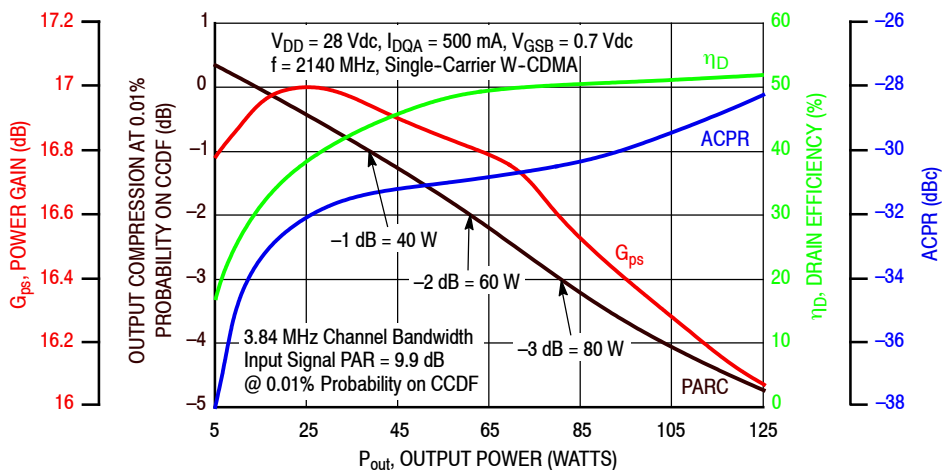


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2200 MHz

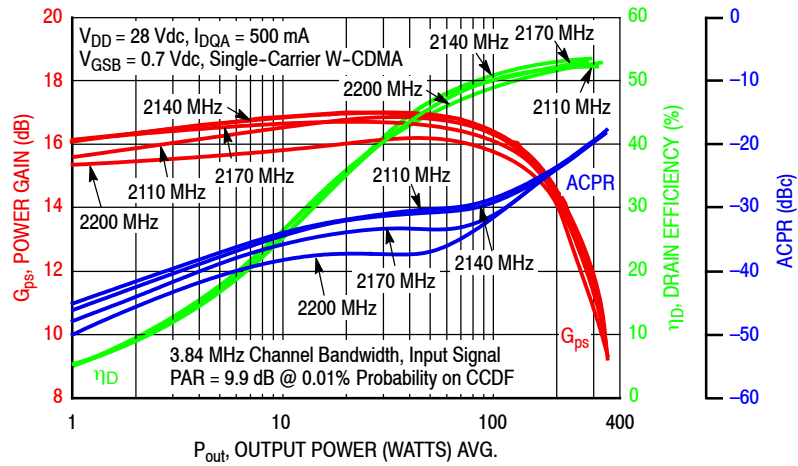


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

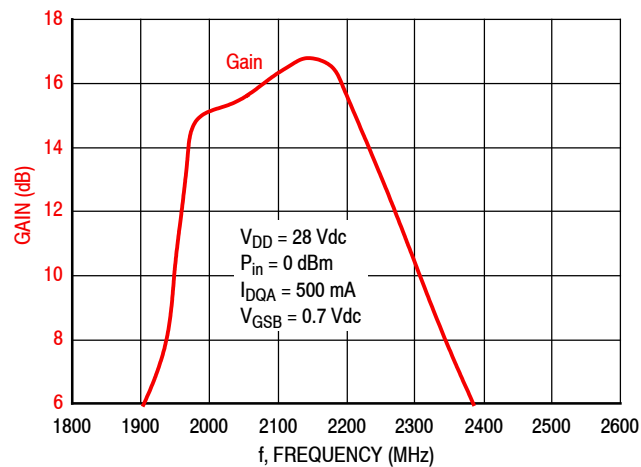


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 806 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	8.29 – j3.71	9.64 + j2.95	1.69 – j3.90	20.2	51.7	148	56.0	-14
2140	8.62 – j1.68	9.40 – j0.19	1.66 – j3.94	20.1	51.5	141	54.1	-13
2170	7.88 + j1.11	7.39 – j2.67	1.69 – j3.81	20.5	51.5	141	55.7	-14
2200	5.32 + j2.59	5.04 – j2.83	1.71 – j4.35	19.8	51.5	141	53.3	-14

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	8.29 – j3.71	10.7 + j2.72	1.66 – j3.99	18.0	52.5	180	58.2	-18
2140	8.62 – j1.68	9.87 – j0.96	1.63 – j4.09	17.9	52.4	173	55.9	-18
2170	7.88 + j1.11	7.26 – j3.17	1.71 – j4.01	18.2	52.3	171	57.5	-18
2200	5.32 + j2.59	4.84 – j3.34	1.65 – j4.39	17.7	52.4	172	55.1	-18

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 806 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	8.29 – j3.71	10.9 + j0.05	3.52 – j1.49	23.2	48.5	71	64.7	-17
2140	8.62 – j1.68	8.38 – j2.17	3.42 – j1.87	22.9	48.7	74	63.7	-15
2170	7.88 + j1.11	6.26 – j3.26	2.74 – j2.46	22.5	49.7	93	62.9	-16
2200	5.32 + j2.59	4.07 – j3.23	2.48 – j2.44	22.6	49.6	91	63.1	-18

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	8.29 – j3.71	10.2 – j0.98	3.52 – j1.42	21.2	49.3	85	66.6	-26
2140	8.62 – j1.68	7.62 – j2.68	3.42 – j1.74	20.9	49.5	89	65.9	-23
2170	7.88 + j1.11	5.88 – j3.53	2.68 – j2.34	20.6	50.4	109	65.2	-24
2200	5.32 + j2.59	3.29 – j3.01	2.43 – j1.57	21.3	49.1	80	65.4	-27

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

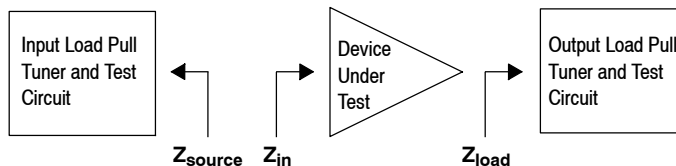


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

$V_{DD} = 28$ Vdc, $V_{GSB} = 1.8$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2110	1.53 – j4.85	1.68 + j5.24	2.03 – j4.56	18.7	54.1	255	51.5	–15
2140	1.72 – j5.10	2.01 + j5.45	2.08 – j4.54	18.9	54.0	251	51.2	–16
2170	2.19 – j5.66	2.53 + j5.70	2.05 – j4.58	18.9	54.0	252	51.0	–17
2200	2.59 – j5.85	3.28 + j5.86	2.07 – j4.68	18.9	54.0	252	51.5	–17

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2110	1.53 – j4.85	1.70 + j5.31	1.86 – j4.74	16.3	54.9	309	53.5	–20
2140	1.72 – j5.10	2.07 + j5.52	1.88 – j4.85	16.5	54.8	304	52.9	–21
2170	2.19 – j5.66	2.62 + j5.80	1.95 – j4.84	16.5	54.8	305	53.0	–22
2200	2.59 – j5.85	3.45 + j6.01	2.04 – j4.88	16.7	54.9	306	54.0	–23

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

$V_{DD} = 28$ Vdc, $V_{GSB} = 1.8$ Vdc, Pulsed CW, 10 μ sec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2110	1.53 – j4.85	1.75 + j5.40	3.28 – j4.94	20.0	53.3	214	56.9	–17
2140	1.72 – j5.10	2.16 + j5.70	3.72 – j4.61	20.4	53.1	203	56.9	–18
2170	2.19 – j5.66	2.78 + j5.99	3.92 – j4.22	20.7	52.9	197	57.6	–20
2200	2.59 – j5.85	3.68 + j6.13	3.90 – j3.96	20.7	52.9	194	58.4	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM ($^\circ$)
2110	1.53 – j4.85	1.82 + j5.42	3.28 – j5.22	18.0	54.0	251	59.8	–24
2140	1.72 – j5.10	2.26 + j5.71	3.65 – j4.90	18.2	53.9	243	59.8	–25
2170	2.19 – j5.66	2.90 + j5.98	3.78 – j4.48	18.5	53.8	240	60.3	–27
2200	2.59 – j5.85	3.94 + j6.10	4.03 – j4.10	18.7	53.6	228	61.3	–28

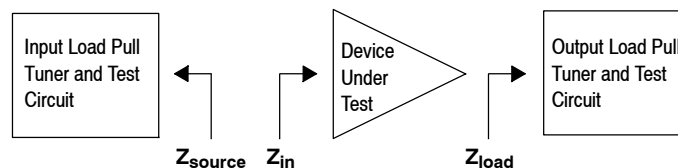
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



A2T21H360-23NR6

P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

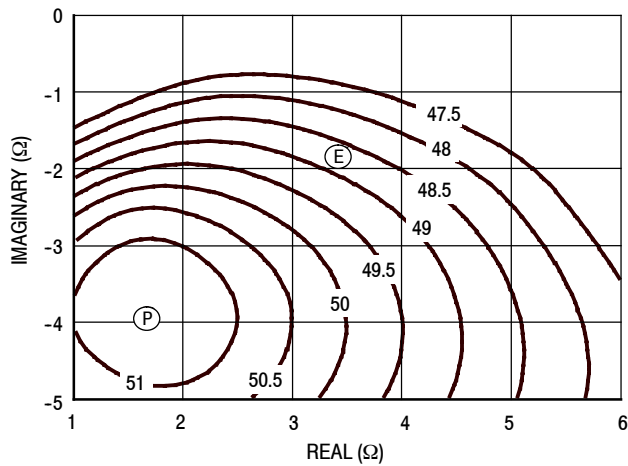


Figure 8. P1dB Load Pull Output Power Contours (dBm)

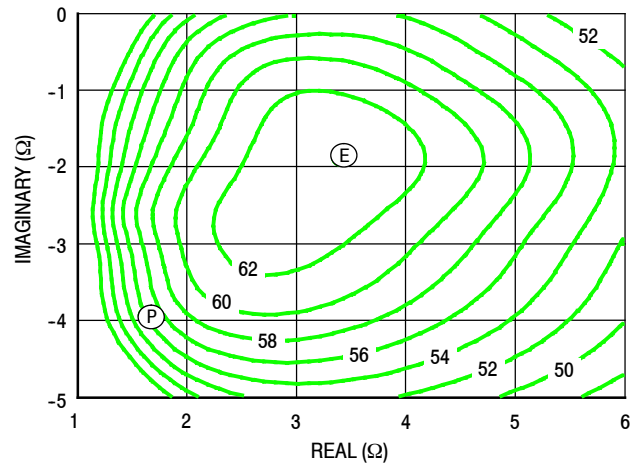


Figure 9. P1dB Load Pull Efficiency Contours (%)

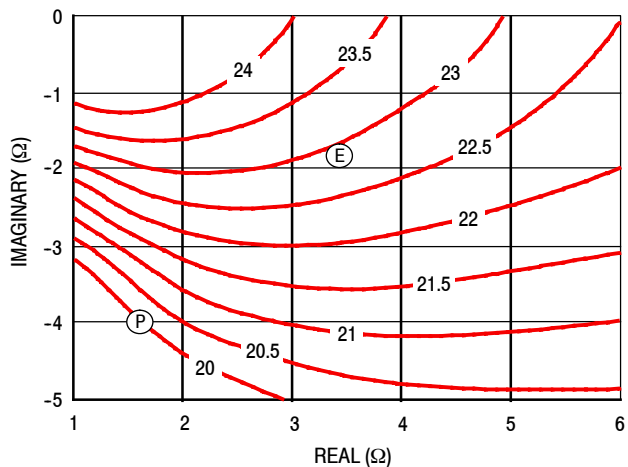


Figure 10. P1dB Load Pull Gain Contours (dB)

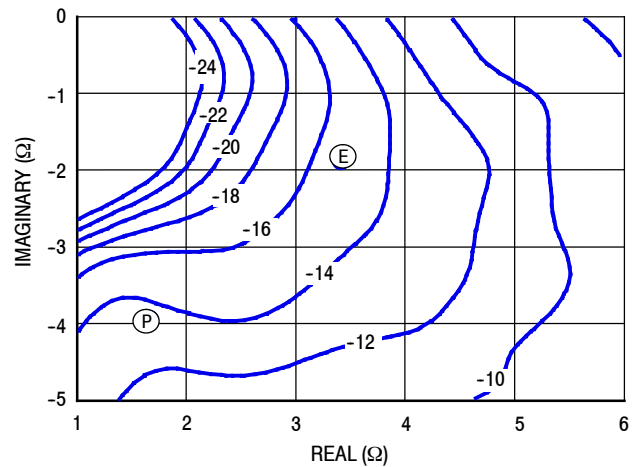


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

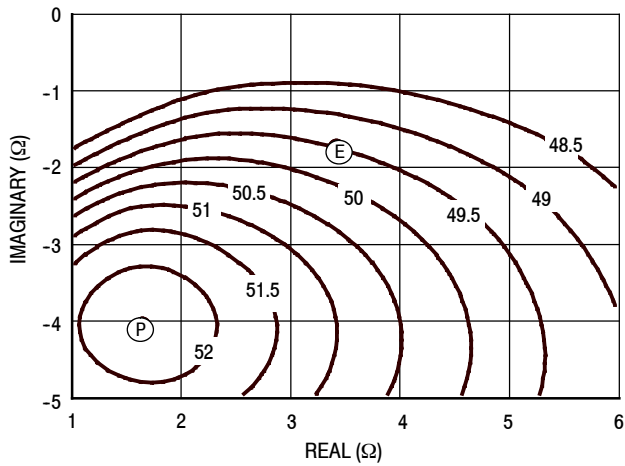


Figure 12. P3dB Load Pull Output Power Contours (dBm)

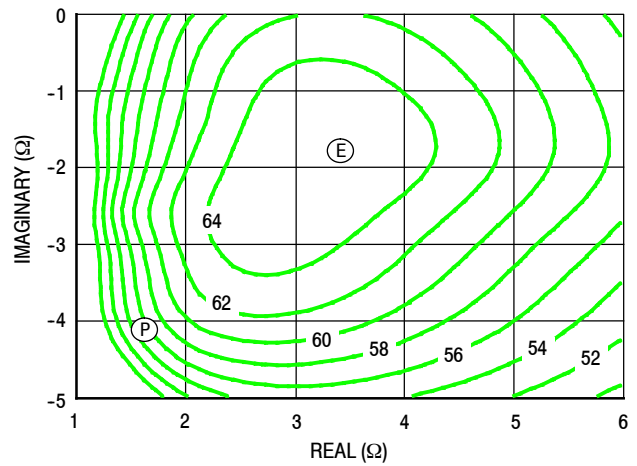


Figure 13. P3dB Load Pull Efficiency Contours (%)

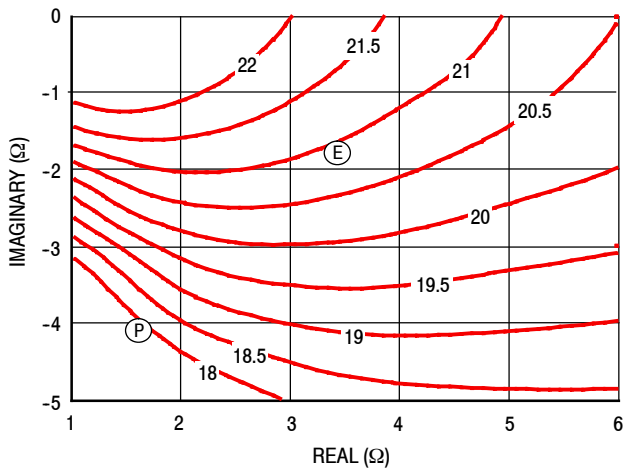


Figure 14. P3dB Load Pull Gain Contours (dB)

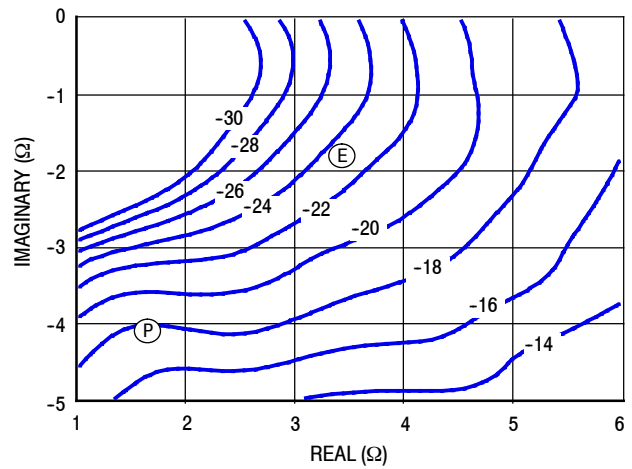


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

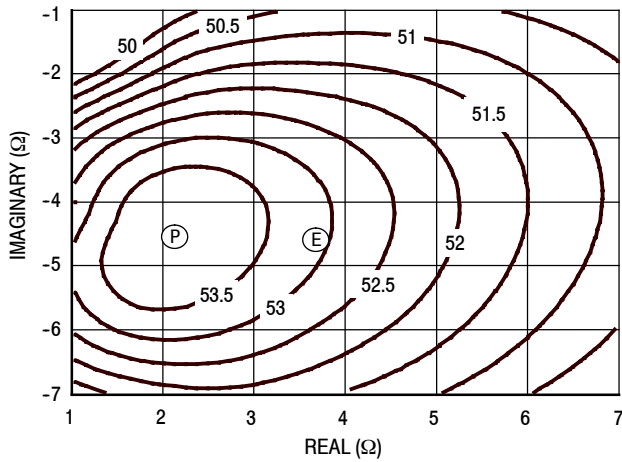


Figure 16. P1dB Load Pull Output Power Contours (dBm)

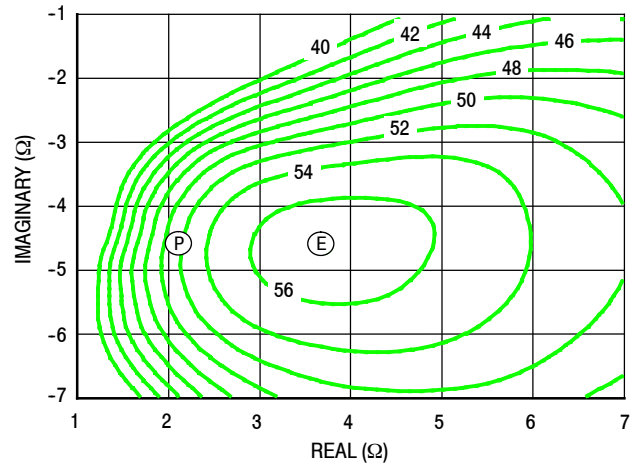


Figure 17. P1dB Load Pull Efficiency Contours (%)

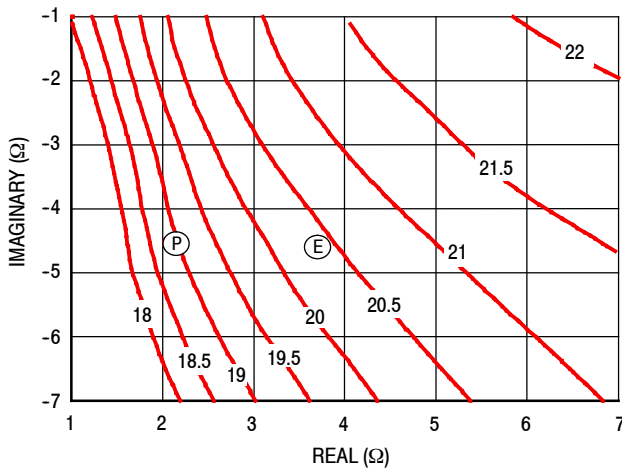


Figure 18. P1dB Load Pull Gain Contours (dB)

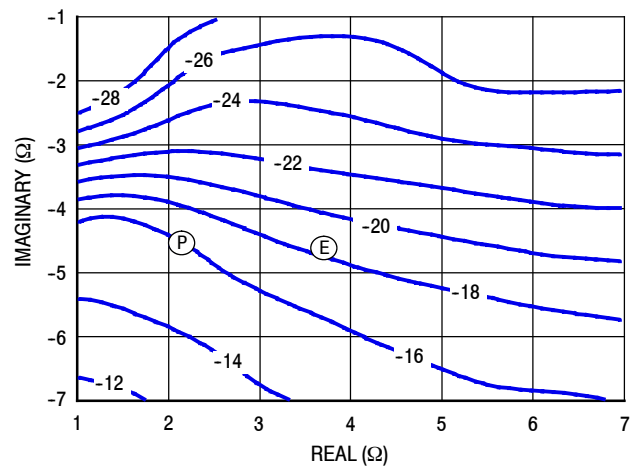


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

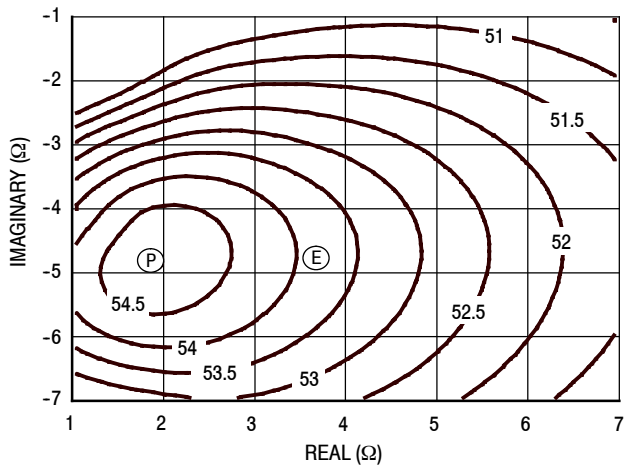


Figure 20. P3dB Load Pull Output Power Contours (dBm)

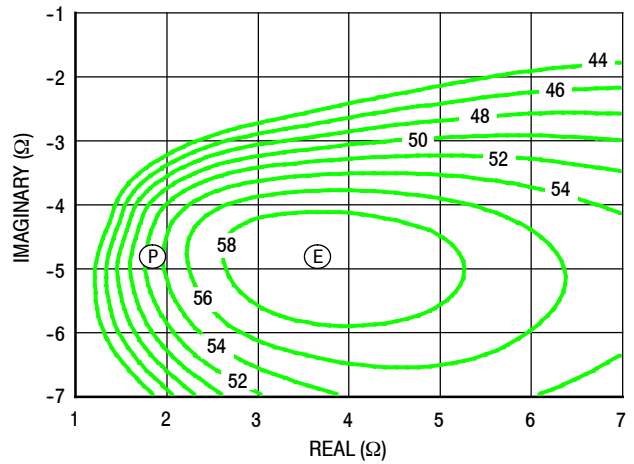


Figure 21. P3dB Load Pull Efficiency Contours (%)

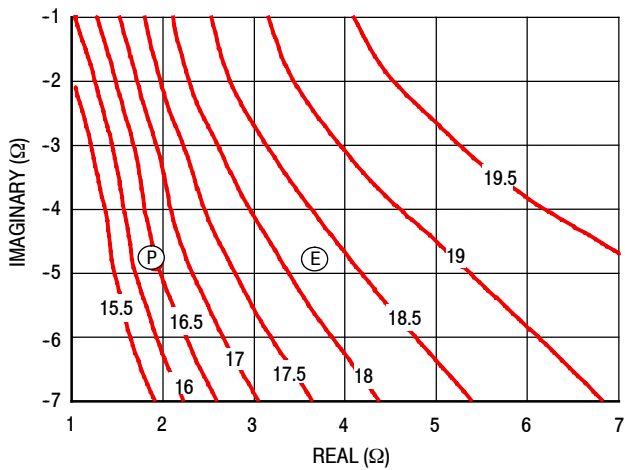


Figure 22. P3dB Load Pull Gain Contours (dB)

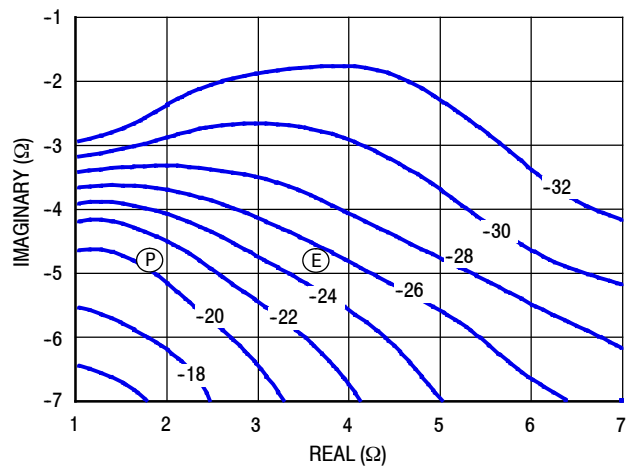
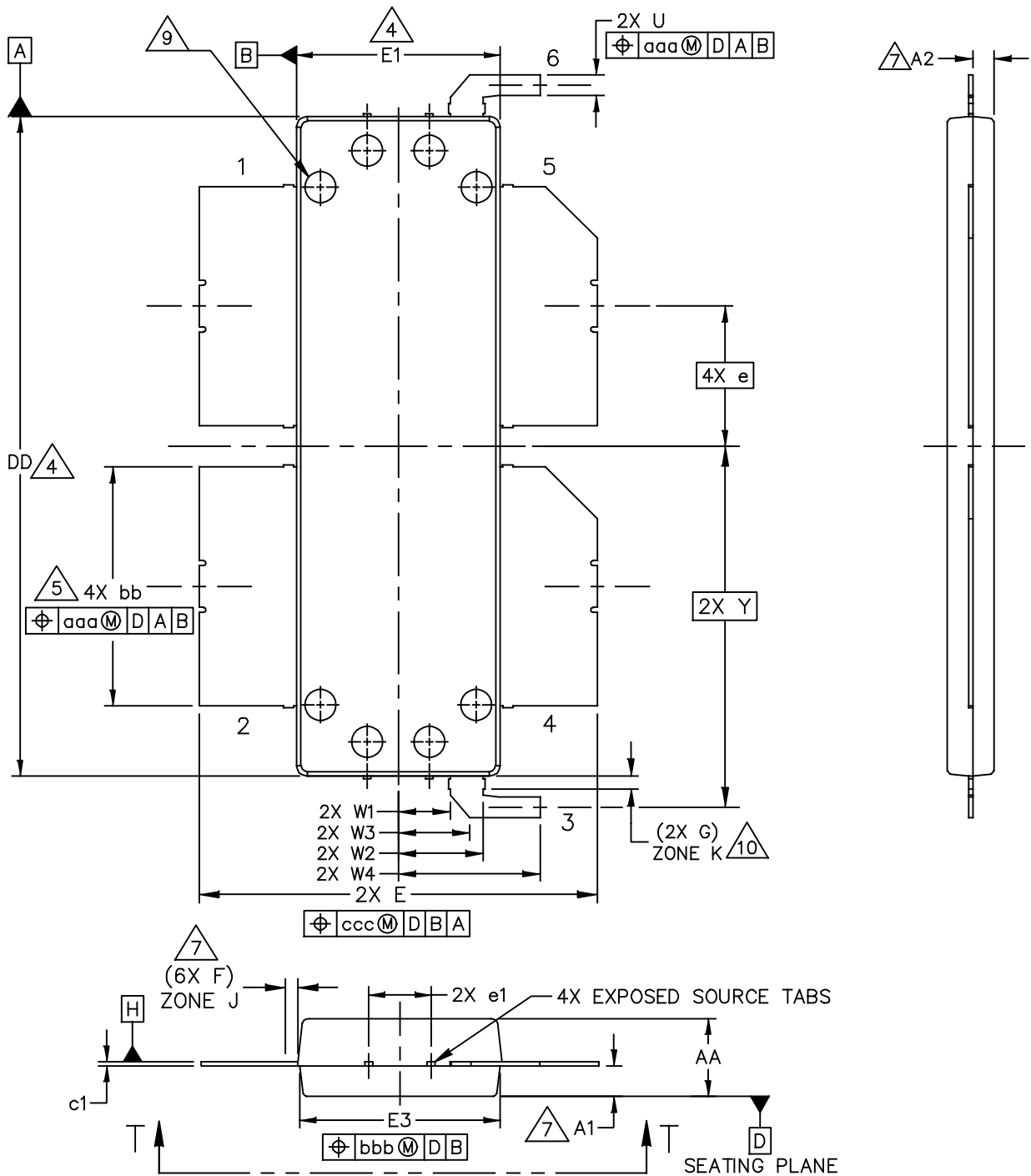


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

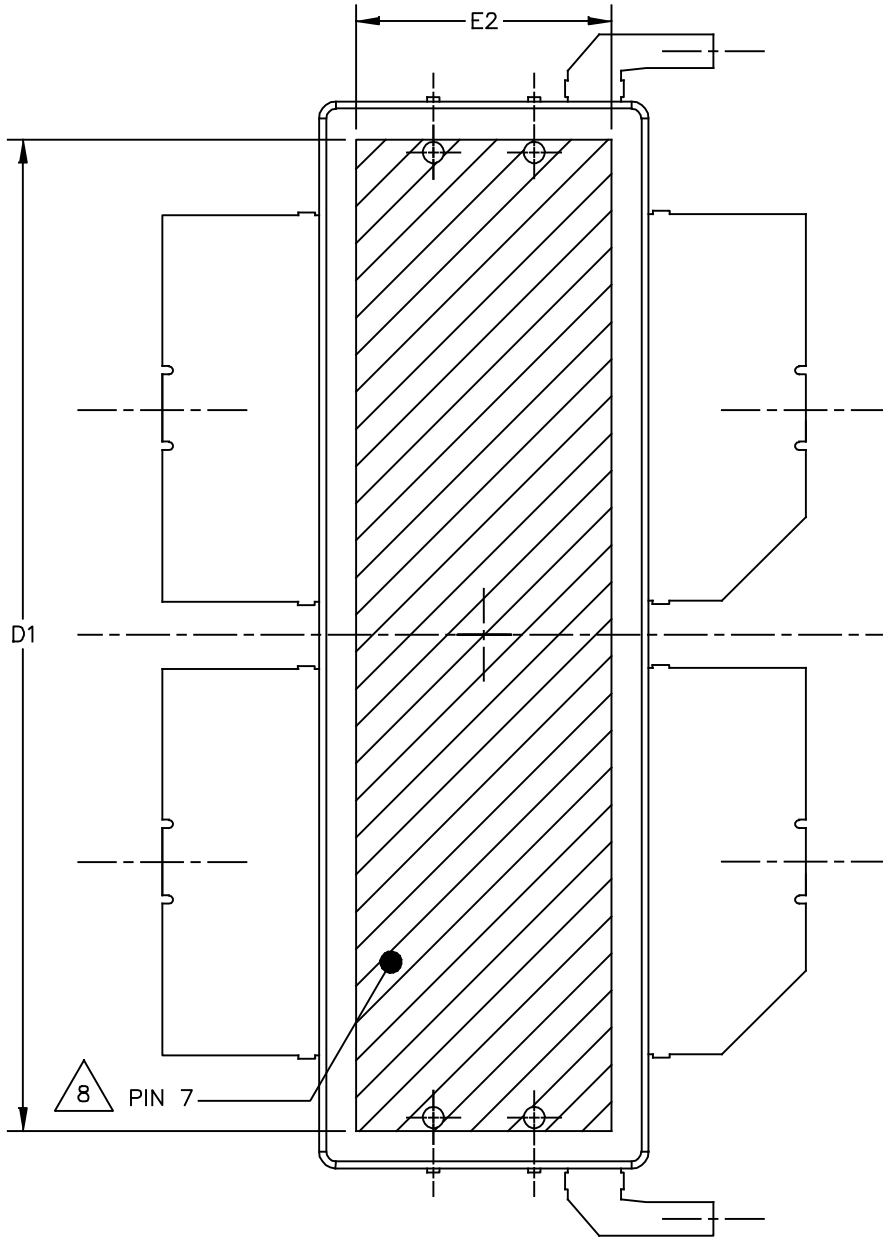
- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM-1230-4L2S	DOCUMENT NO: 98ASA00885D STANDARD: NON-JEDEC SOT1819-2	REV: A 18 FEB 2016

A2T21H360-23NR6



BOTTOM VIEW
VIEW T-T

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: OM-1230-4L2S		DOCUMENT NO: 98ASA00885D	REV: A
		STANDARD: NON-JEDEC	
		SOT1819-2	18 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLY WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1, 2, 4 AND 5. A2 APPLIES TO PINS 3 AND 6.
8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W2	.158	.168	4.01	4.27
A1	.059	.065	1.50	1.65	W3	.132	.142	3.35	3.61
A2	.056	.068	1.42	1.73	W4	.265	.281	6.73	7.14
DD	1.267	1.273	32.18	32.33	U	.037	.043	0.94	1.09
D1	1.180	----	29.97	----	Y	.695 BSC		17.65 BSC	
E	.762	.770	19.35	19.56	bb	.457	.463	11.61	11.76
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.270 BSC		6.86 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 REF		0.64 REF		aaa	.004		0.10	
G	.030 REF		0.76 REF		bbb	.006		0.15	
W1	.095	.105	2.41	2.67	ccc	.010		0.25	

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM-1230-4L2S		DOCUMENT NO: 98ASA00885D REV: A	
		STANDARD: NON-JEDEC	
		SOT1819-2	18 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2016	• Initial release of data sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2016 Freescale Semiconductor, Inc.

