Performance Demonstration Kit for the ADS131E08

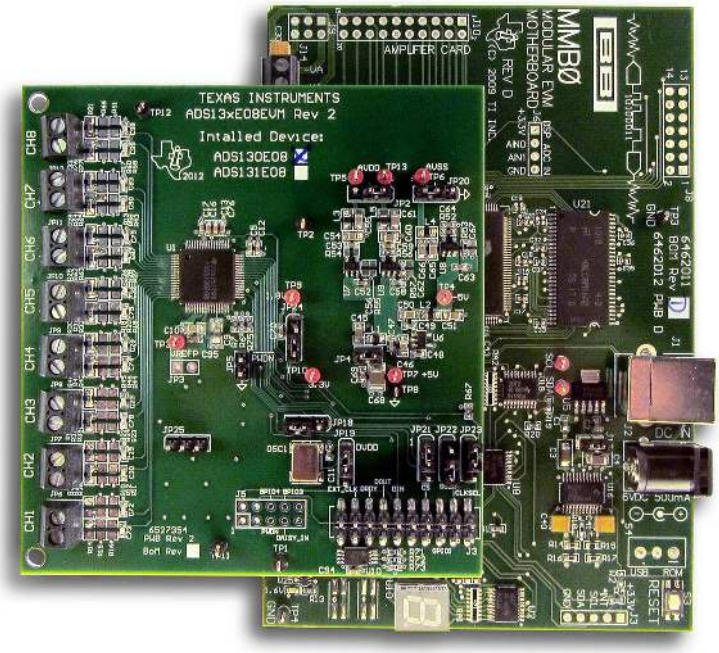

Figure 1. ADS131E08EVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS131E08EVM-PDK. This performance demonstration kit is an evaluation module for the ADS131E08, an eight-channel, 24-bit, low-power, integrated analog front-end (AFE) designed for power protection circuits. The ADS131E08EVM-PDK is intended for prototyping and evaluation. This user's guide includes a complete circuit description, schematic diagram, and bill of materials.

Throughout this document, the terms ADS131E08EVM-PDK, demonstration kit, evaluation board, evaluation module, and EVM are synonymous with the ADS131E08EVM.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Table 1. Related Documentation

Device	Literature Number
ADS131E08	SBAS561

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1 ADS131E08EVM Overview

1.1 Information about Cautions

This document contains caution statements. The information in a caution statement is provided for your protection. Be sure to read each caution carefully.

> **CAUTION**
>
> This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

1.2 Introduction

The ADS131E08EVM-PDK is intended for evaluating the ADS131E08 low-power, 24-bit, simultaneously-sampling, eight-channel analog-to-digital converter (ADC). The digital SPI™ control interface is provided by the MMB0 modular EVM motherboard that connects to the ADS131E08 evaluation board. The ADS131E08EVM-PDK is designed to expedite evaluation and system development.

The MMB0 motherboard allows the ADS131E08EVM to be connected to the computer thorugh an available USB port. This manual shows how to use the MMB0 as part of the ADS131E08EVM-PDK, but does not provide technical details about the MMB0.

1.3 Supported Features

Hardware Features:

- Configurable for bipolar or unipolar supply operation
- Configurable for internal and external clock through jumper settings
- Analog test signals can be applied easily using screw terminals

Software Features:

- Analysis tools, including a virtual oscilloscope, histogram, and fast Fourier transform (FFT)
- Access to a variety of register contents, including data rate, PGA options, and more.
- Set ADS131E08 register settings with easy-to-use, graphical user interface (GUI) software

1.3.1 Features Not Supported in Current Version

32 kSPS and 64 kSPS data capture is ***not*** supported by the current version of the firmware.

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1.4 ADS131E08EVM Hardware

Figure 2 shows the hardware included in the ADS131E08EVM kit. Contact the factory at http://e2e.ti.com if any component is missing. Also, it is highly recommended that you check the TI website at http://www.ti.com to verify that you have the latest software.

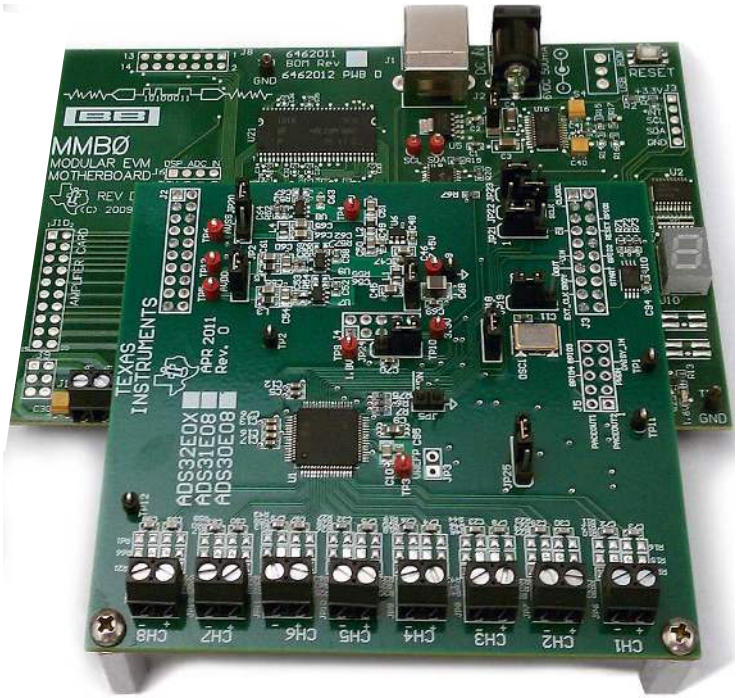

Figure 2. ADS131E08EVM-PDK Kit

The complete kit includes the following items:

- ADS131E08EVM printed-circuit board (PCB)
- MMB0 (modular EVM motherboard)

An external power supply is required to power the MMB0 board. Any supply used to power the MMB0 board through the jack located at J2 must comply with the following requirements:

- Output voltage: 5.5 VDC to 15 VDC
- Maximum output current: ≥ 500 mA
- Output connector: barrel plug (positive center), 2.5-mm I.D. x 5.5-mm O.D. (9-mm insertion depth)
- Complies with applicable regional safety standards

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2 Software Installation

2.1 Minimum Requirements

Before installing the software that is intended for use with the EVM kit, please verify that your PC-compatible computer meets the following minimum requirements:

- Pentium III® or Celeron® processor, 866 MHz or equivalent
- Minimum 256 MB of RAM (512 MB or greater recommended)
- USB 1.1-compatible input
- Hard disk drive with at least 200 MB free space
- Microsoft® Windows® XP operating system with SP2, or Windows 7 operating system
- Mouse or other pointing device
- 1280 × 960 minimum display resolution

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2.2 Installing the Software

CAUTION

Do not connect the ADS131E08EVM hardware before installing the software on a suitable PC. Failure to observe this caution may cause Microsoft Windows to not recognize the ADS131E08EVM.

Download the latest software from the TI website at www.ti.com/tool/ADS131E08EVM-PDK. To install the ADS131E08 software, unzip and run *setup.exe*. Figure 3 shows the initialization screen.

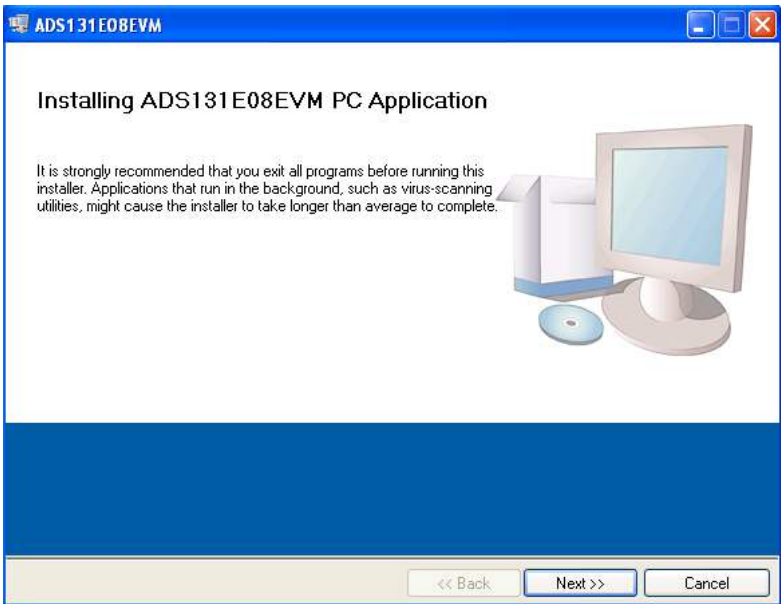

Figure 3. Initialization of ADS131E08EVM GUI

You must accept the two license agreements shown in Figure 4 and Figure 5 before the installation can proceed.

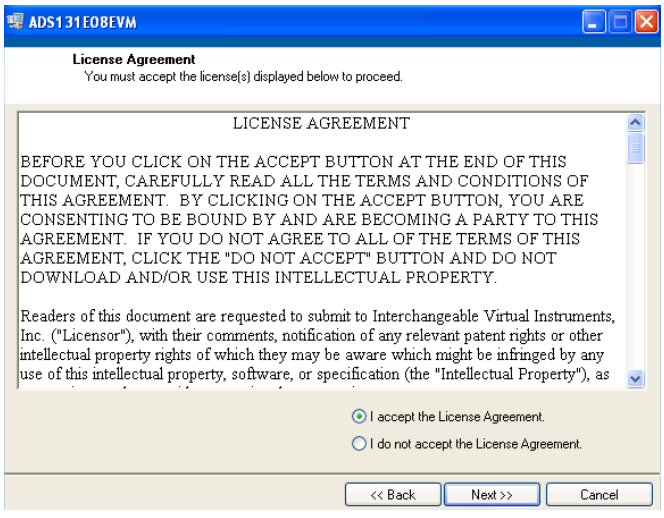

Figure 4. License 1

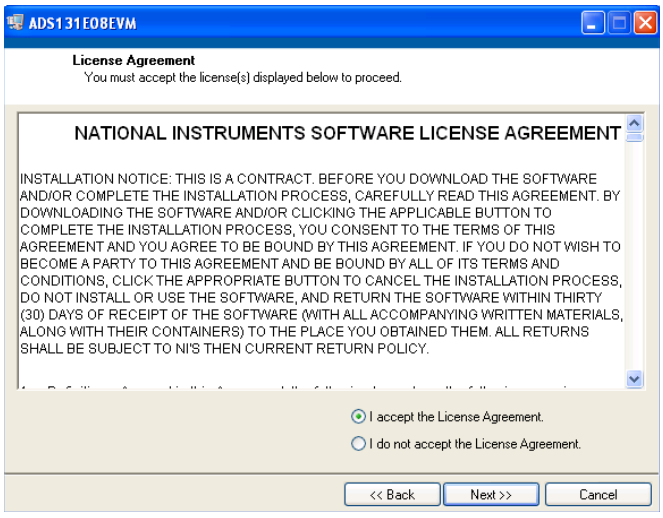

Figure 5. License 2

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2.3 Installing the ADS131E08EVM-PDK Hardware Drivers

2.3.1 Installing the First USB Driver

Apply power to the MMB0 using a power supply as discussed in Section 1.4 and connect the MMB0 to your PC through any available USB port. The *Found New Hardware Wizard* window appears, as shown in Figure 6. Note that this is the first of two USB drivers that are installed. Click *Next* to continue driver installation.

Figure 6. New Hardware Wizard Screen 1

Click *Next* when the screen in Figure 7 appears.

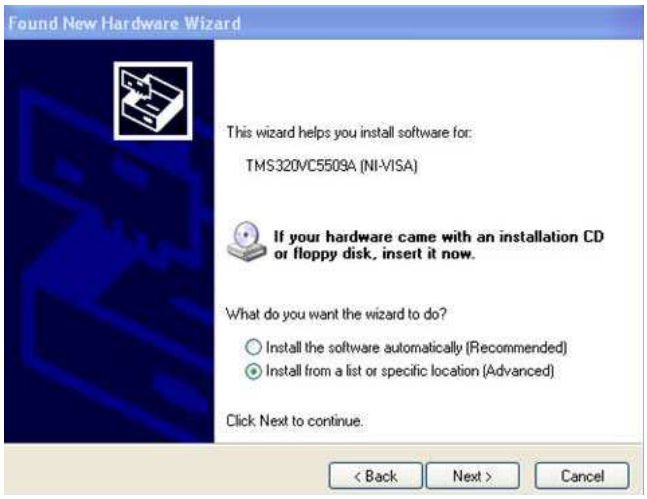

Figure 7. New Hardware Wizard Screen 2

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Navigate to *C:\Program Files\ADS131E08EVM\USB Driver*, as shown in Figure 8.

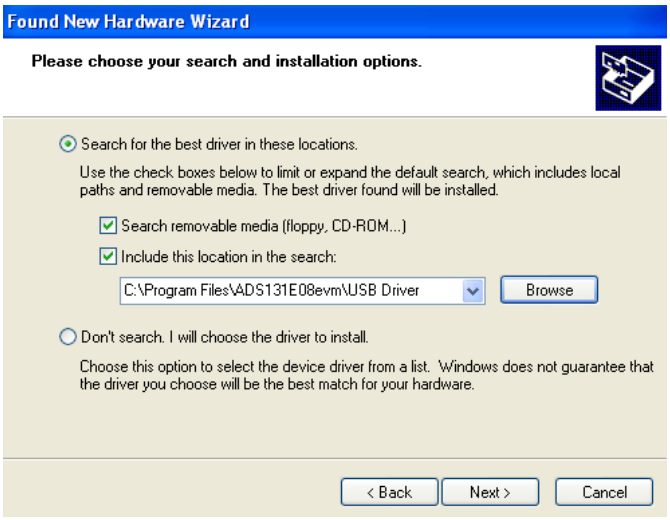

Figure 8. New Hardware Wizard Screen 3

Click *Next* to find and install the driver. When the wizard is complete, the screen in Figure 9 appears.

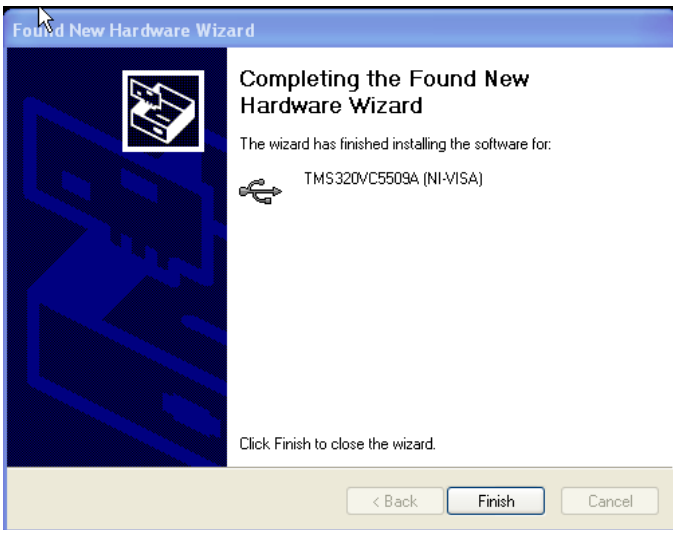

Figure 9. Completion of the First USB Driver

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2.3.2 Installing the Second USB Driver

Launch the ADS131E08EVM-PDK software from the program menu. The software loads and begins downloading firmware to the processor on the MMB0. After the firmware is loaded and running, the *Found New Hardware Wizard* starts again, as shown in Figure 10.

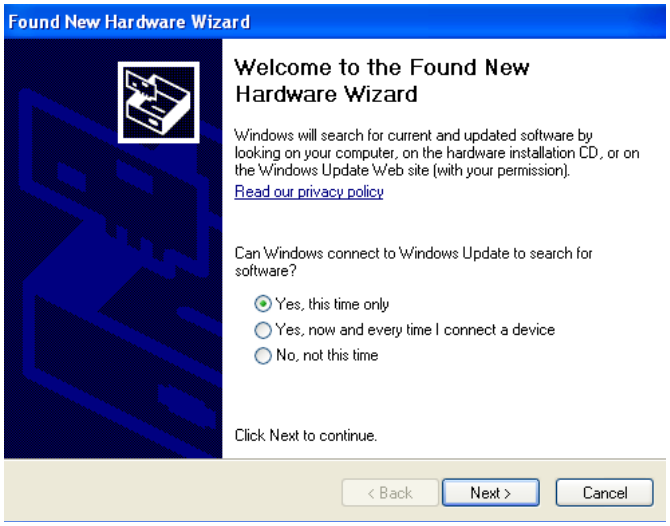

Figure 10. Second New Hardware Wizard Screen

Click *Next* and the screen in Figure 11 appears.

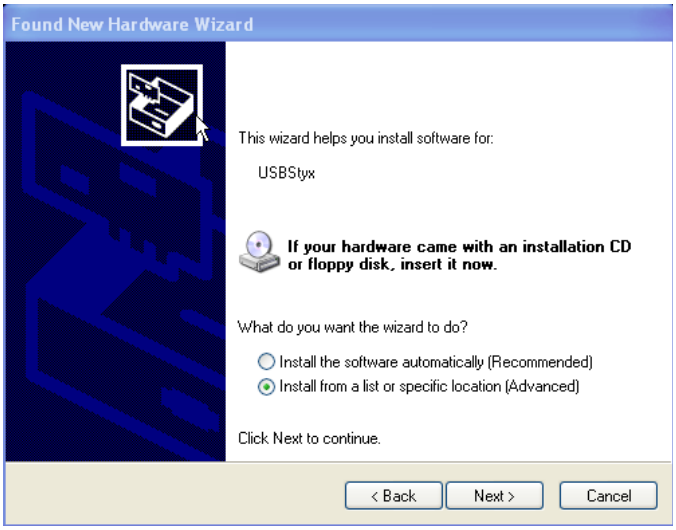

Figure 11. Installing the USBStyx Driver

Click *Next* to complete the installation. If the computer is unable to find the USBStyx driver, point to the installation directory of *C:\Program Files\ADS131E08EVM\USB Drivers*.

At this time, you may receive an error message because the ADS131E08EVM-PDK software has timed out. If so, click *OK*, close the GUI program, power cycle the ADS131E08EVM, and restart the newly installed ADS131E08 evaluation program. This process may need to be repeated if you plug the ADS131E08EVM-PDK into a different USB port on your computer.

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3 ADS131E08EVM Daughter-Card Hardware Overview

CAUTION

Many of the components on the ADS131E08EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling procedures when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses should also be worn.

The ADS131E08EVM-PDK board is a four-layer circuit board. The board layout and schematics are appended to the end of this document.

The ADS131E08EVM-PDK is configured to be used with the TI MMB0 data converter evaluation platform. The key features of the ADS131E08 system on a chip (SOC) are:

- Eight integrated instrumentation amplifiers (INAs) and eight, 24-bit, high-resolution ADCs
- Low power consumption
- Data rates of 1 kSPS, 2 kSPS, 4 kSPS, 8 kSPS, 16 kSPS, 32 kSPS, and 64 kSPS (NOTE: 32 kSPS and 64 kSPS data capture is ***not*** supported by the current version of the firmware).
- 3-V to 5-V unipolar or bipolar analog supply, and 1.8-V to 3-V digital supply
- SPI data interface

The following sections explain some of the hardware settings possible with the EVM for evaluating the ADS131E08 under various test conditions.

3.1 Power Supply

The ADS131E08EVM mounts on the MMB0 board with connectors J1, J2, and J3. The main power supplies (+5 V, +3 V, and +1.8 V) for the front-end board are supplied by the host MMB0 board through connector J3. All other power supplies required for the front-end board are generated onboard by power management devices.

The ADS131E08 operates in unipolar mode using a +3.0-V to +5.0-V analog supply (AVDD/AVSS) and a +1.8-V to +3.3-V digital supply (DVDD), or in bipolar mode using the onboard analog supply (±1.5 V to ±2.5 V). The power consumption of the front-end board is measured by using the JP3 jumper. Power down the ADS131E08 by shorting jumper JP4.

Test points TP4, TP5, TP6, TP7, TP8, TP9, TP10, and TP13 are provided to verify that the host power supplies are correct. The corresponding voltages are shown in Table 2.

Table 2. Power-Supply Test Points

Test Point	Voltage
TP7	+5.0 V
TP4	–4.96 V
TP9	+1.8 V
TP10	+3.3 V
TP5	+3.0 V
TP13	+2.5 V
TP6	–2.5 V
TP8	GND

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The front-end board must be properly configured in order to achieve the various power-supply schemes. The default power-supply setting for the ADS131E08EVM is a bipolar analog supply of ±2.5 V, and there are onboard options to switch to a unipolar analog supply of +3 V. The digital supply (DVDD) is selectable to either +3.3 V or +1.8 V. Table 3 shows the board and component configurations for each analog power-supply scheme. Table 4 shows the board configurations for the digital supply. Note that the EVM is shipped with the analog supply set to ±2.5 V and digital supplies set to 3.3 V.

Table 3. Analog Supply Configurations

AVDD and AVSS	Unipolar Analog Supply		Bipolar Analog Supply	
	3 V	5 V	±1.5 V	±2.5 V
JP7	1-2	1-2	2-3	2-3
JP1	2-3	2-3	1-2	1-2
U6	TPS73230	TPS73250	Don't care	Don't care
U8	Don't care	Don't care	TPS73201	TPS73201
U7	Don't care	Don't care	TPS72301	TPS72301
R61	Don't care	Don't care	21 kΩ	47.5 kΩ
R62	Don't care	Don't care	78.7 kΩ	43.2 kΩ
R59	Don't care	Don't care	23.3 kΩ	49.9 kΩ
R60	Don't care	Don't care	95.3 kΩ	46.4 kΩ
C48, C54, C59	Not installed	Not installed	Not installed	Not installed

Table 4. Digital Supply Configurations (DVDD and DGND)

DVDD	3.3 V	1.8 V
JP11	2-3	1-2

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3.2 Clock

The ADS131E08 has an on-chip oscillator circuit that generates a 2.048-MHz clock (nominal). This clock can vary by ±5% over temperature. For applications that require higher accuracy, the ADS131E08 can also accept an external clock signal. The ADS131E08 provides an option to test both internal and external clock configurations. It also provides an option to generate the external clock from either the onboard oscillator or from an external clock source.

The onboard oscillator is powered by the DVDD supply of the ADS131E08. Care must be taken to ensure that the external oscillator can operate either with +1.8 V or +3.3 V, depending on the DVDD supply configuration. Table 5 shows the jumper settings for the three options for the ADS131E08 clocks.

Table 5. CLK Jumper Options

ADS131E08 Clock	Internal Clock	External OSC Clock	External Clock
JP5	Not installed	2-3	1-2
JP6	Don't care	1-2 (disable)	Don't care
J4 - pin 10	Don't care	Don't care	Clock source

A 2.048-MHz oscillator available for the +3.3-V DVDD supply is the FXO-HC735-2.048MHz. For a +1.8-V DVDD supply, use the SiT8002AC-34-18E-2.048. The EVM is shipped with the external oscillator enabled.

3.3 Reference

The ADS131E08 has an on-chip internal reference circuit that provides reference voltages to the device. Alternatively, the internal reference can be powered down and VREFP can be applied externally. This configuration is achieved with the external reference generators (U2 and U3) and driver buffer. These components (U2, U3, and U4) must be installed by the user; they are not installed at the factory. The external reference voltage can be set to either 4.096 V or 2.5 V, depending on the analog supply voltage. Measure TP3 to make sure the external reference is correct and stable. The settings for the external reference is described in Table 6. This table assumes REF5025 is installed at U2 and REF5040 at U3. A low-noise amplifier like the OPA350 can be installed at U4.

Table 6. External Reference Jumper Options

ADS131E08 Reference	Internal Reference	External Reference	
	VREF = 2.5 V	VREF = 4.096 V	VREF = 2.5 V
JP12	Don't care	2-3	1-2
JP2	Not installed	Installed	Installed

3.3.1 Accessing ADS131E08 Analog Supplies

Some ADS131E08 output signals are provided as test points for probing purposes using J4 (not installed on the board). Table 7 lists the various test signals with the corresponding test points.

Table 7. Auxiliary Connector Test Signals and Test Points

Signal	J4 Pin Number		Signal
Not connected	1	2	GPIO1
Not connected	3	4	GPIO2
PWDN	5	6	GPIO3
Dasiy in	7	8	GPIO4
AGND	9	10	Not connected

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3.3.2 Accessing ADS131E08 Digital Supplies

The ADS131E08 digital signals (including SPI signals, some GPIO signals, and some control signals) are available at connector J1. These signals are used to interface to the MMB0 board DSP. The pinout for this connector is shown in Table 8.

Table 8. Serial Interface Pinout

Signal	J1 Pin Number		Signal
START/CS	1	2	CLKSEL
CLK	3	4	GND
NC	5	6	GPIO1
CS	7	8	RESET
NC	9	10	GND
DIN	11	12	GPIO2
DOUT	13	14	NC/START
DRDY	15	16	SCL
EXT_CLK	17	18	GND
NC	19	20	SDA

3.4 Analog Inputs

The ADS131E08 provides users the option to feed in signals from any arbitrary signal source directly. Analog signals can be applied at terminal blocks J5 through J12.

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4 Using the Software

The software GUI contains a *Save to File* feature (located in the *Save* tab) that allows all data from any combination of channels, along with notes to describe the data, to be saved to a specified directory. This data can then be read back using a text editor. Saving the data in this format can be completed by clicking the *Save to File* button, as shown in Figure 12.

An additional option in the evaluation software allows register configurations to be saved to a file that can be reloaded to the GUI. To create a configuration file with all of the stored register settings, use the *Save Configuration Settings* option, found in the *File* menu at the top left-hand corner of the GUI. This configuration file can be reloaded to the GUI using the *Load Configuration Setting*s option found in the same *File* menu.

Figure 12 shows the options available in the *Save* tab.

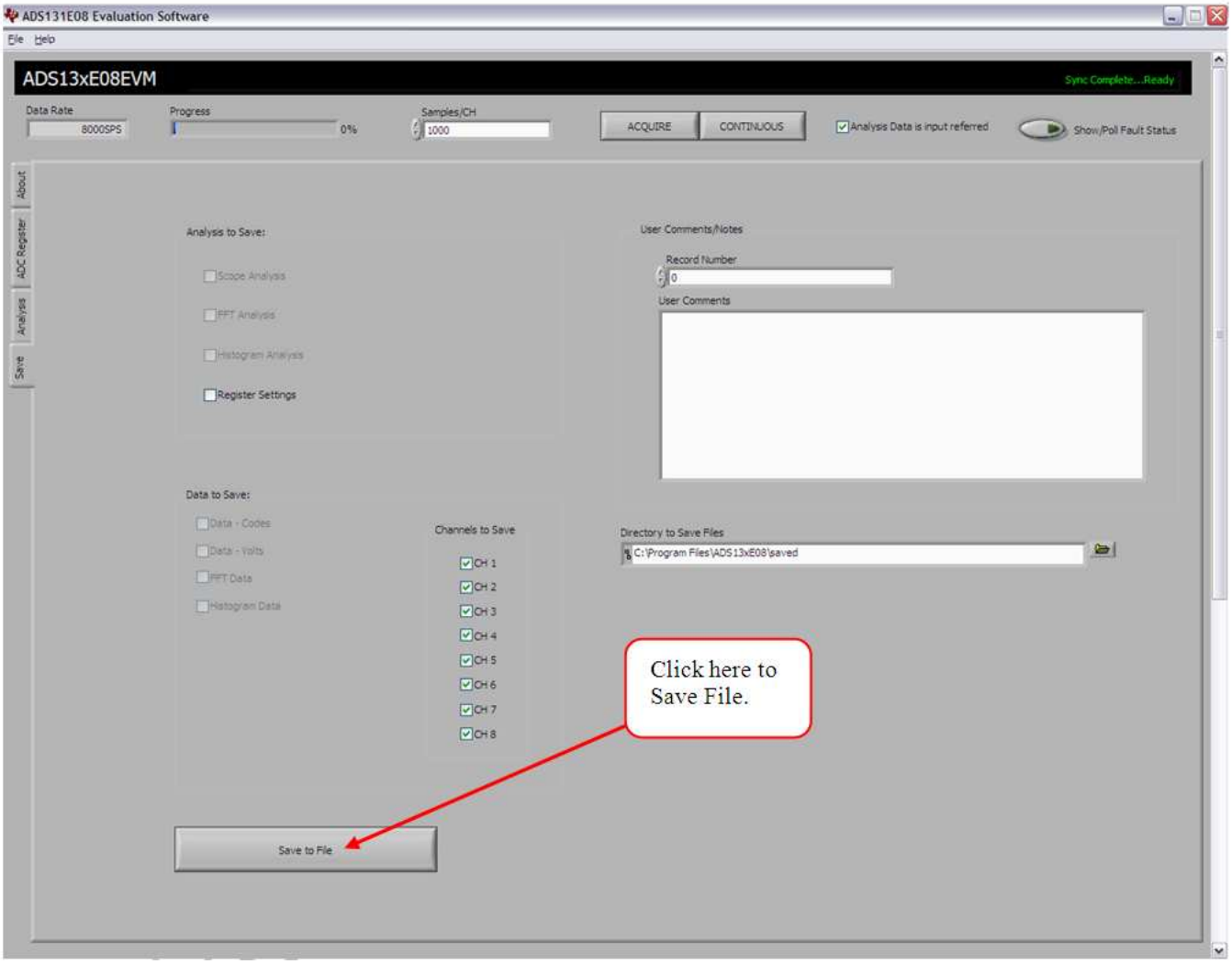

Figure 12. File Save Option Under Save Tab

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4.1 Software Overview

This section provides a quick overview of the various features and functions of the ADS131E08EVM software package.

There are four tabs across the left side of the GUI; from top to bottom, they are:

- **About:** Provides information about the EVM and software version revisions.
- **ADC Register:** Includes all of the control registers for the ADS131E08 in a series of related subtabs:
  - Channel Registers
  - GPIO
  - Register Map
- **Analysis:** Provides different ways to analyze captured data, in the time or frequency domain, using the following subtabs:
  - Scope
  - Histogram
  - FFT
- **Save:** Provides options for saving acquired data

4.2 Global Channel Registers

The *Channel Registers* tab provides access to the ADS131E08 configuration and fault threshold registers. The Global Channel Registers tab has the following options:

- **Configuration Register 1:** Controls daisy-chain and multiple readback (MRB) modes, the CLKOUT connection, and the output data rate. Note that the 32 kSPS and 64 kSPS data rates provide 16-bit data (***not*** supported by the current version of the firmware), and the 1 kSPS, 2 kSPS, 4 kSPS, 8 kSPS, and 16 kSPS data rates are 24 bits wide.
- **Configuration Register 2:** Controls the internal test source, along with the test-signal amplitude and frequency.
- **Configuration Register 3:** Controls the reference buffer power-down control, the reference voltage, and the op amp buffer control.
- **Fault Control Register:** Sets the comparator threshold level for fault.

Figure 13 shows the GUI panel to manipulate these registers and the respective settings for each.

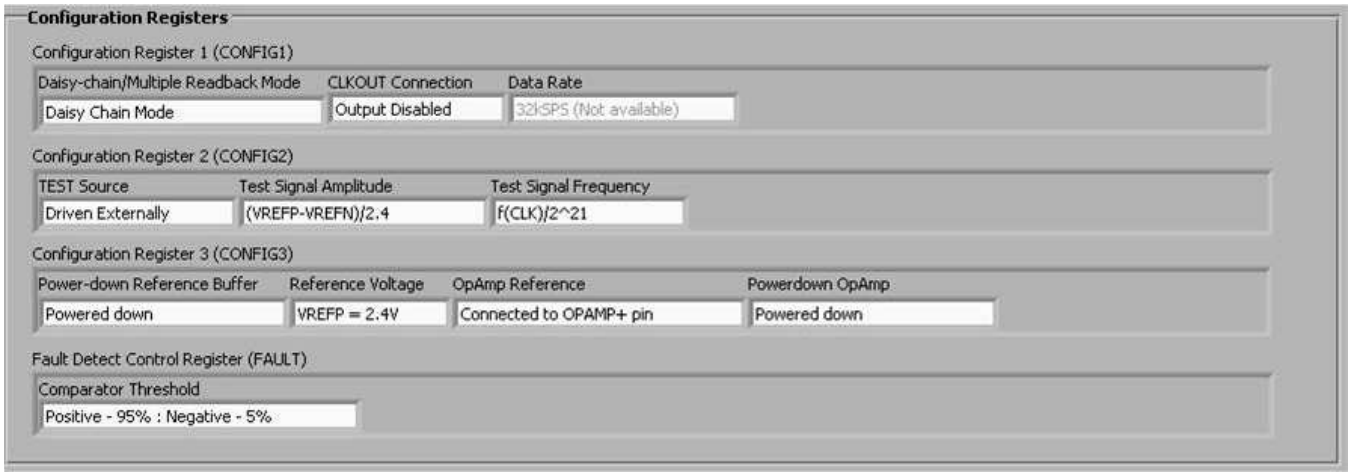

Figure 13. Channel Registers GUI for the Configuration Registers

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4.3 Channel Control Registers

The second section under the Channel Registers tab is the Channel Control Registers box. This panel allows the user to uniquely configure the front-end multiplexer (mux) for each channel. Additionally, at the top of the Channel Control Registers box is the option to globally set all channels to the same setting. Table 9 lists the register map. The channel-specific mux is illustrated in Figure 14, and the all-channel-specific mux is shown in Figure 15.

Table 9. Register Assignments: Channel-Specific Settings

Address	Register	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Channel-Specific Settings										
05	CH1SET	00	PD1	GAIN12	GAIN11	GAIN10	0	MUXn2	MUXn1	MUXn0
06	CH2SET	0	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07	CH3SET	0	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08	CH4SET	0	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09	CH5SET	0	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0A	CH6SET	0	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0B	CH7SET	0	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0C	CH8SET	0	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80

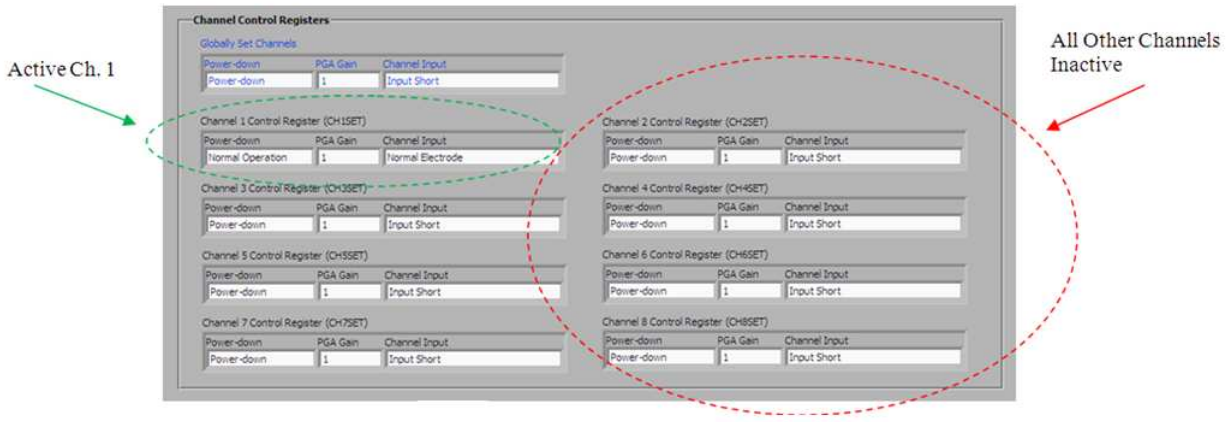

Figure 14. Channel Control Register GUI Panel: Single Channel Enabled

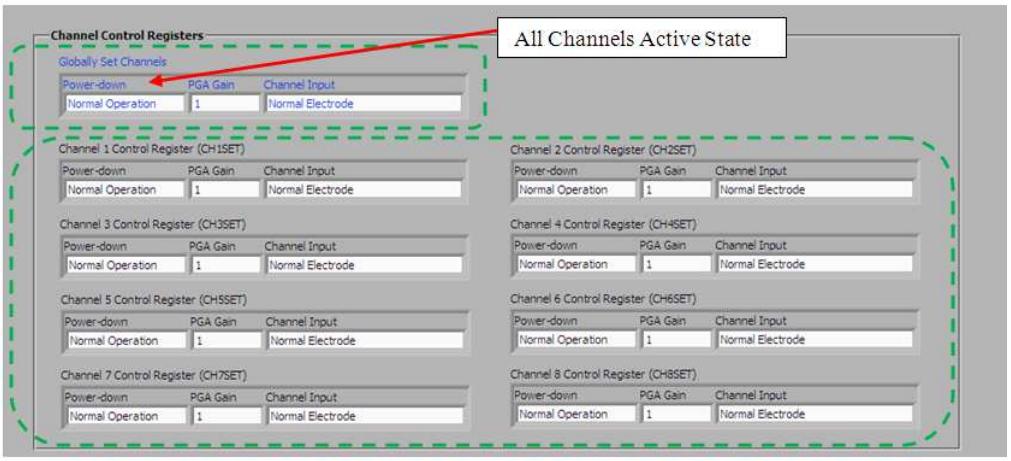

Figure 15. Channel Control Registers GUI Panel: All Channels Enabled

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4.4 Internal Test Signals Input and the Scope Display Tab

Configuration Register 2 controls the signal amplitude and frequency of an internally-generated square wave test signal. The primary purpose of this test signal is to verify the functionality of the front-end mux, the programmable gain amplifier (PGA), and the ADC. The test signals may be viewed on the *Analysis→Scope Display* tab, as Figure 16 shows.

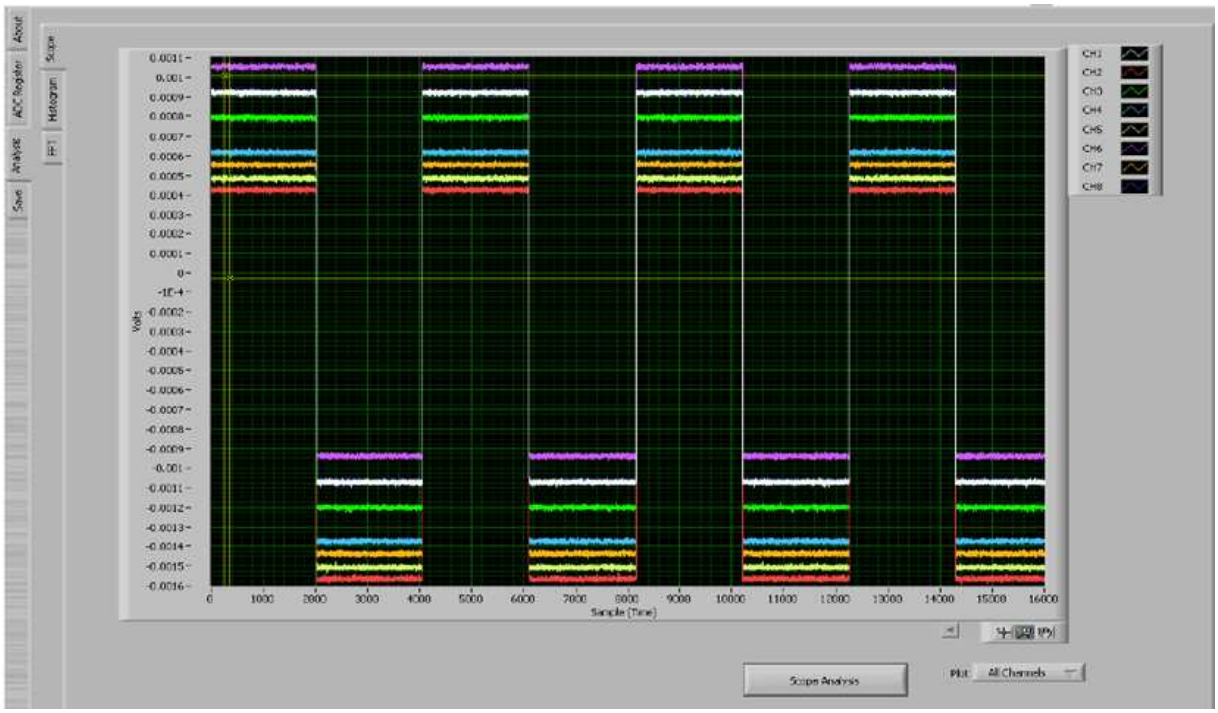

Figure 16. Example of Internal Test Signals Viewed on the Scope Display Tab

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4.5 Temperature Sensor and the Scope Display Tab

The internal temperature sensor on the ADS131E08 is shown in Figure 22.

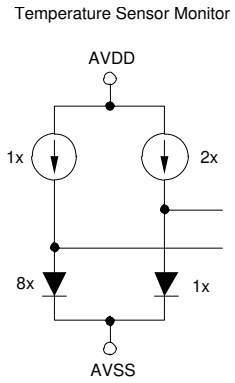

Figure 17. Internal Temperature Sensor

When the internal mux is routed to the temperature sensor input, the output voltage of the ADC may be converted to a temperature value using Equation 1:

$$\text{Temperature (°C)} = \left\{ \frac{\text{Temperature Readnig } (\mu\text{V}) - 145{,}300\ \mu\text{V}}{490\ \mu\text{V/°C}} \right\} + 25°\text{C} \tag{1}$$

The output voltage corresponding to a given temperature can be read by running a data acquisition after the *Temperature Sensor* mux option is selected, as shown in the *Channel Control Registers* section. Figure 18 demonstrates an example of temperature sensor readings read back using the GUI.

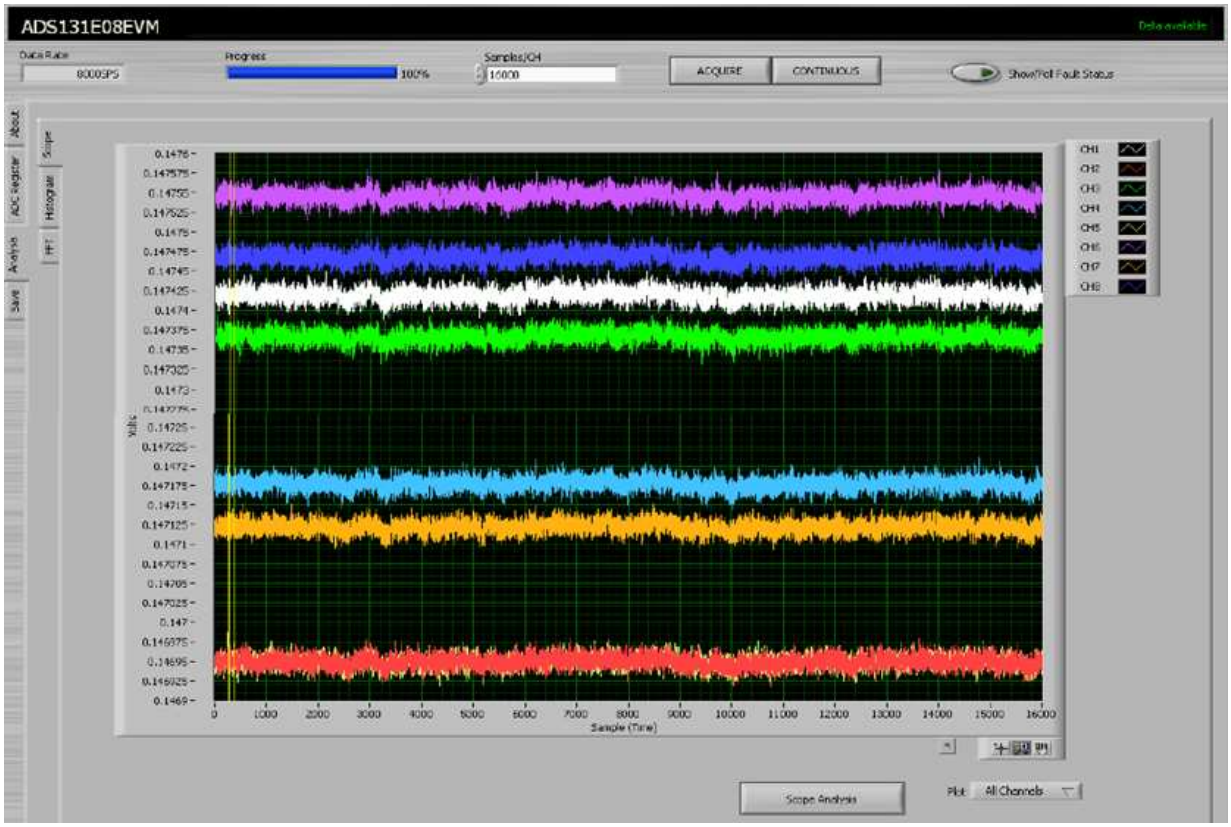

Figure 18. Eight-Channel Read of Internal Temperature Data

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The number 0.1447 V (on the y-axis) can be calculated as a temperature using Equation 2:

$$\text{Temperature (°C)} = \left[\frac{0.1447 - 0.145300}{0.00049}\right] + 25 = 23.78°C \quad (2)$$

4.5.1 MV_{DD} Input and the Scope Tab

The MV_{DD} input option allows the measurement of the supply voltage V_S = (AVDD + AVSS) / 2 for channels 1, 2, 5, 6, 7, and 8; however, the supply voltage for channel 3 is DVDD / 2.

4.6 General-Purpose I/O Register (GPIO)

The GPIO registers control four general-purpose input and output (I/O) pins. Table 10 shows the respective register to control these pins. Figure 19 illustrates the GPIO Control Register GUI panel.

Table 10. GPIO: General-Purpose I/O Register

Address	Register	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14h	GPIO	0Fh	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

Figure 19. GPIO Control Register GUI Panel

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4.7 Fault Status Registers (FAULT_STATP and FAULT_STAIN)

The Fault Status registers store the status of whether the positive and/or negative input on each channel has a fault. This is a convenient feature to help pinpoint if any of the inputs are out of range. The GUI for this feature is enabled by clicking in the upper right-hand corner of the EVM software on the *Show/Poll Fault Status* button, as shown in Figure 20.

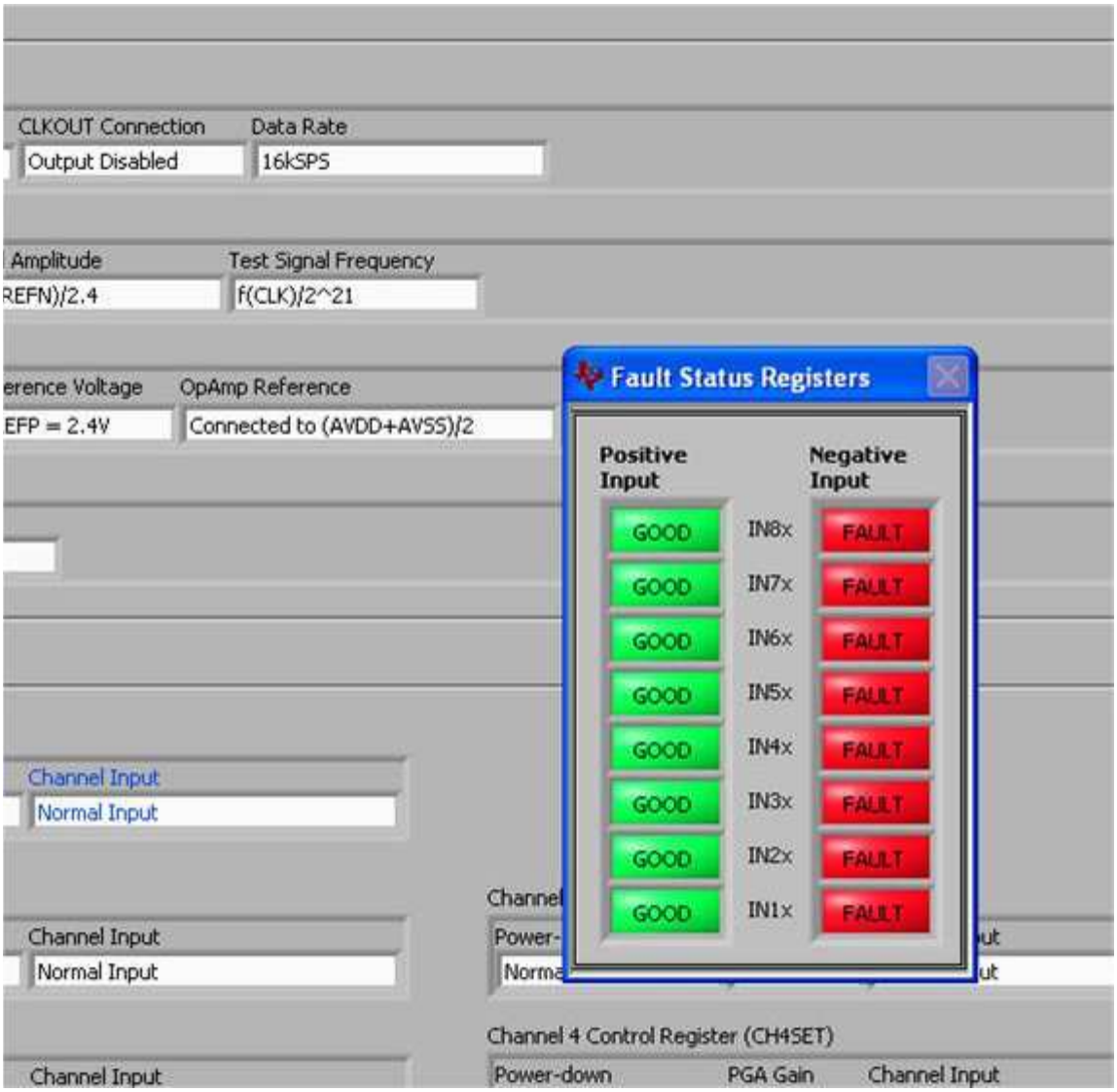

Figure 20. Fault Status Indicator

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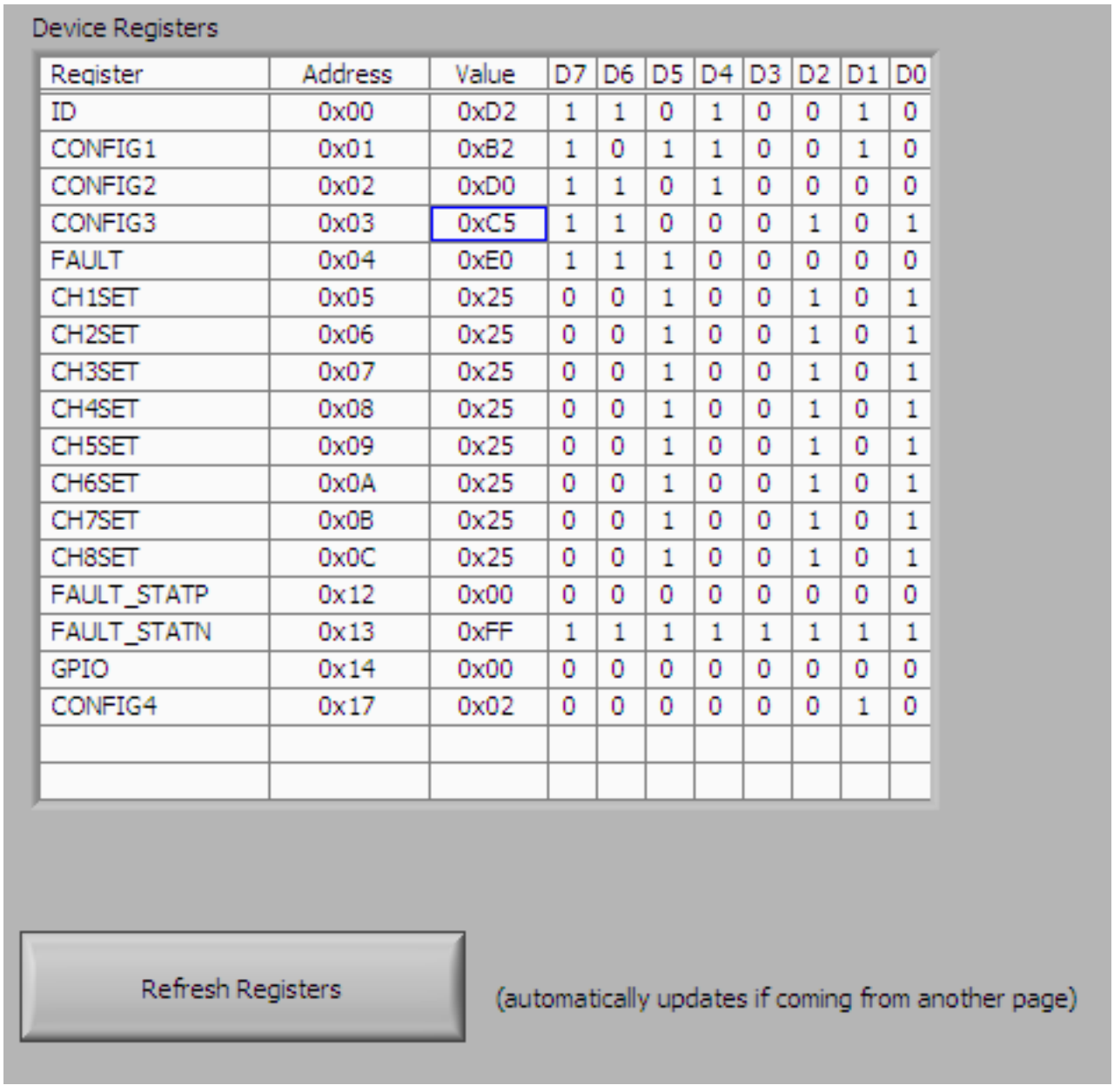
4.8 Register Map

The *Register→Device Register* tab is a helpful debug feature that allows the user to view the state of all the internal registers. This tab is shown in Figure 21.



Register	Address	Value	D7	D6	D5	D4	D3	D2	D1	D0
ID	0x00	0xD2	1	1	0	1	0	0	1	0
CONFIG1	0x01	0xB2	1	0	1	1	0	0	1	0
CONFIG2	0x02	0xD0	1	1	0	1	0	0	0	0
CONFIG3	0x03	0xC5	1	1	0	0	0	1	0	1
FAULT	0x04	0xE0	1	1	1	0	0	0	0	0
CH1SET	0x05	0x25	0	0	1	0	0	1	0	1
CH2SET	0x06	0x25	0	0	1	0	0	1	0	1
CH3SET	0x07	0x25	0	0	1	0	0	1	0	1
CH4SET	0x08	0x25	0	0	1	0	0	1	0	1
CH5SET	0x09	0x25	0	0	1	0	0	1	0	1
CH6SET	0x0A	0x25	0	0	1	0	0	1	0	1
CH7SET	0x0B	0x25	0	0	1	0	0	1	0	1
CH8SET	0x0C	0x25	0	0	1	0	0	1	0	1
FAULT_STATP	0x12	0x00	0	0	0	0	0	0	0	0
FAULT_STATN	0x13	0xFF	1	1	1	1	1	1	1	1
GPIO	0x14	0x00	0	0	0	0	0	0	0	0
CONFIG4	0x17	0x02	0	0	0	0	0	0	1	0

Figure 21. Device Register Settings

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5 ADS131E08 Analysis Tools

Under the *Analysis* tab in the ADS131E08 GUI software, there are three different analysis tools available that enable a detailed examination of the signals selected by the front-end mux:

- Scope
- Histogram
- FFT

5.1 Scope Tool

The *Scope* tool, available under the *Analysis* tab, is a very useful means of examining the data results in the time domain. Users can decide if they would like their data displayed as input-referred or not, as well as review the details of the converted data to ensure that the data meets expectations. Figure 22 shows the scope tool features.

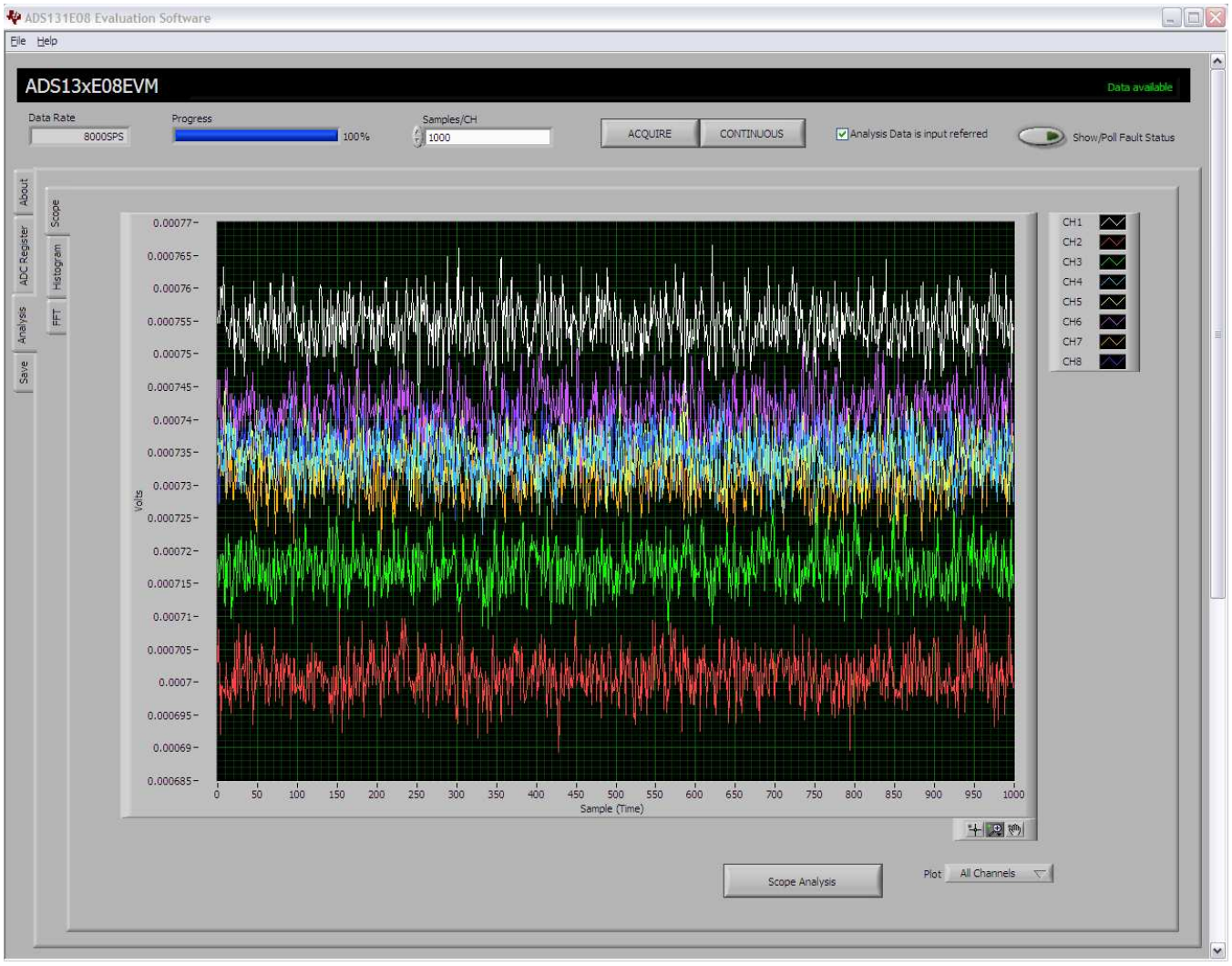

Figure 22. Scope Tool Features

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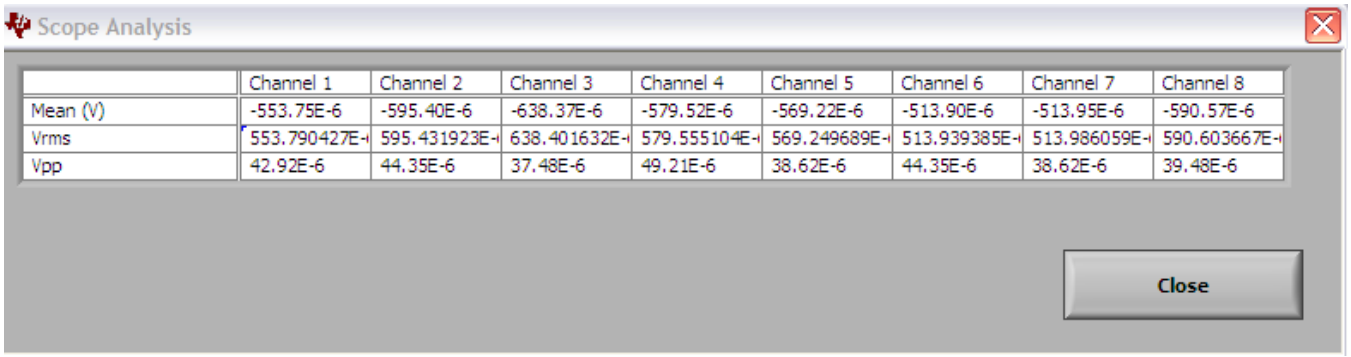
5.1.1 Scope Analysis Button

The *Scope Analysis* button opens a pop-up window that displays the mean voltage, root mean square (RMS) voltage, and peak-to-peak voltage for noise analysis. Figure 23 shows an example of this window.



	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
Mean (V)	-553.75E-6	-595.40E-6	-638.37E-6	-579.52E-6	-569.22E-6	-513.90E-6	-513.95E-6	-590.57E-6
Vrms	553.790427E-6	595.431923E-6	638.401632E-6	579.555104E-6	569.249689E-6	513.939385E-6	513.986059E-6	590.603667E-6
Vpp	42.92E-6	44.35E-6	37.48E-6	49.21E-6	38.62E-6	44.35E-6	38.62E-6	39.48E-6

Figure 23. Scope Analysis Tab (Noise Levels for Each Channel Shown)

5.1.2 Waveform Examination Tool

The waveform examination tool allows the user to either zoom in on all channels simultaneously, or on just a single channel. Figure 24 shows an example of the waveform examination tool.

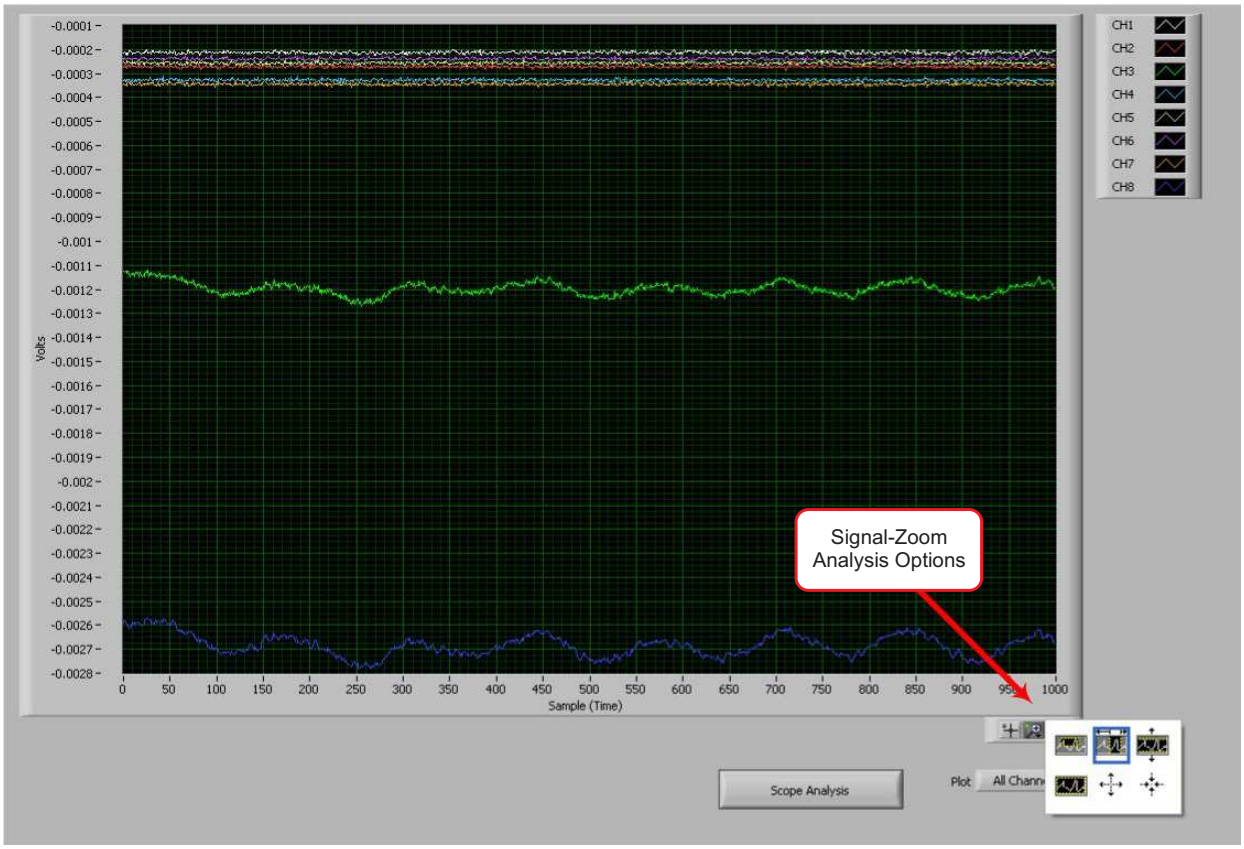


Figure 24. Zoom Option on the Waveform Examination Tool

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5.2 Histogram Tool

The *Histogram* subtab displays the data in a histogram format for the eight channels. The data set is arranged in the total number of histogram bins set within the tab following acquisition. The screen shot shown in Figure 25 illustrates the histogram output for an input shorted signal. The same signal-zoom analysis shown in the previous section may be used on the histogram plots for a more detailed examination of the amplitude bins.

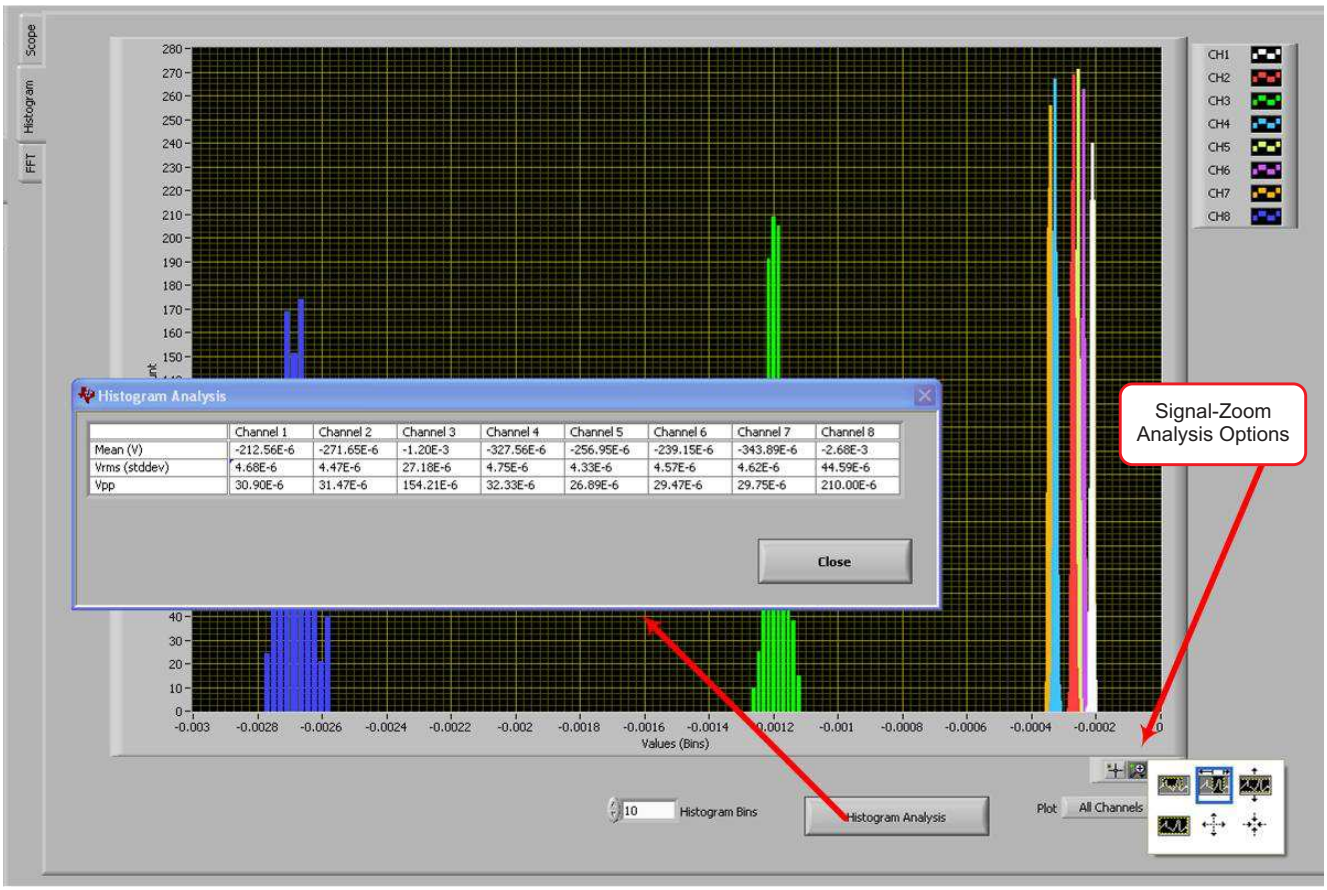

Figure 25. Histogram Bins

The *Histogram Analysis* button can be used to view the mean voltage, standard deviation used for the RMS voltage, and peak-to-peak voltage for analysis, as shown in Figure 26.

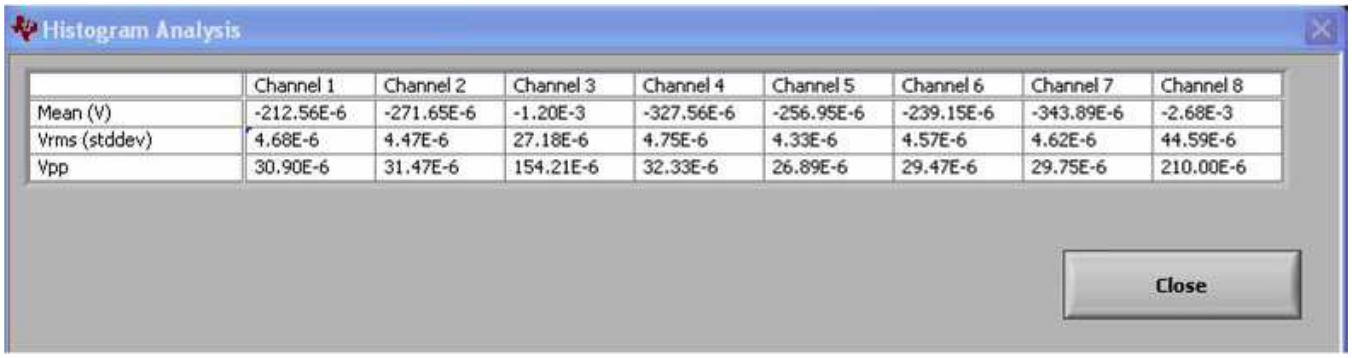

Figure 26. Statistics for the Signal Amplitude of Eight Channels

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5.3 FFT Tool

The *FFT* subtab displays the data in the frequency domain by performing an FFT on the eight channels. Details of the FFT, including SNR, THD, and more, can be viewed using the *FFT Analysis* button located at the bottom of the display. Figure 27 shows the FFT display.

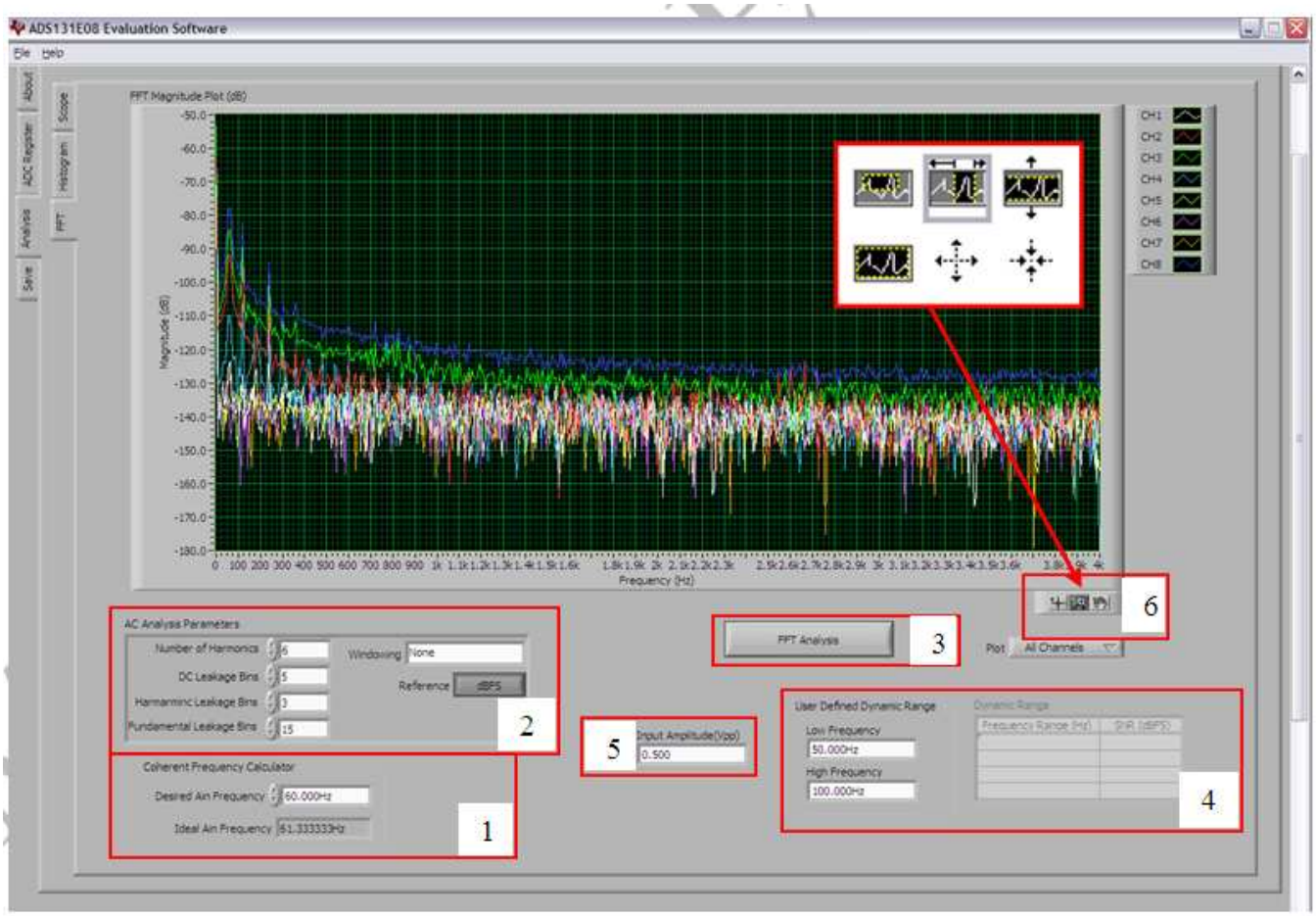

Figure 27. Analysis→FFT Graph of Normal Electrode Configuration

5.3.1 Coherent Frequency Calculator

The red box labeled *1* in Figure 27 shows the Coherent Frequency Calculator. Coherent sampling in an FFT is defined in Equation 3:

$$\frac{f_{AIN}}{f_{SAMPLE}} = \frac{N_{WINDOW}}{N_{TOTAL}} \quad (3)$$

where:

- f_{AIN} = input frequency
- f_{SAMPLE} = ADS131E08 sampling frequency
- N_{WINDOW} = number of odd integer cycles during a given sampling period
- N_{TOTAL} = number of data points (in power of 2) that is used to create the FFT.

If the conditions for coherent sampling can be met, the FFT results for a periodic signal are optimized. The ideal A_{IN} frequency is a value that is calculated based on the sampling rate so that the coherent sampling criteria can be met.

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5.3.2 AC Analysis Parameters

The *AC Analysis Parameters* portion of the FFT tool (red box 2 in Figure 27) is used to dictate the number of harmonics, dc leakage bins, harmonic leakage bins, and fundamental leakage bins that are used in the creation of various histograms. Press the *Windowing* button, shown in in Figure 28, to evaluate the FFT graph under a variety of different windowing options. Pressing the *Reference* button toggles between dBFS (decibels, full-scale) and dBc (decibels to carrier).

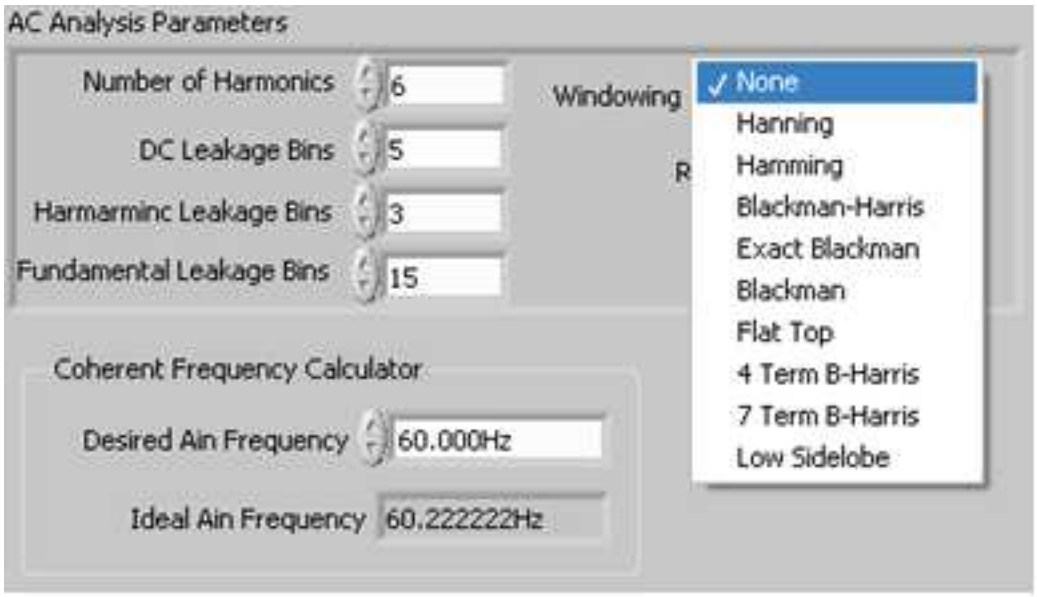
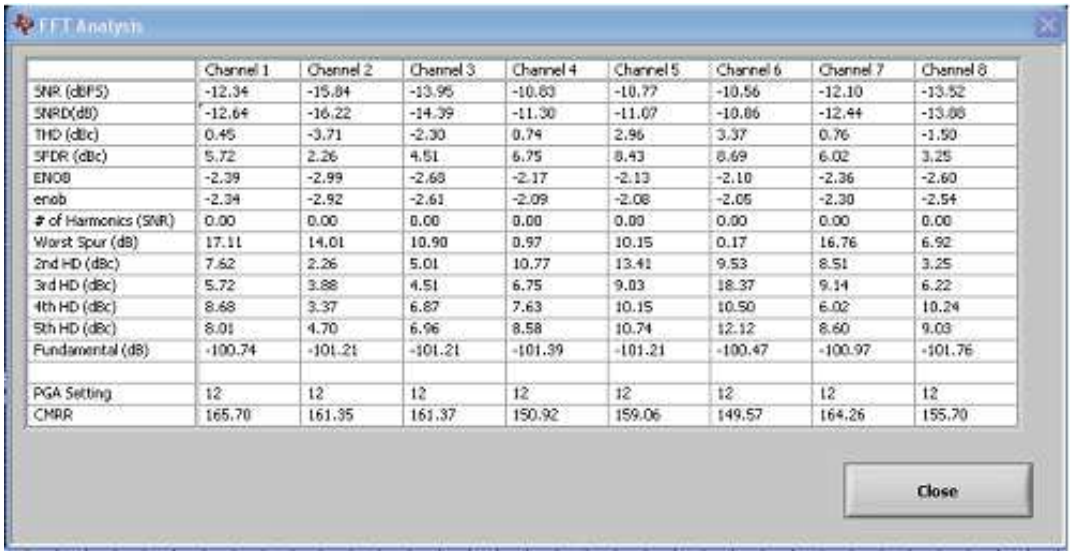


Figure 28. Analysis→FFT→AC Analysis Parameters: Windowing Options

5.3.3 FFT Analysis

The *FFT Analysis* button (red box 3, Figure 27) pulls up the window shown in Figure 29. This window displays the ac details of the data set after it is viewed in the frequency domain. The SNR, THD, and harmonic information is listed in a table format.



	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
SNR (dBFS)	-12.34	-15.84	-13.95	-10.83	-10.77	-10.56	-12.10	-13.52
SNRD(dB)	-12.64	-16.22	-14.39	-11.30	-11.07	-10.86	-12.44	-13.88
THD (dBc)	0.45	-3.71	-2.30	0.74	2.96	3.37	0.76	-1.50
SFDR (dBc)	5.72	2.26	4.51	6.75	8.43	8.69	6.02	3.25
ENOB	-2.39	-2.99	-2.68	-2.17	-2.13	-2.10	-2.36	-2.60
enob	-2.34	-2.92	-2.61	-2.09	-2.08	-2.05	-2.30	-2.54
# of Harmonics (SNR)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Worst Spur (dB)	17.11	14.01	10.90	0.97	10.15	0.17	16.76	6.92
2nd HD (dBc)	7.62	2.26	5.01	10.77	13.41	9.53	8.51	3.25
3rd HD (dBc)	5.72	3.88	4.51	6.75	9.03	18.37	9.14	6.22
4th HD (dBc)	8.68	3.37	6.87	7.63	10.15	10.50	6.02	10.24
5th HD (dBc)	8.01	4.70	6.96	8.58	10.74	12.12	8.60	9.03
Fundamental (dB)	-100.74	-101.21	-101.21	-101.39	-101.21	-100.47	-100.97	-101.76
PGA Setting	12	12	12	12	12	12	12	12
CMRR	165.70	161.35	161.37	150.92	159.06	149.57	164.26	155.70

Figure 29. Analysis→FFT→FFT Analysis: Input Short Condition

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5.3.4 User-Defined Dynamic Range

This portion of the FFT tool (red box 4, Figure 27) is used to examine the SNR of a specific channel within a given frequency band defined by the *Low Frequency* and *High Frequency* fields. The SNR displayed in this window also appears under the *Dynamic Range* heading, as shown in Figure 30.

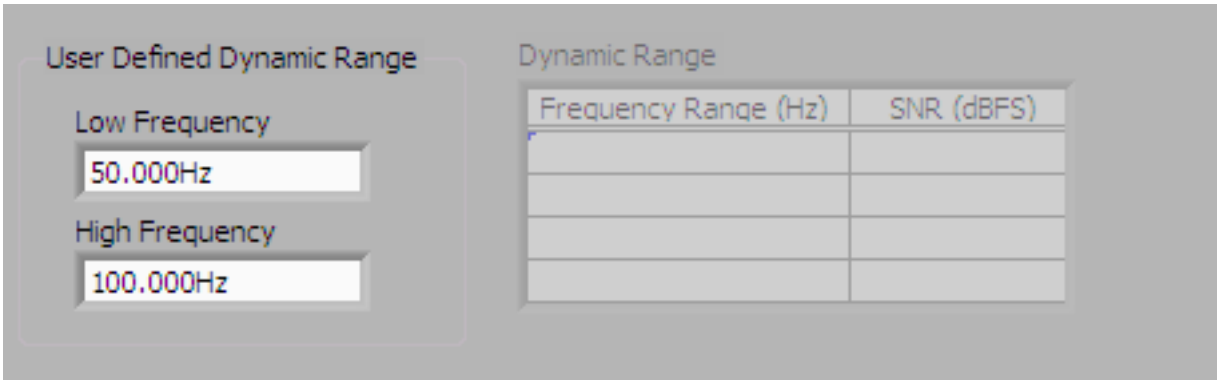

Figure 30. Changing the User-Defined Dynamic Range for Channel 1

5.3.5 Input Amplitude (V_{PP})

The *Input Amplitude* field (red box 5, Figure 27) is a user input that is important for accurately calculating the CMRR of each channel.

5.3.6 Waveform Zoom

This zoom function allows a closer examination of the FFT at frequencies of interest, as shown in Figure 31.

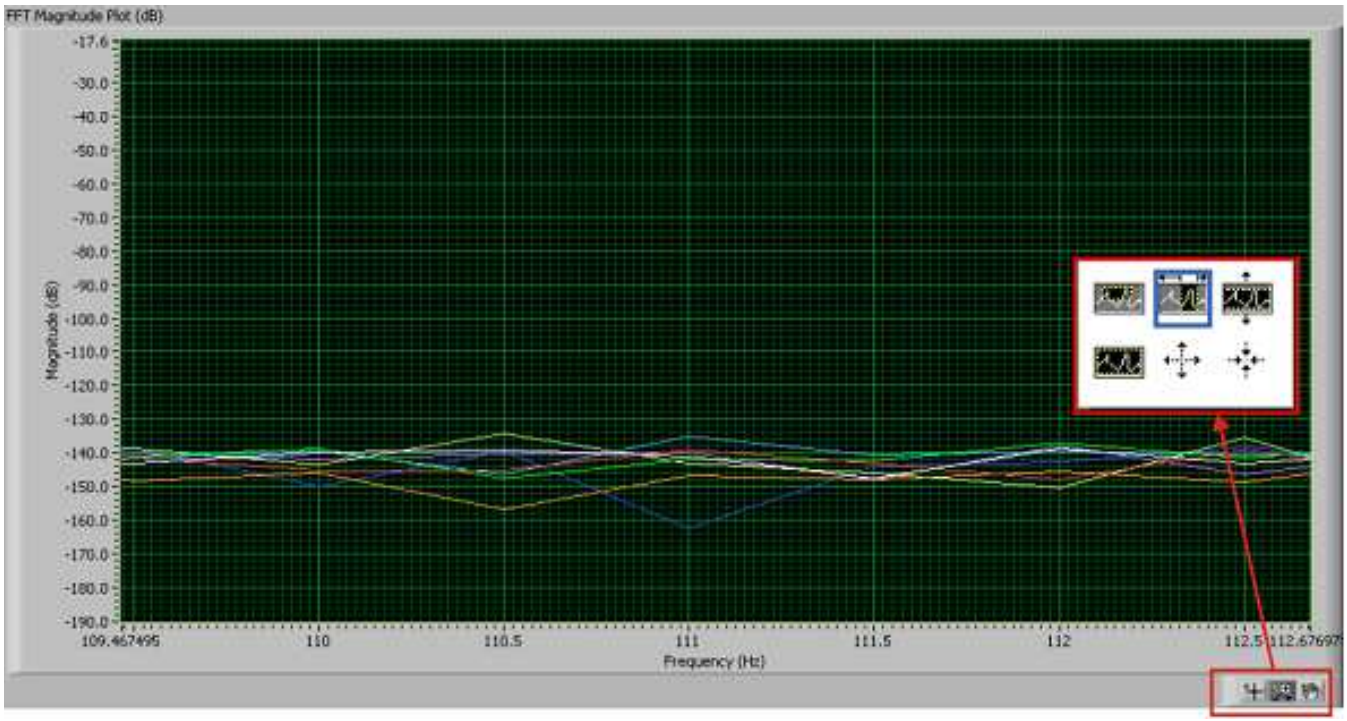

Figure 31. FFT Plot Using Waveform Zoom Function

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6 Bill of Materials (BOM), Layout, and Schematic

This section contains the complete BOM, printed circuit board (PCB) layouts, and schematic diagrams for the ADS131E08.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS131E08 PCBs.

6.1 Bill of Materials

Table 11 lists the bill of materials for the ADS131E08.

Table 11. ADS131E08 Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer	Part Number
1	1	N/A	Printed Circuit Board	TI	6527354
2	15	C1, C2, C3, C4, C5, C6, C11, C17, C39, C40, C41, C44, C50, C68, C69	CAP CER 1UF 25V 10% X5R 0603	Murata	GRM188R61E105KA12D
3	0	C7, C8, C15, C19, C26, C28, C30, C32, C33, C34, C35, C36, C48, C54, C59	Not Installed		
4	1	C9	CAP CER 22UF 6.3V 10% X5R 0805	Taiyo Yuden	JMK212BJ226KG-T
5	11	C10, C37, C38, C42, C43, C46, C47, C52, C53, C57, C58	CAP CER 10UF 10V 10% X5R 0805	Murata	GRM219R61A106KE44D
6	10	C12, C13, C14, C16, C18, C49, C61, C62, C75, C76	CAP CER 0.1UF 50V 10% X7R 0603	Murata	GRM188R71H104KA93D
7	16	C20, C21, C22, C23, C24, C64, C65, C66, C67, C70, C71, C72, C73, C74, C77, C78	CAP CER 470PF 50V C0G 5% 0603	TDK	C1608C0G1H471J
8	0	C25, C27, C29	Not Installed		
9	0	C31	Not Installed		
10	4	C45, C51, C55, C56	CAP CER 2.2UF 6.3V 10% X5R 0603	Murata	GRM185R60J225KE26D
11	2	C60, C63	CAP CER 100UF 10V 20% X5R 1210	Taiyo Yuden	LMK325BJ107MM-T
12	0	D1–D16	Not Installed		
13	1	J1 (Top side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
14	1	J1, J2 (Bottom side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
15	1	J3 (Bottom side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
16	0	J4	Not Installed		
17	8	J5–J12	TERMINAL BLOCK 3.5MM 2POS PCB	On Shore	ED555/2DS
18	8	JP1, JP5–JP11	3 Position Jumper _ .1" spacing	Samtec	TSW-103-07-T-S
19	0	JP2	Not Installed		
20	2	JP3, JP4	2 Position Jumper _ .1" spacing	Samtec	TSW-102-07-T-S
21	0	JP12	Not Installed		

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Table 11. ADS131E08 Bill of Materials (continued)

Item	Qty	Ref Des	Description	Manufacturer	Part Number
22	5	L1–L5	FERRITE BEAD 470 OHM 0805	Taiyo Yuden	BK2125HM471-T
23	5	R1, R67, R68, R69, R70	RES 0.0 OHM 1/10W 5% 0603 SMD	Yageo	RC0603JR-070RL
24	20	R2, R3, R4, R7, R10, R13, R16, R19, R22, R25, R28, R31, R34, R37, R40, R43, R46, R49, R63, R71	RES 10.0K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710KL
25	0	R5, R6, R8, R9, R11, R12, R14, R15, R17, R18, R20, R21, R23, R24, R26, R27, R29, R30, R32, R33, R35, R36, R38, R39, R41, R42, R44, R45, R47, R48, R50, R51, R52, R53, R54, R55, R56, R57, R58, R64, R65, R66	Not Installed		
26	1	R59	RES 49.9K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0749K9L
27	1	R60	RES 46.4K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0746K4L
28	1	R61	RES 47.5K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0747K5L
29	1	R62	RES 43.2K OHM 1/10W 1% 0603 SMD	Yageo	RC0603FR-0743K2L
30	5	TP1, TP2, TP8, TP11, TP12	TEST POINT PC MINI .040"D BLACK	Keystone	5001
31	11	TP3, TP4, TP5, TP6, TP7, TP9, TP10, TP13, TP14, TP15, TP16	TEST POINT PC MINI .040"D RED	Keystone	5000
32	1	U1	Low-Cost, 8-Channel, 16-Bit Analog Front-End for Power Control	TI	ADS131E08IPAG
33	0	U2,U3, U4	Not Installed		
34	1	U5	IC UNREG CHRG PUMP V INV SOT23-5	TI	TPS60403DBVT
35	1	U6	IC LDO REG 250MA 3.0V SOT23-5	TI	TPS73230DBVT
36	1	U7	IC LDO REG NEG 200MA ADJ SOT23-5	TI	TPS72301DBVT
37	1	U8	IC LDO REG 250MA ADJ-V SOT23-5	TI	TPS73201DBVT
38	1	U9	IC EEPROM 256KBIT 400KHZ 8TSSOP	Microchip	24AA256-I/ST
39	1	OSC1	OSC 2.0480 MHZ 3.3V HCMOS SMT	Fox	FXO-HC735-2.048
40	9	N/A	0.100 Shunt - Black Shunts	3M	969102-0000-DA
41	1	N/A	Printed Circuit Board	TI	6462011 (MMB0)

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6.2 PCB Layout

The ADS131E08 PCB layout is appended to this document.

6.3 Front-End Board Schematic

The ADS131E08 schematic is appended to this document.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (February 2016) to C Revision	Page
• Corrected Table 4.	11

Changes from A Revision (February 2016) to B Revision	Page
• Removed *supplied wall-mount power supply* from the *Installing the First USB Driver* section.	7

Changes from Original (June 2012) to A Revision	Page
• Removed support for *included* power adapter for this EVM.	4

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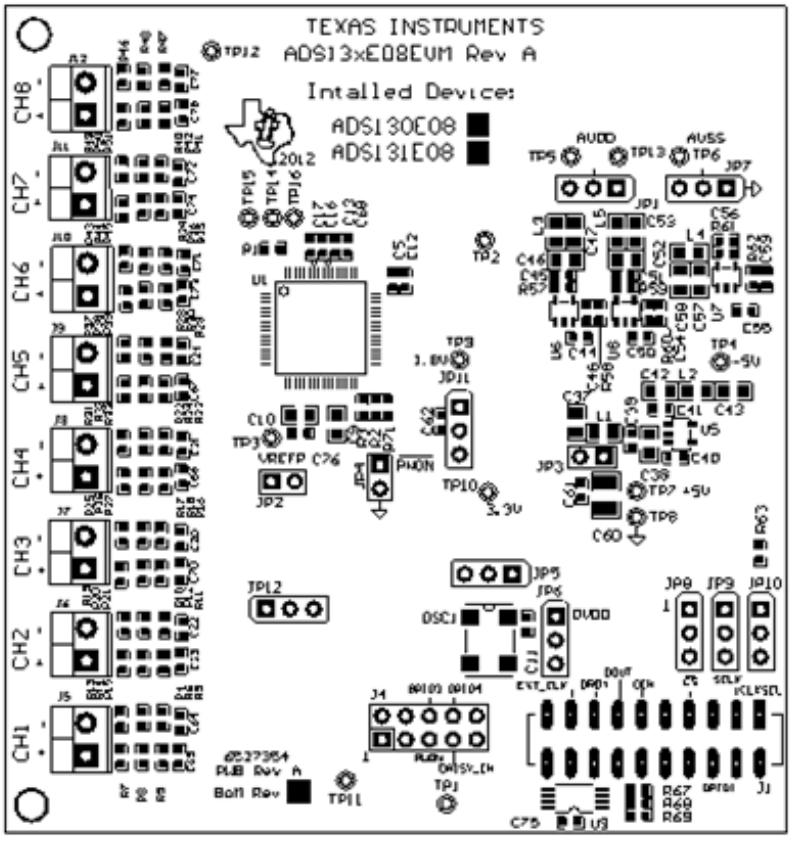
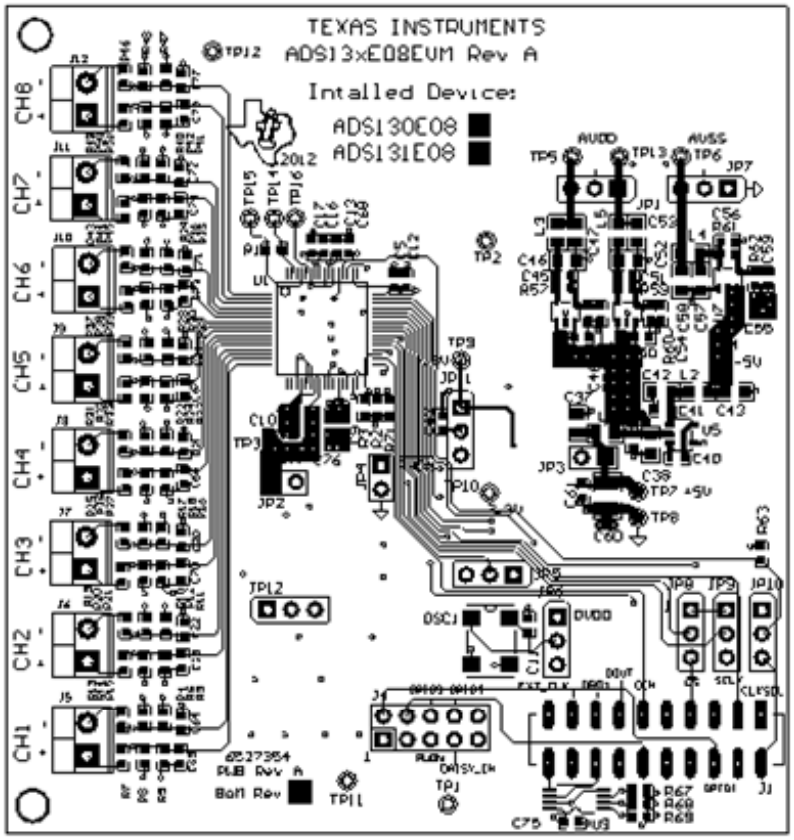
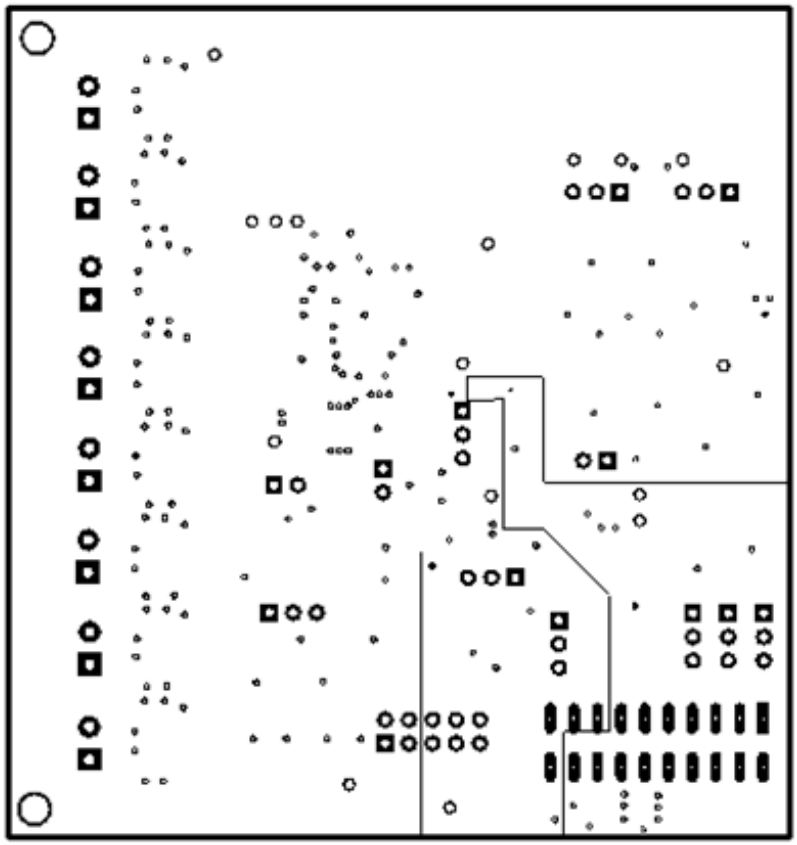


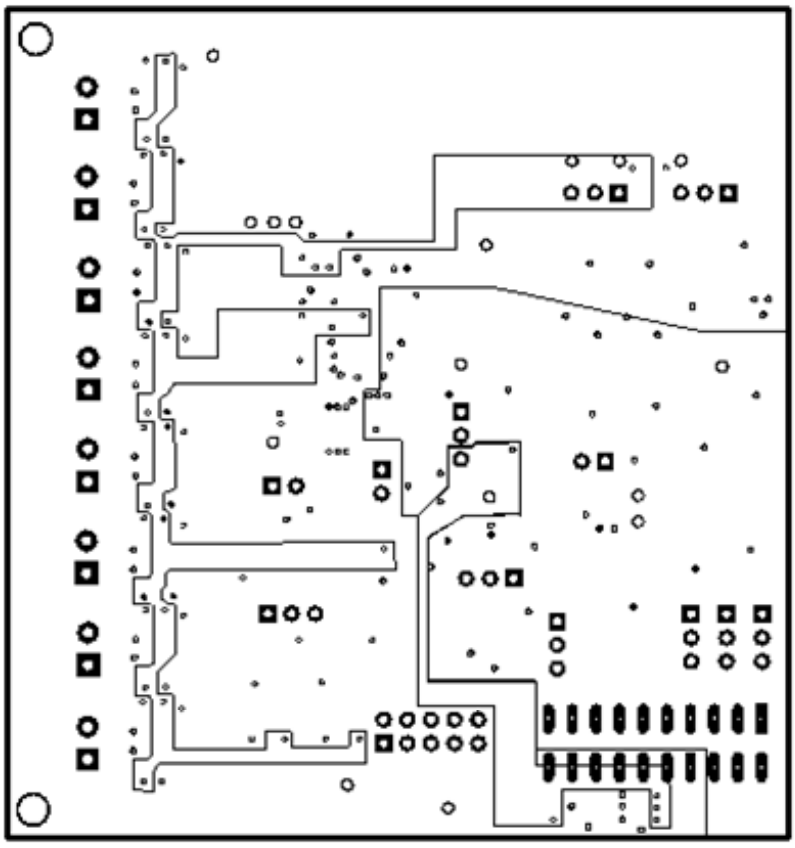
Top Assembly



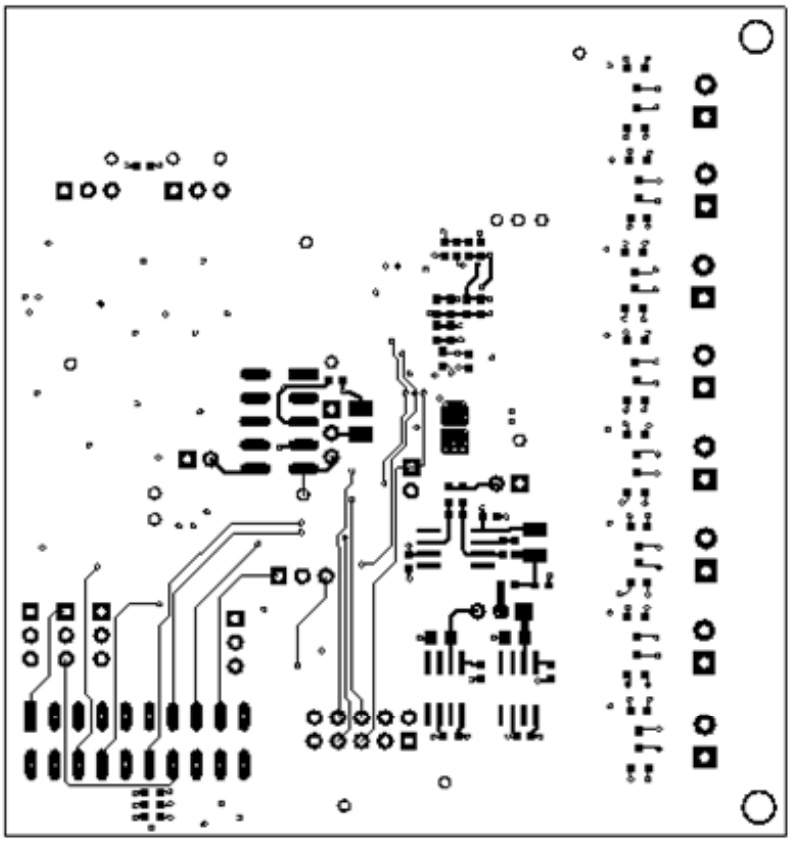
Top Layer



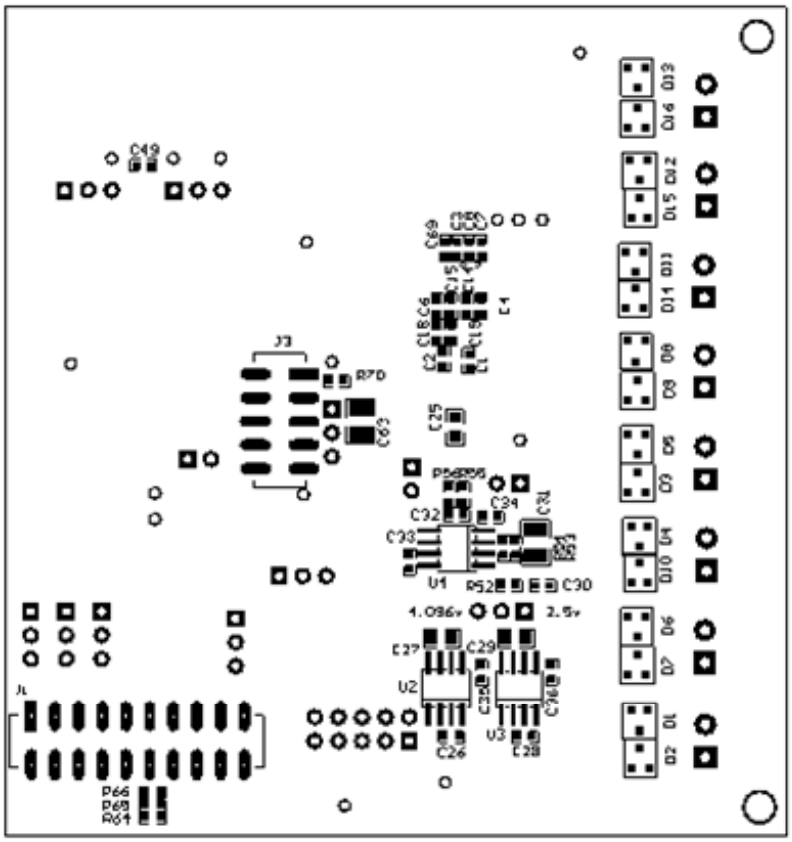
Internal Layer 1



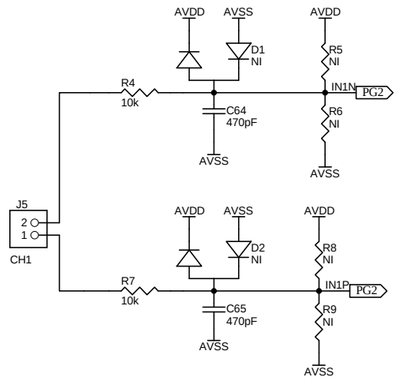
Internal Layer 2

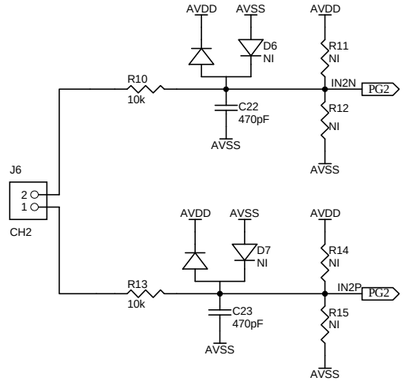


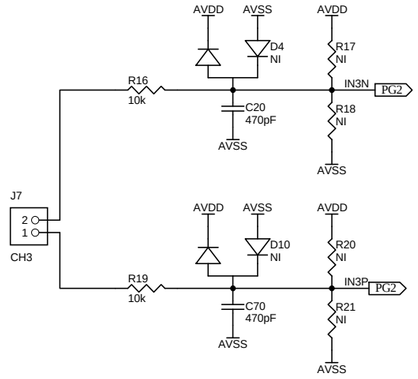
Bottom Layer

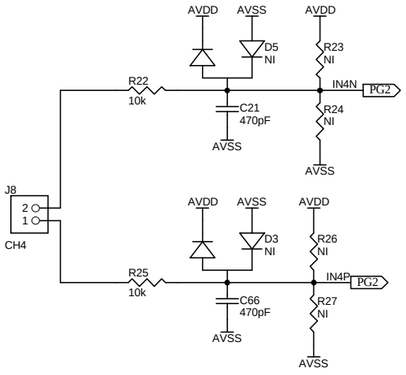


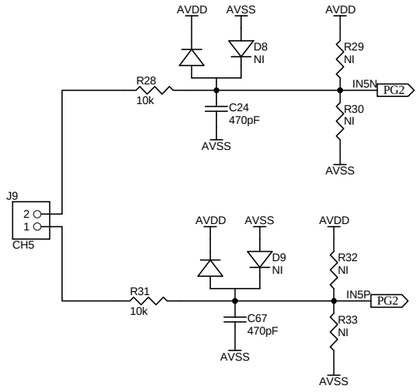
Bottom Assembly

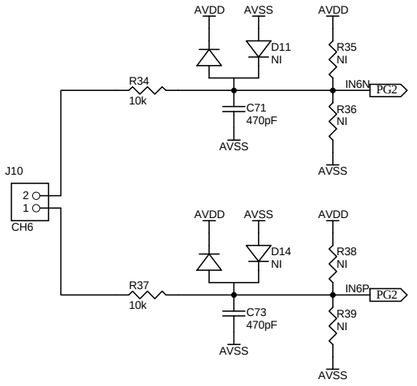


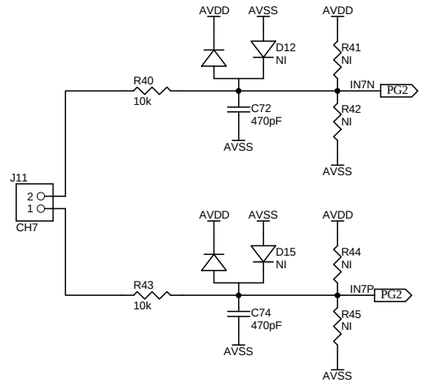


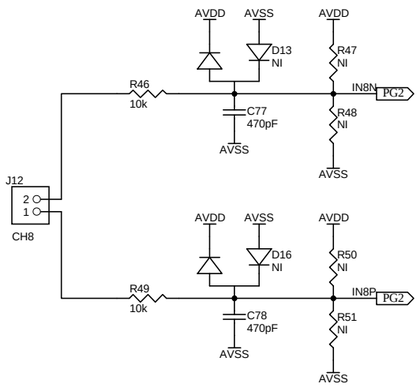












Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
FILE:	

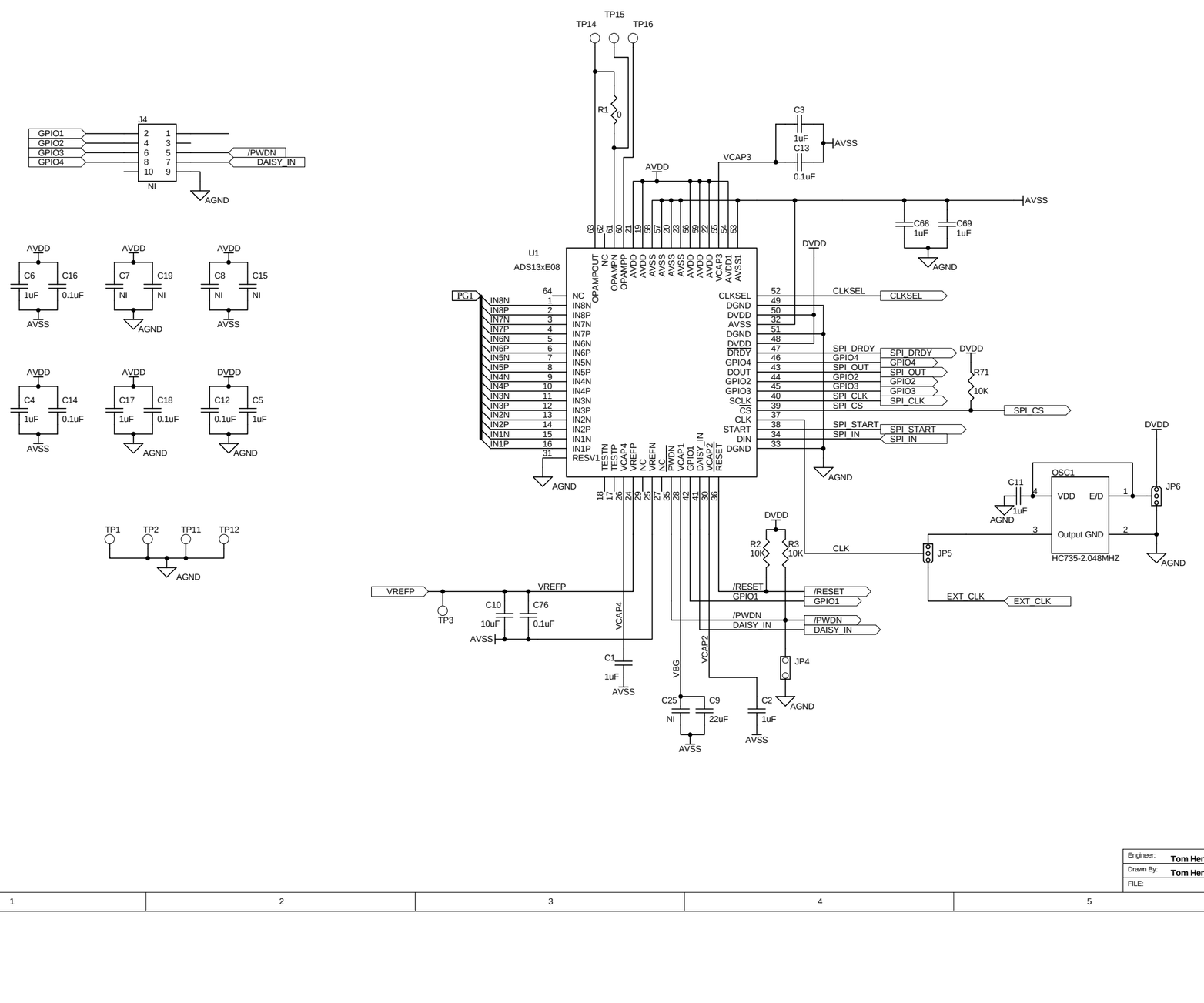
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: **ADS13xE08**

DOCUMENTCONTROL #

REV: **A**

DATE: 2-May-2012 SIZE: SHEET: **1** OF: **5**



ADC Frontend

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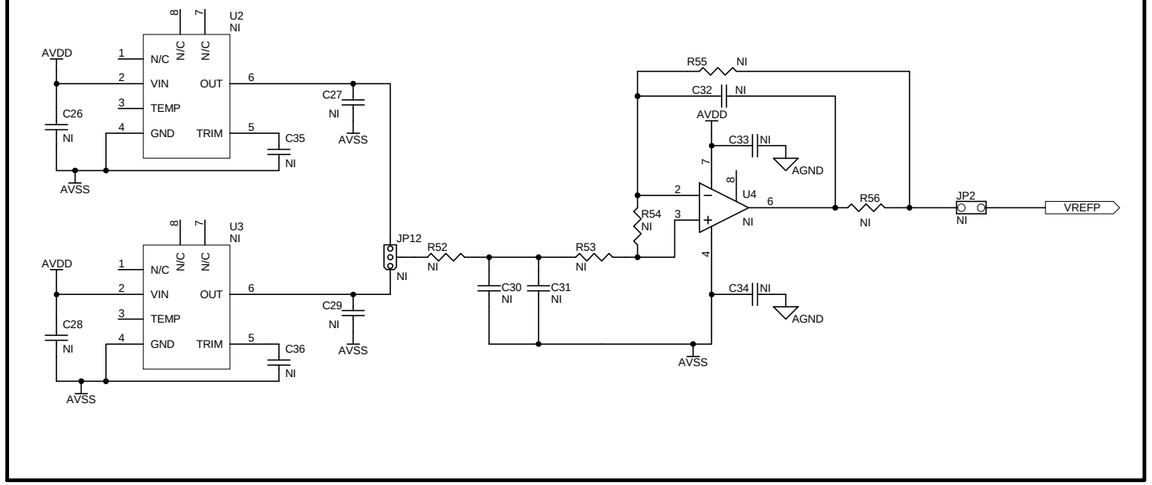
Engineer: Tom Hendrick	DOCUMENTCONTROL #	REV: A	
Drawn By: Tom Hendrick			
FILE:	DATE: 2-May-2012	SIZE:	SHEET: 2 OF: 5

External Reference

External Reference Drivers



NOT INSTALLED

Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
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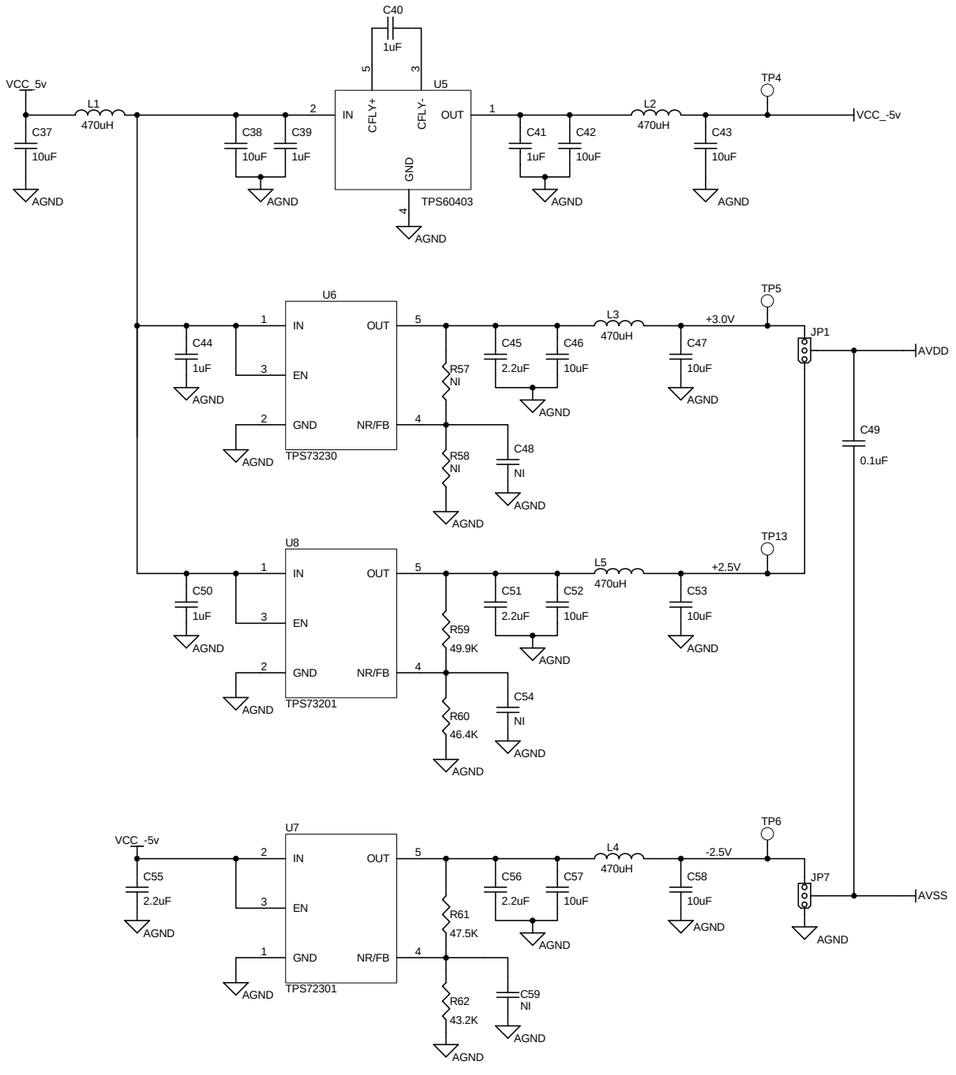
DATE: 2-May-2012 SIZE: SHEET: **3** OF: **5**



Power Supplies

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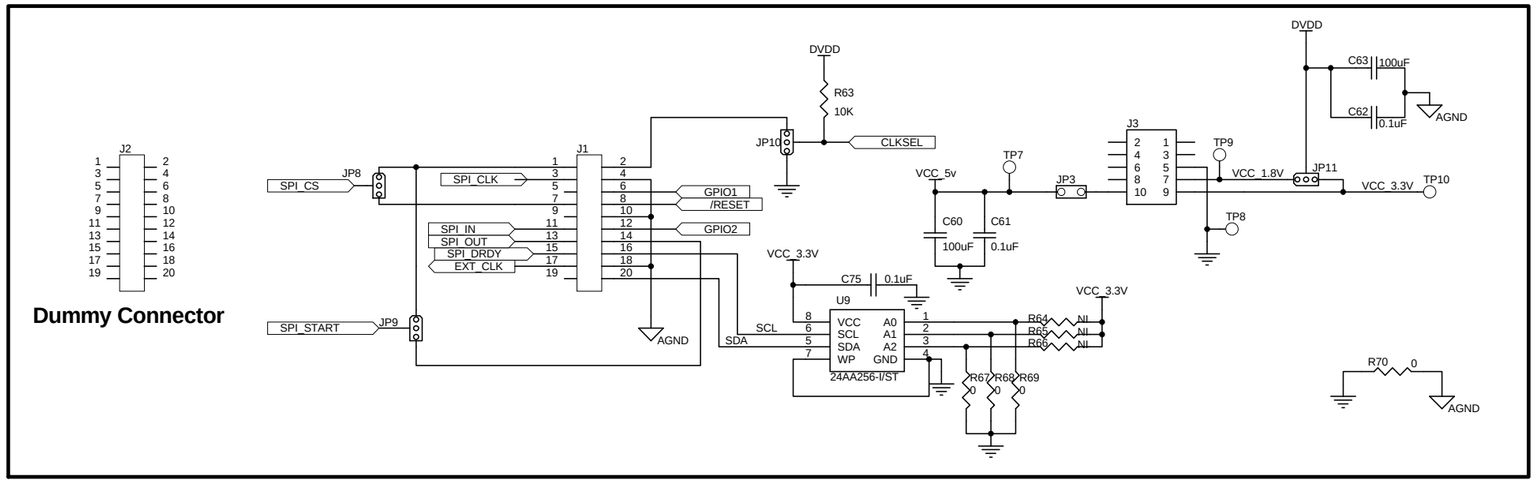
Engineer: Tom Hendrick	Title: ADS13xE08		
Drawn By: Tom Hendrick	DOCUMENTCONTROL #		REV: A
FILE:	DATE: 2-May-2012	SIZE:	SHEET: 4 OF: 5

Dummy Connector



Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
FILE:	

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Title: **ADS13xE08**

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