HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

Features

- Gain, D.C. ..... 2 x 10^6 V/V
- Aquisition Time 1.0μs (0.01%)
- Droop Rate ..... 0.08μV/μs (+25°C)
  17μV/μs (Full Temperature)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Description

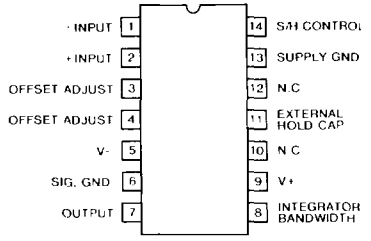
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

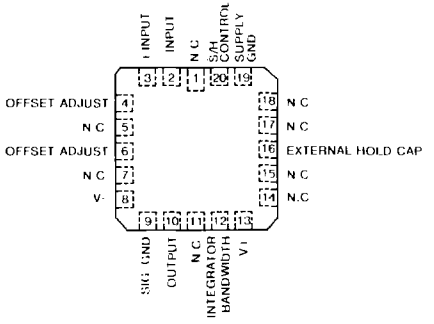
This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 is available in a Ceramic 14-pin DIP, and a Ceramic 20-pin LCC package. For further information, please see Application Note 538.

Pinouts

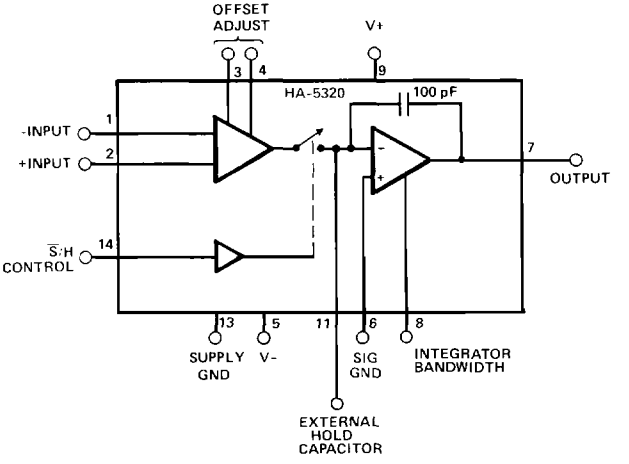
14 PIN CERAMIC DIP
TOP VIEW



20 PIN CERAMIC LCC



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage ..... ±24V
Digital Input Voltage ..... +8V, -15V
Output Current, Continuous ..... ±20mA (Note 2)
Junction Temperature ..... +175°C

Operating Temperature Range

HA-5320-2/-8 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-5320-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications

Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; C_H = Internal; Digital Input: $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold), Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-5320-2/-8 MIN	HA-5320-2/-8 TYP	HA-5320-2/-8 MAX	HA-5320-5/-7 MIN	HA-5320-5/-7 TYP	HA-5320-5/-7 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Input Resistance	+25°C	1	5	-	1	5	-	MΩ
Input Capacitance	+25°C	-	-	3	-	-	3	pF
Offset Voltage	+25°C	-	0.2	-	-	0.5	-	mV
	Full	-	-	2.0	-	-	1.5	mV
Bias Current	+25°C	-	70	200	-	100	300	nA
	Full	-	-	200	-	-	300	nA
Offset Current	+25°C	-	30	100	-	30	300	nA
	Full	-	-	100	-	-	300	nA
Common Mode Range	Full	±10	-	-	±10	-	-	V
CMRR (Note 3)	+25°C	80	90	-	72	90	-	dB
Offset Voltage T.C.	Full	-	5	15	-	5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, D.C.	+25°C	10^6	$2x10^6$	-	$3x10^5$	$2x10^6$	-	V/V
Gain Bandwidth Product ($A_V = +1$)	+25°C							
(Note 5) $C_H = 100pF$	-	-	2.0	-	-	2.0	-	MHz
$C_H = 1000pF$	-	-	0.18	-	-	0.18	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 4)	+25°C	-	600	-	-	600	-	kHz
Output Resistance (Hold Mode)	+25°C	-	1.0	-	-	1.0	-	Ω
Total Output Noise, D.C. to 10MHz								
Sample	+25°C	-	125	200	-	125	200	μV_{RMS}
Hold	+25°C	-	125	200	-	125	200	μV_{RMS}
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	-	100	-	-	100	-	ns
Overshoot (Note 5)	+25°C	-	15	-	-	15	-	%
Slew Rate (Note 6)	+25°C	-	45	-	-	45	-	V/µs

Electrical Specifications (Continued)

PARAMETER	TEMP	HA-5320-2/-8			HA-5320-5/-7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	-	-	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current (V_{IL} = 0V)	Full	-	-	10	-	-	4	µA
Input Current (V_{IH} = +5V)	Full	-	-	0.1	-	-	0.1	µA
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% (Note 7)	+25°C	-	0.8	1.2	-	0.8	1.2	µs
Acquisition Time to 0.01% (Note 7)	+25°C	-	1.0	1.5	-	1.0	1.5	µs
Aperture Time (Note 8)	+25°C	-	25	-	-	25	-	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	-	0.3	-	-	0.3	-	ns
Droop Rate	+25°C	-	0.08	0.5	-	0.08	0.5	µV/µs
	Full	-	17	100	-	1.2	100	µV/µs
Drift Current (Note 9)	+25°C	-	8	50	-	8	50	pA
	Full	-	1.7	10	-	0.12	10	nA
Charge Transfer (Note 9)	+25°C	-	0.1	0.5	-	0.1	0.5	pC
Hold Mode Settling Time 0.01%	Full	-	165	350	-	165	350	ns
Hold Mode Feedthrough ($10V_{p-p}$, 100kHz)	Full	-	2	-	-	2	-	mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current (Note 10)	+25°C	-	11	13	-	11	13	mA
Negative Supply Current (Note 10)	+25°C	-	-11	-13	-	-11	-13	mA
Power Supply Rejection V+	Full	80	-	-	80	-	-	dB
(Note 11) V-	Full	65	-	-	65	-	-	dB

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below 20mA.
3. V_{CM} = ±5V D.C.
4. V_O = $20V_{p-p}$; R_L = 2kΩ; C_L = 50pF; unattenuated output.
5. V_O = $200mV_{p-p}$; R_L = 2kΩ; C_L = 50pF.
6. V_O = 20V Step; R_L = 2kΩ; C_L = 50pF.
7. V_O = 10V Step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{IH} = +3.5V, t_r < 20ns (V_{IL} to V_{IH}).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA at 20V.
11. Based on a one volt delta in each supply, i.e. 15V ±0.5V D.C.

Applying the HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_H is used, then a noise bandwidth capacitor of value 0.1 C_H should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon® and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

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Applications

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier — its most widely used configuration. As an input device for a fast successive — approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor C_H as shown. As mentioned earlier, $0.1C_H$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

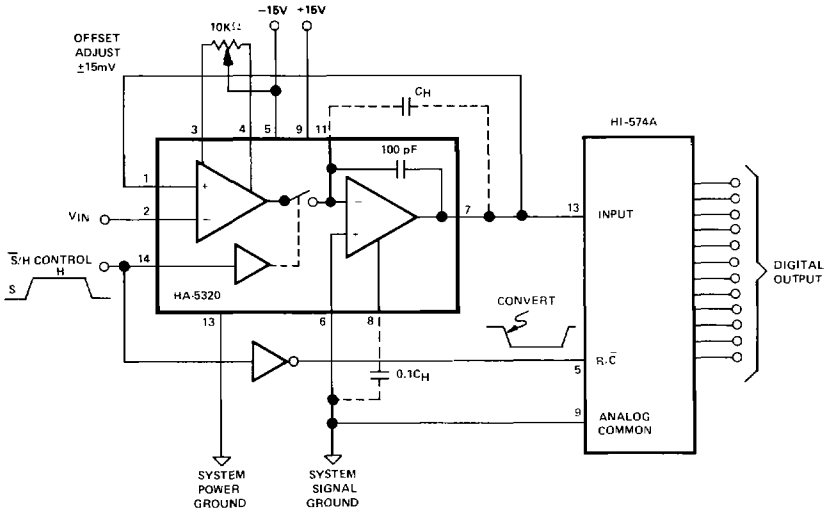


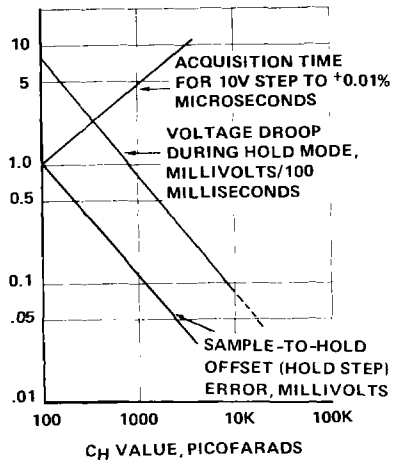
FIGURE 1.

TYPICAL HA-5320 CONNECTIONS: NONINVERTING UNITY GAIN MODE

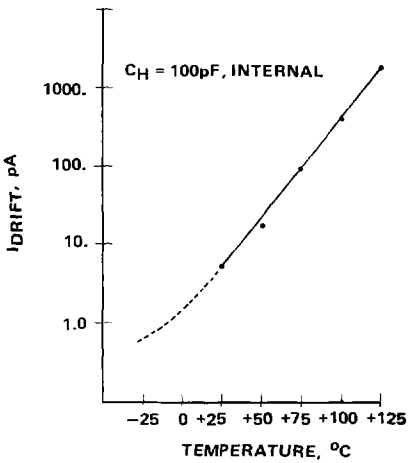
NOTE: Pin Numbers Refer to DIP Package Only.

Performance Curves V_{SUPPLY} = ±15VDC

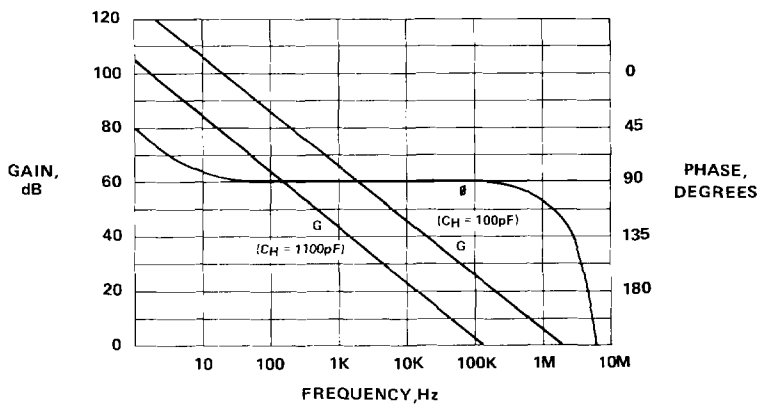
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT vs. TEMPERATURE

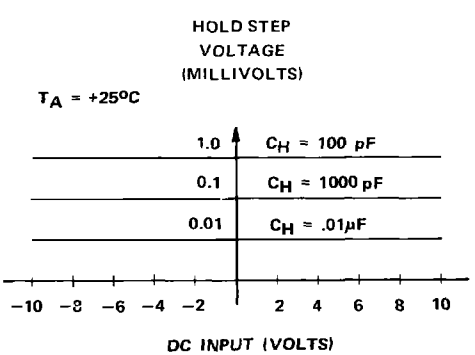


OPEN LOOP GAIN AND PHASE RESPONSE

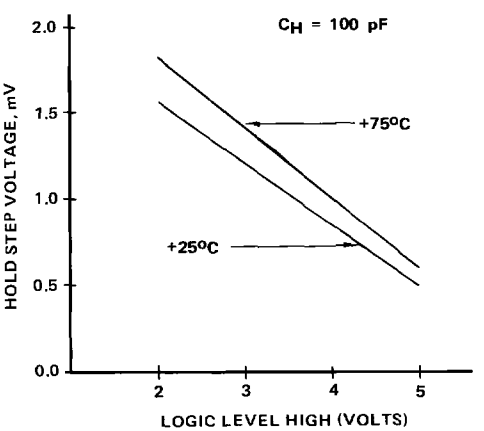


TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

HOLD STEP vs. INPUT VOLTAGE

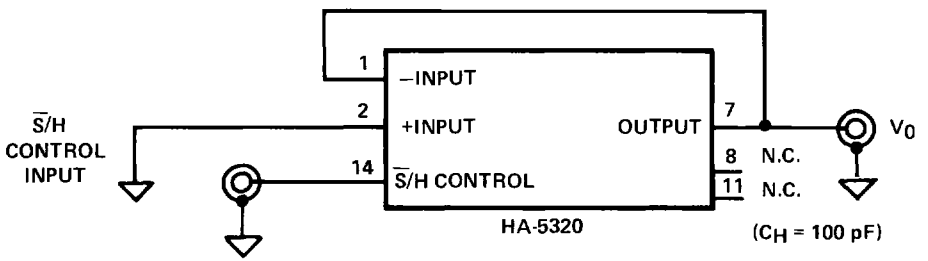


HOLD STEP vs. LOGIC (V_{IH}) VOLTAGE



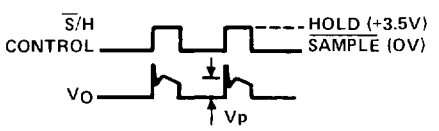
Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

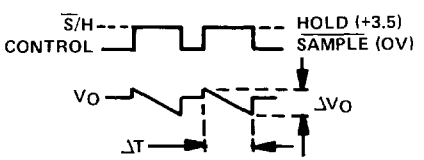
1. Observe the "hold step" voltage V_p:



2. Compute charge transfer: $Q = V_p C_H$

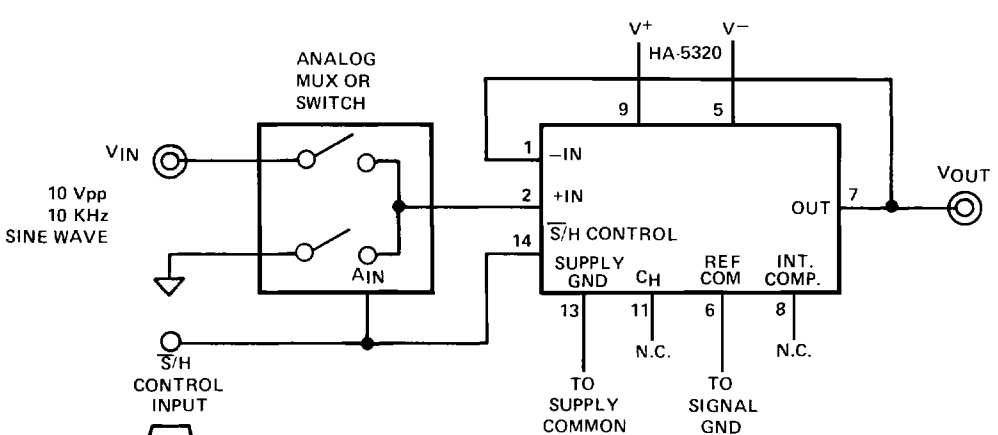
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta V_O/\Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$, and compute drift current: $I_D = C_H \Delta V_O/\Delta T$.

HOLD MODE FEED THROUGH ATTENUATION



Feedthrough in dB = 20 Log $\frac{V_{OUT}}{V_{IN}}$ where:

V_{OUT} = $Volts_{p-p}$, Hold Mode,
V_{IN} = $Volts_{p-p}$.

Glossary of Terms

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Offset Error (V)}$$

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

HOLD STEP ERROR:

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to $\overline{S}$/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (Volts/sec)}$$

Die Characteristics

Transistor Count 175
Die Dimensions ..... 90.2 x 143.7 x 19 mils
Substrate Potential ..... $-V_{SUPPLY}$
Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19