MAX3580

Direct-Conversion TV Tuner

General Description

The MAX3580 fully integrated, direct-conversion TV tuner is designed for Digital Video Broadcasting-Terrestrial (DVB-T) applications. The integrated tuner covers a 170MHz to 230MHz input frequency range for the VHF-III band and 470MHz to 878MHz for the UHF band.

The MAX3580 direct-conversion tuner integrates an RF input switch and a multiband tracking filter, allowing low-power tuner-on-board applications without the cost and power-dissipation issues of dual-conversion tuner solutions. The zero-IF architecture eliminates the need for SAW filters by providing baseband I and Q outputs directly to the demodulator. In addition, DC-offset cancellation is implemented on-chip using a mixed-signal architecture to improve the second-order distortion performance and the dynamic range of the downstream digitizer and demodulator.

The MAX3580 features dynamic gain control of more than 76dB and a typical midband noise figure of 4.7dB referred to the LNA input. The VCO architecture optimizes both in-band and wideband phase noise for OFDM applications where sensitivity to both 1kHz phase noise and wideband phase noise related to strong adjacents can be a problem.

The MAX3580 communicates using a 2-wire serial bus. The device operates from a typical +3.3V power supply and dissipates 650mW. The MAX3580 is available in a small 32-pin TQFN package (5mm x 5mm) with an exposed paddle.

Applications

- Digital Televisions
- Digital Terrestrial Set-Tops
- Laptop Televisions
- USB Peripherals

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3580ETJ+	-40°C to +85°C	32 TQFN-EP*
MAX3580ETJ+T	-40°C to +85°C	32 TQFN-EP*

**EP = Exposed pad.*

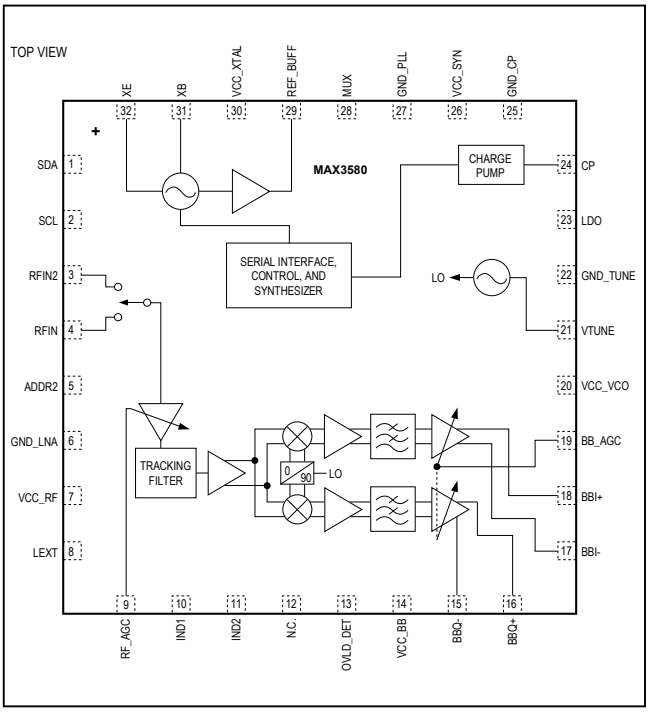
+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel package.

Features

- 650mW Power Dissipation (at V_{CC} = +3.3V)
- I and Q Baseband Outputs Eliminate All IF-SAW Filters
- Integrated RF Tracking Filters
- Tunable Baseband Lowpass Filters
- Full-Band VHF-III and UHF Tuning
- +38dB Digital ACPR, +47dB Analog ACPR
- Low Noise Figure: 4.7dB (typ)
- Frac-N Synthesizer for -90dBc/Hz Close-In Phase Noise
- +3.1V to +3.5V Supply Voltage Range
- Ultra-Small, 5mm x 5mm Thin QFN Package

Pin Configuration/Functional Diagram



maxim integrated™

Absolute Maximum Ratings

VCC_ _ to GND.....-0.3V to +3.6V
SDA, SCL, ADDR2, MUX, REF_BUFF,
BB_AGC, RF_AGC to GND .....-0.3V to +3.6V
All Other Pins to GND .....-0.3V to (+V_{CC} + 0.3V)
RF Input Power .....+10dBm
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +165°C
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 21.3mW/°C above +70°C).....1702mW
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

Electrical Characteristics

(MAX3580 EV kit, V_{CC} = +3.1V to +3.5V, V_{GND} = 0V, V_{BB_AGC} = V_{RF_AGC} = +2.85V, RF input terminated into a 75Ω load, BBI_ and BBQ_ are open, no input signal, VCO active, registers set according to the specified default register conditions, unless otherwise specified. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Supply Voltage	V_{CC}		3.1		3.5	V
Supply Current	I_{CC}	Active		197	225	mA
		Shutdown mode		< 100		µA
RF_AGC AND BB_AGC						
Input Bias Current	I_{AGC}	V_{AGC} at +0.5V and +2.85V	-50		+50	µA
RF and Baseband AGC Control Voltage	V_{AGC}	Maximum gain	2.85			V
		Minimum gain			0.5	
SERIAL INTERFACE AND MUX OUTPUT (SCL, SDA, MUX)						
Input Logic-Level Low	V_{IL}				0.3 x V_{CC}	V
Input Logic-Level High	V_{IH}		0.7 x V_{CC}			V
Input Hysteresis				0.05 x V_{CC}		V
SDA, SCL Input Current			-10		+10	µA
Output Logic-Level Low	V_{OL}	Sink current = 0.3mA			0.4	V
Output Logic-Level High	V_{OH}	Source current = 0.3mA	V_{CC} x 0.5			V
Operating Frequency Range	f_{RF}	Gain specification met across this frequency band	170		230	MHz
			470		878	
Overall Voltage Gain (Note 2)		V_{RF_AGC} = V_{BB_AGC} = +2.85V	71			dB
		V_{RF_AGC} = V_{BB_AGC} = +0.5V			26	
RF Gain Flatness		Within each VHF-III and UHF band (Note 10)	-4		+4	dB
Input Return Loss		Worst case across band selected, 75Ω system		7		dB

Electrical Characteristics (continued)

(MAX3580 EV kit, V_{CC} = +3.1V to +3.5V, V_{GND} = 0V, V_{BB_AGC} = V_{RF_AGC} = +2.85V, RF input terminated into a 75Ω load, BBI_ and BBQ_ are open, no input signal, VCO active, registers set according to the specified default register conditions, unless otherwise specified. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Noise Figure (DSB) (Notes 3, 4)	NF	230MHz		5.4		dB
		470MHz		4.7		
		858MHz		6.5		
Input 2nd-Order Intercept Point	IIP2	Broadband (Notes 4, 5)		15		dBm
		Broadband, RF_AGC adjusted for 49dB of gain		> 26		
Input 3rd-Order Intercept Point	IIP3	Broadband (Notes 4, 6)		> -4		dBm
		Broadband, RF_AGC adjusted for 49dB of gain		> 12		
		Narrowband (Notes 4, 7)		-6		
		Narrowband, RF_AGC adjusted for 49dB of gain (Note 7)		+16		
RF 1dB Desense		$P_{DESIRED}$ = -78dBm and converted to 3.75MHz, PTONE 10MHz higher (Note 4)		-22		dBm
		RF_AGC adjusted for 49dB of gain, $P_{DESIRED}$ = -55dBm		+1		
LO Harmonic Reception		RF input range of 170MHz to 960MHz (Note 8)		> -60		dBc
		RF input range of 960MHz to 1400MHz		> -40		
RF Channel Flatness		8MHz RF channel at baseband, tested at 169MHz and 469MHz	-1		+1	dB
Isolation		DC to 30MHz, RF input to baseband output, relative to desired channel		> 60		dBc
Quadrature Accuracy		I/Q phase error at 1MHz	-3		+3	Degrees
		I/Q amplitude error at 1MHz	-1.5		+1.5	dB
Spurious at the RF Input (Note 3)		50MHz to 470MHz		-50	-20	dBmV
		470MHz to 878MHz		-50	-35	
		878MHz to 1732MHz		< -50	-20	
Phase Noise (Single-Sideband, Closed Loop)	ΦN	At 1kHz to 10kHz (Note 3)	-77	-90		dBc/Hz
		At 100kHz (Note 3)	-94	-107		
		At 1MHz		-130		

Electrical Characteristics (continued)

(MAX3580 EV kit, V_{CC} = +3.1V to +3.5V, V_{GND} = 0V, V_{BB_AGC} = V_{RF_AGC} = +2.85V, RF input terminated into a 75Ω load, BBI_ and BBQ_ are open, no input signal, VCO active, registers set according to the specified default register conditions, unless otherwise specified. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SIGMA-DELTA FRACTIONAL-N SYNTHESIZER						
REFERENCE OSCILLATOR						
Frequency	f_{REF}		4		27	MHz
Input Impedance	Z_{IN}			10		kΩ
Voltage Gain				30		V/V
Output Impedance	Z_{OUT}			15		Ω
Buffered Output		10kΩ || 10pF load	0.7			V_{P-P}
DIVIDERS						
RF N Divider Ratio		(Notes 12, 13)	12		251	—
RF R Divider Ratio		VHF band operation requires R divider = 2	1		2	—
Fractional-N Resolution				20		Bits
LO PHASE DETECTOR AND CHARGE PUMP						
Phase-Detector Frequency			4		27	MHz
Charge-Pump Current	I_{CP}	Gain = 0		600		µA
		Gain = 1		1200		
Charge-Pump Tri-State Current			-10		+10	µA
Charge-Pump Compliance Range		Charge-pump positive to negative current matching of ≤ ±5%	0.4		V_{CC} -0.4	V
LOCAL OSCILLATOR						
Tuning Frequency Range	f_{OSC}	Tank Frequency	2160		4400	MHz
VCO Dividers			4		16	—
BASEBAND STAGE						
Nominal Output Voltage		(Note 2)		1		V_{P-P}
1dB Output Compression Point	P_{1dB}	Differential voltage at 3MHz	1.6	2		V_{P-P}
Output Impedance		Differential		60		Ω
Passband AGC Range		V_{BB_AGC} = 0.5V to 2.85V	30	50		dB
Passband Cutoff Attenuation		At 3.8MHz (UHF Mode); at 3.325MHz (VHF Mode)		2	5	dB
Passband Differential Gain Error		2MHz to 3.8MHz, I channel vs. Q channel (UHF mode)	-0.45		+0.45	dB
Passband Group Delay		From DC to 3.8MHz over any 1.1kHz band (UHF mode)		5		ns
Group Delay Mismatch		From 0.1MHz to 3.8MHz, I channel vs. Q channel (UHF mode) (Note 9)		< 2		ns

Electrical Characteristics (continued)

(MAX3580 EV kit, V_{CC} = +3.1V to +3.5V, V_{GND} = 0V, V_{BB_AGC} = V_{RF_AGC} = +2.85V, RF input terminated into a 75Ω load, BBI_ and BBQ_ are open, no input signal, VCO active, registers set according to the specified default register conditions, unless otherwise specified. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rejection Ratio		At 5.25MHz (UHF mode)	23			dB
		At 4.75MHz (VHF mode)	23			
		At 13.25MHz (UHF mode) (Note 3)	63			
		At 11.75MHz (VHF mode) (Note 3)	61			
		At > 16.2MHz		84		
DC Output Voltage	V_{CM}	Common mode (Note 11)		0.485 x V_{CC}		V_{DC}
Output DC Offset		V_{BB_AGC} = 2.85V	-100		+100	mV
Baseband Highpass Cutoff		Programmable		20 to 200		Hz
AGC Gain Slope		V_{BB_AGC} = 0.5V to 2.85V	14		35	dB/V
Ratio of Passband to Stopband Noise		V_{BB_AGC} = 2.85V, 10kHz to 3.8MHz vs. 16.2MHz to 23.8MHz		15		dB
2-WIRE INTERFACE						
Clock Rate					400	kHz

Note 1: Part is tested at room temperature only. Performance at cold and hot temperature is guaranteed by design and characterization.
Note 2: The specified overall voltage gain is suitable to amplify -93dBm to -20dBm to $1V_{P-P}$ at the baseband output.
Note 3: Guaranteed by design characterization over the specified operating conditions. Not production tested.
Note 4: BB_AGC adjusted for gain = 72dB with RF_AGC at 2.85V.
Note 5: Two tones at a) 230MHz and 431MHz with IM measured at 201MHz and b) 230MHz and 701MHz with IM measured at 471MHz.
Note 6: Two tones at 499MHz and 689MHz with IM measured at 879MHz.
Note 7: IM3 measured with two tones within the adjacent channel at a) 205.75MHz and 210.5MHz with IM measured at 201MHz and b) 475.25MHz and 479.5MHz with IM measured at 471MHz.
Note 8: Measured at RF = 171MHz with harmonics at 511MHz (3rd harmonic) and 851MHz (5th harmonic).
Note 9: Delay of 2ns equal 2.74° phase error.
Note 10: UHF rolloff of 4dB in addition to gain flatness specification.
Note 11: Production tested at V_{CC} = +3.5V to limits of 1.7V -0.12/+0.1V.
Note 12: Operation in the VHF band requires the R-divider = 2.
Note 13: Operation of the N-divider at values below 12 is not tested or guaranteed.

Performance to Standards

The following is selected overall performance data for the MAX3580 + digital demodulator.

Table 1 shows the typical overall performance as measured using the MAX3580 and one current production DVB-T demodulator. This reference design is available in NIM card form factor upon request.

MBRAI refers to standard **MBRAI 04-102 IEC 62002-1** available from **www.ansi.org**.

NorDig refers to standard Unified 1.0.2 available from **www.nordig.org**.

Modulation of wanted and interfering channel(s) is 8k mode, 16 QAM, C/R = 3/4, GI = 1/4, sensitivity or immunity Reference Bit Error Rate is 2 x 10e-4, unless stated otherwise.

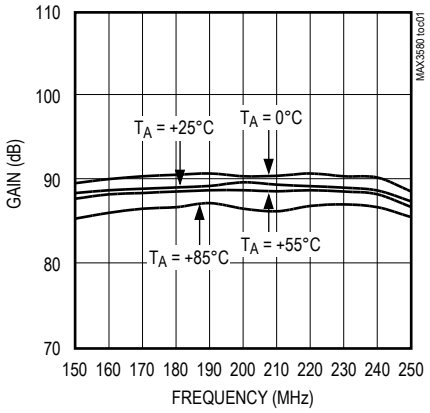
Table 1. Selected Typical MBRAI and NorDig Performance

TEST SCENARIO	COMMENTS	SPEC MINIMUM	MAX3580 TYPICAL
MBRAI S2	Immunity/ACPR for N ±1 adjacent ch.	29dB	40dB
MBRAI S2	Immunity/ACPR N ±2 alternate ch.	40dB	43dB
MBRAI L3	Linearity/crossmod. with N+2 and N+4 ch.	40dB	47dB
NorDig 16 QAM 2/3	Sensitivity at channel 21 (470MHz)	-84.1dBm	-85.1dBm
NorDig QPSK 1/2	Sensitivity at channel 42 (642MHz)	-92.1dBm	-94.8dBm
NorDig 64 QAM 7/8	Sensitivity at channel 59 (778MHz)	-74.7dBm	-76dBm

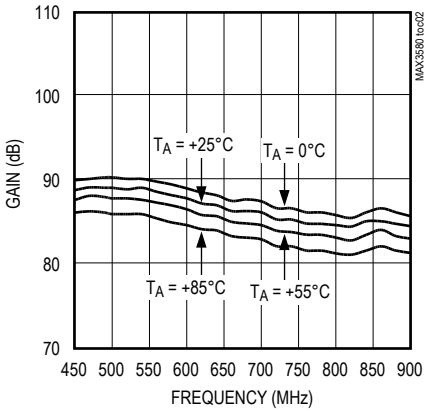
Typical Operating Characteristics

(MAX3580 Evaluation Kit, typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

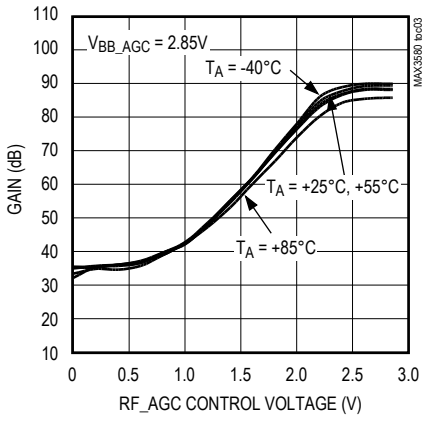
VHF-III BAND VOLTAGE GAIN vs. FREQUENCY



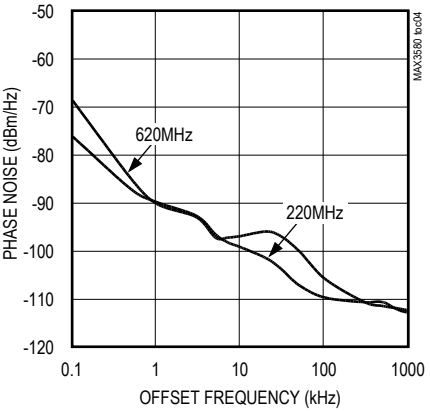
UHF BAND VOLTAGE GAIN vs. FREQUENCY



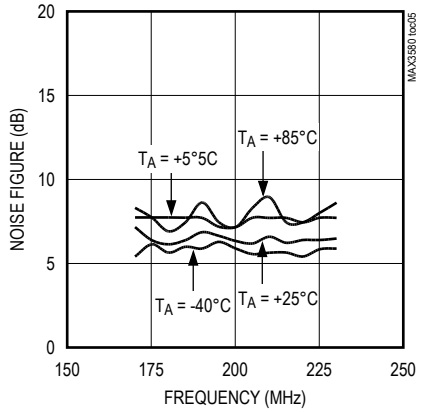
VOLTAGE GAIN vs. RF_AGC CONTROL VOLTAGE



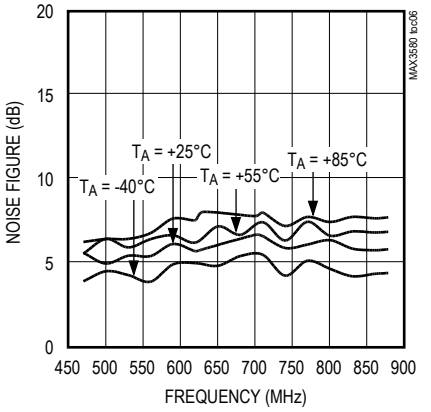
PHASE NOISE vs. OFFSET FREQUENCY



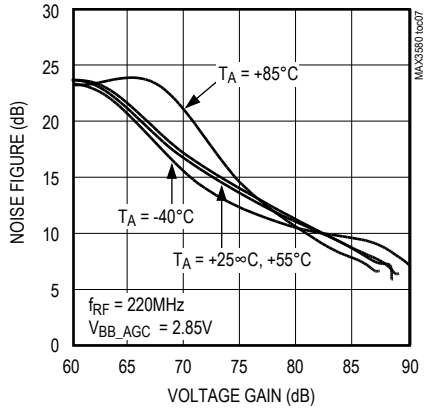
NOISE FIGURE vs. VHF FREQUENCY



NOISE FIGURE vs. UHF FREQUENCY



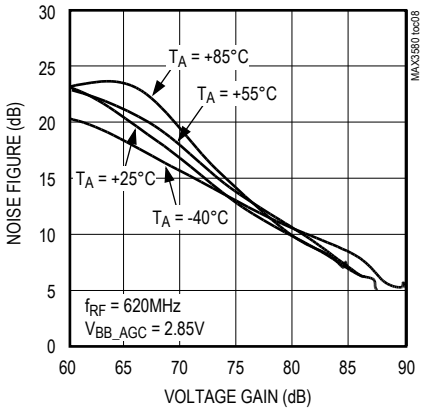
VHF MODE NOISE FIGURE vs. VOLTAGE GAIN



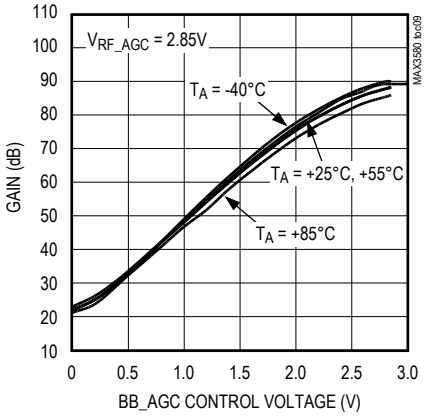
Typical Operating Characteristics (continued)

(MAX3580 Evaluation Kit, typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

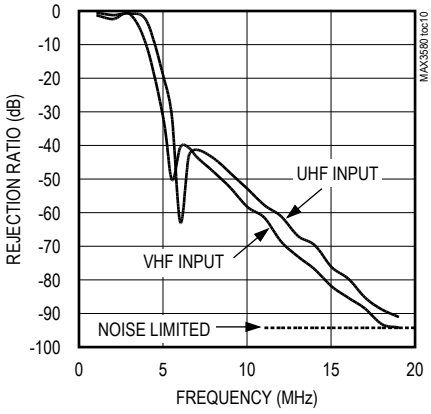
UHF MODE NOISE FIGURE vs. VOLTAGE GAIN



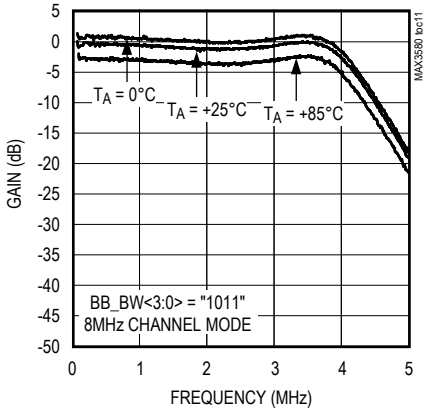
VOLTAGE GAIN vs. BB_AGC CONTROL VOLTAGE



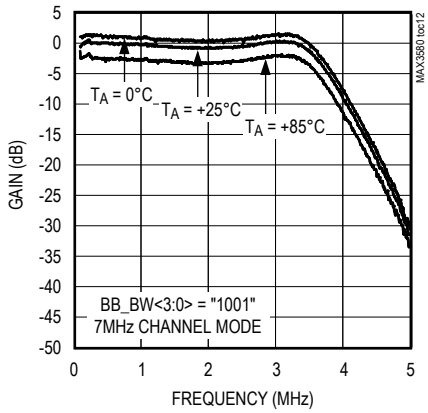
BASEBAND FILTER REJECTION RATIO



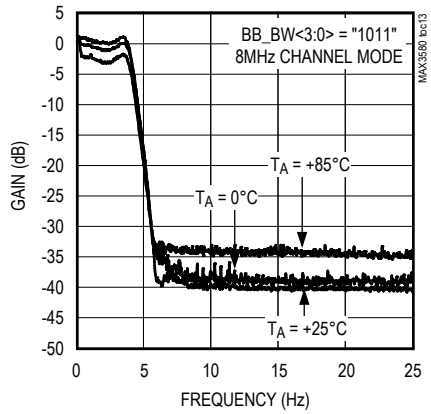
NORMALIZED BASEBAND FREQUENCY RESPONSE



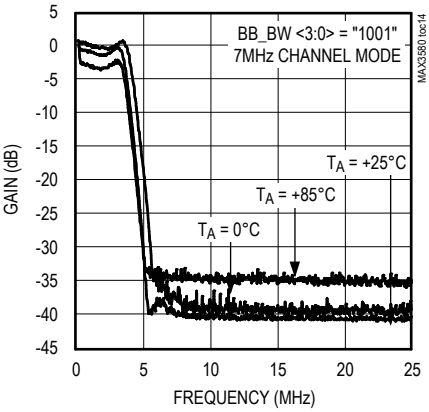
NORMALIZED BASEBAND FREQUENCY RESPONSE



NORMALIZED BASEBAND FREQUENCY RESPONSE



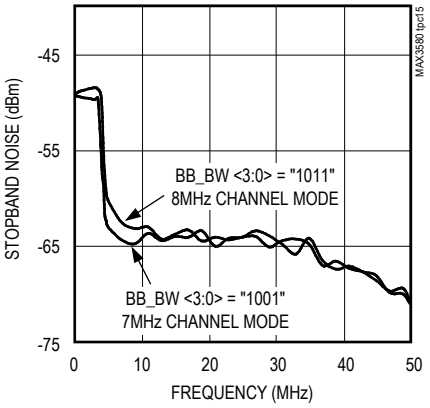
NORMALIZED BASEBAND FREQUENCY RESPONSE



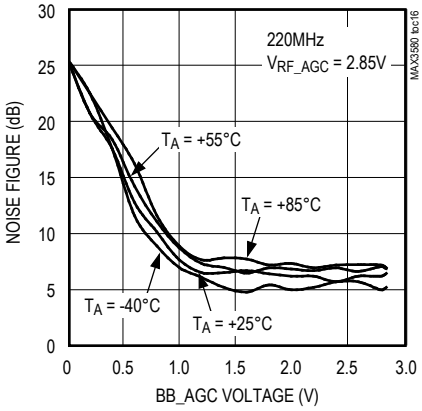
Typical Operating Characteristics (continued)

(MAX3580 Evaluation Kit, typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

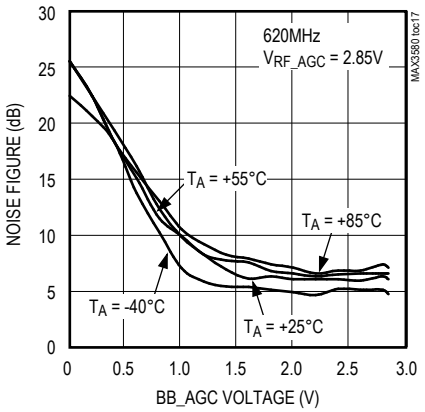
STOPBAND NOISE vs. FREQUENCY



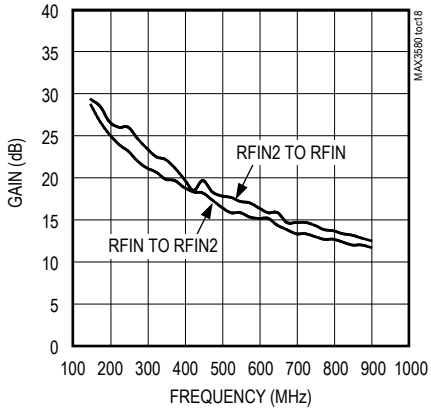
VHF MODE NOISE FIGURE vs. BB_AGC VOLTAGE



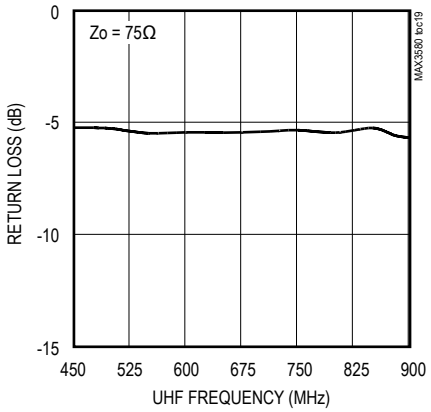
UHF MODE NOISE FIGURE vs. BB_AGC VOLTAGE



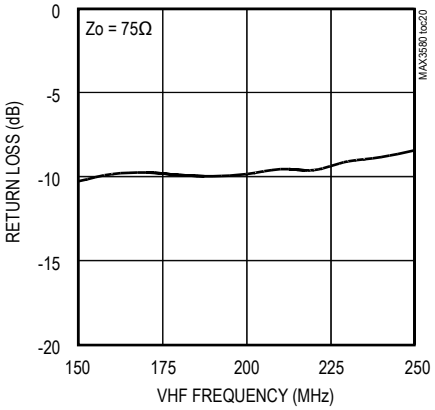
RF PORT-TO-PORT ISOLATION



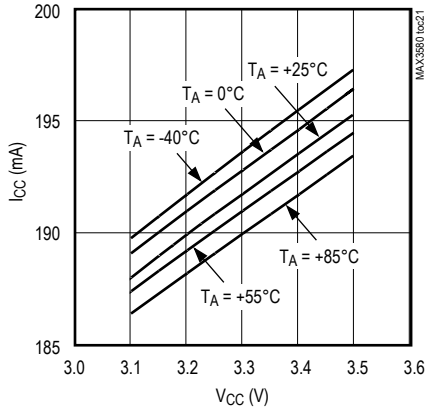
RF INPUT RETURN LOSS vs. UHF FREQUENCY



RF INPUT RETURN LOSS vs. VHF FREQUENCY



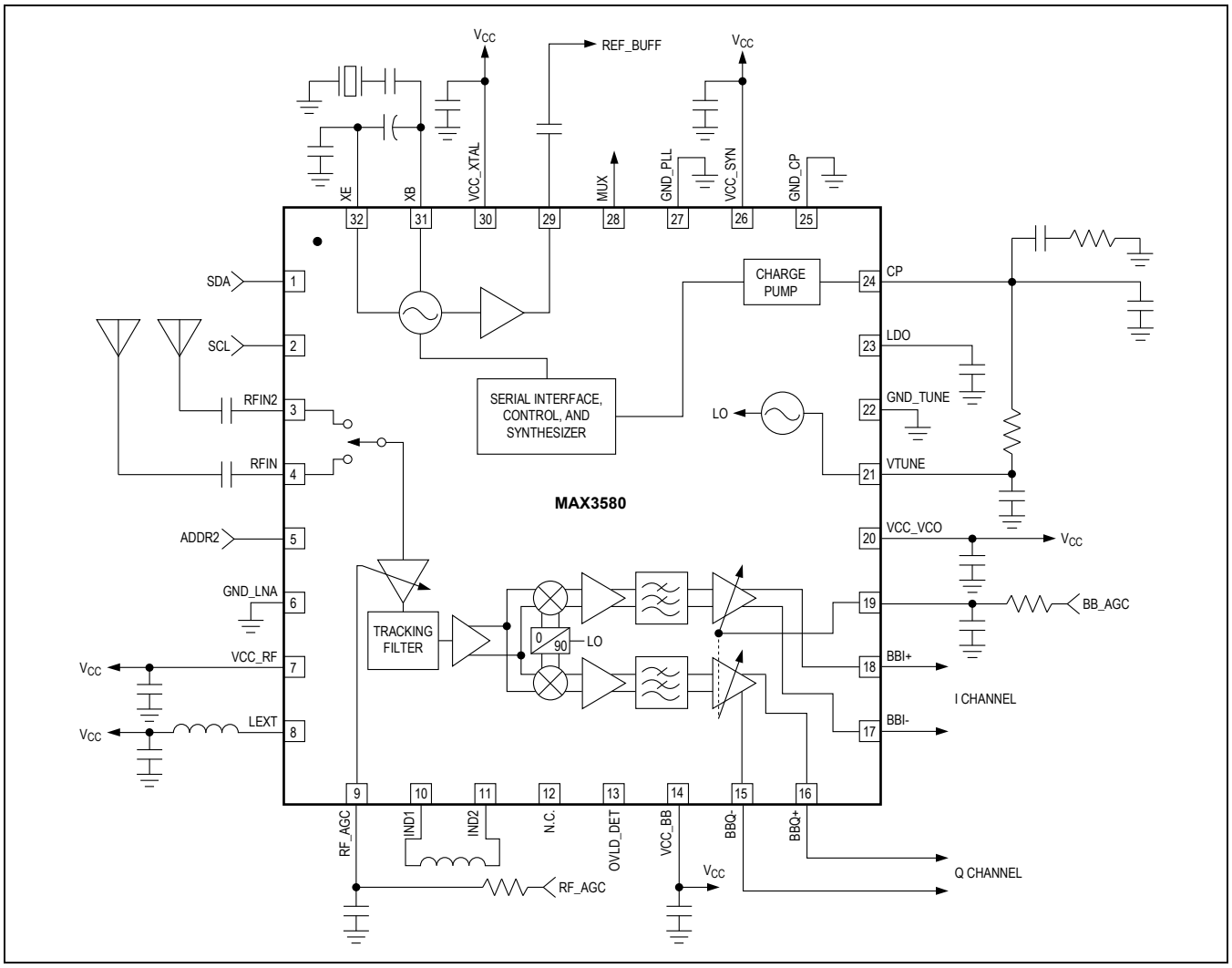
SUPPLY CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	SDA	Serial-Data Input Line. Requires a pullup resistor to V_{CC}.
2	SCL	Serial-Clock Input. Requires a pullup resistor to V_{CC}.
3	RFIN2	Second RF Input
4	RFIN	First RF Input
5	ADDR2	Address Line. Sets the 3rd LSB of the device address. Connect to ground to set for “0” or V_{CC} to set for “1.”
6	GND_LNA	Not Internally Connected. Connect to ground.
7	VCC_RF	DC Supply for RF LNA. Connect as close as possible a 100pF capacitor from this pin to GND.
8	LEXT	External Bias Inductor. Connect to V_{CC} with a 270nH inductor.
9	RF_AGC	Gain Control Input for RF VGA
10	IND1	VHF Inductor Pin 1. Keep traces to inductor as short as possible.
11	IND2	VHF Inductor Pin 2. Keep traces to inductor as short as possible.
12	N.C.	No Connection
13	OVLD_DET	Overload Detector. Do not connect any circuitry to this pin.
14	VCC_BB	DC Supply for Baseband Filter. Connect as close as possible a 10nF capacitor from this pin to ground.
15	BBQ-	Quadrature Inverted Baseband Output
16	BBQ+	Quadrature Noninverted Baseband Output
17	BBI-	In-Phase, Inverted Baseband Output
18	BBI+	In-Phase, Noninverted Baseband Output
19	BB_AGC	Gain Control Input for Baseband VGAs
20	VCC_VCO	DC Supply for the VCO. Connect as close as possible a 100pF capacitor from this pin to ground.
21	VTUNE	VCO Tuning Voltage Input. Connect the PLL loop filter output directly to this pin.
22	GND_TUNE	Ground Reference for the Tuning Voltage. Connect to ground of the loop filter.
23	LDO	VCO LDO Output. Connect a 0.1µF capacitor to ground.
24	CP	Charge-Pump Output. Connect the charge-pump output to the PLL loop filter input.
25	GND_CP	Ground for the Charge Pump
26	VCC_SYN	DC Supply for Synthesizer and Serial Interface Control. Connect as close as possible a 10nF capacitor from this pin to ground.
27	GND_PLL	Ground for the PLL
28	MUX	Multiplex Output Line. Can be used as a PLL lock-detector output.
29	REF_BUFF	Buffered Output of Reference Oscillator
30	VCC_XTAL	DC Supply for Reference Oscillator. Connect as close as possible a 10nF capacitor from this pin to ground.
31	XB	Reference Input. Connect to a parallel resonant mode XTAL through a load-matching capacitor, or can also be used as a reference clock input pin.
32	XE	Reference Oscillator Feedback. Connect to a capacitive divider when used in self-oscillating mode.
—	EP	Exposed Pad. Internally connected to ground. Solder EP to the board’s ground plane to achieve the lowest possible impedance path and optimum RF performance.

Typical Application Circuit



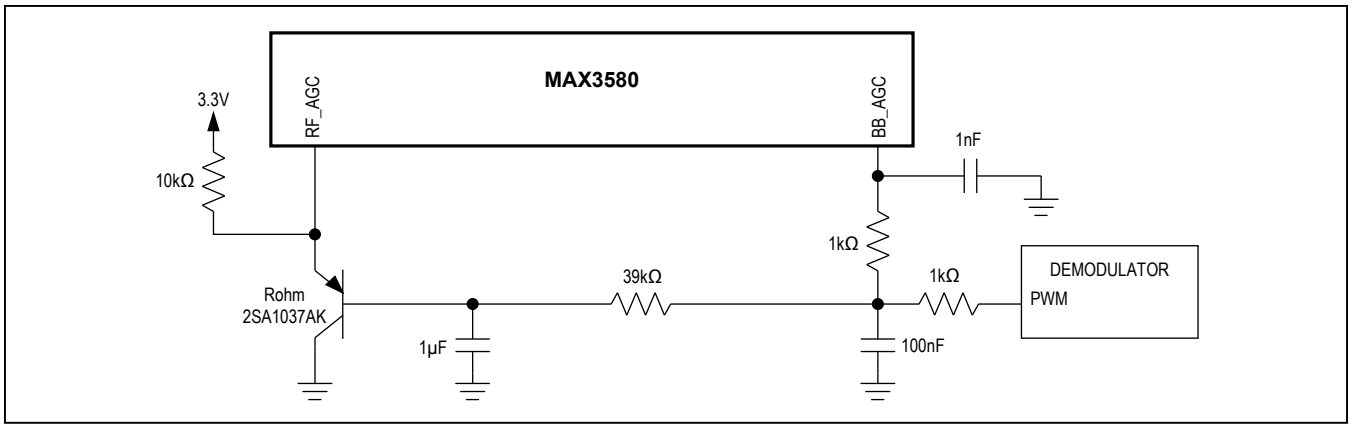


Figure 1. Single-Loop AGC Schematic

Detailed Description

Programmable Registers

The MAX3580 includes thirteen write/read registers and three read-only registers. See Table 2 for register configuration and the *Register Description* section. The register configuration of Table 2 shows each bit name and the bit usage information for all registers. “U” labeled under each bit name indicates that the bit value is user defined to meet specific application requirements. A “0” or “1” indicates that the bit must be set to the defined “0” or “1” value for proper operation. Operation is not tested or guaranteed if these bits are programmed to other values and is only for factory/bench evaluation. For field use, always program to the defined operational state. Note that all registers must be written after and no earlier than 100µs after device power-up.

Note 1: To correctly tune the VCO during a channel change, first write to Register 0x05, continuing through Register 0x06 to Register 0x12, and then write to Register 0x00 through Register 0x04.

Note 2: Upon power-up or recovery from a supply voltage brownout, all registers must be written, including the “factory use only” values. Follow up by writing the register needed for tuning to a particular frequency per note above or simply rewrite all registers a second time.

Table 2. Register Configuration

REGISTER ADDRESS	8-BIT DATA								REGISTER SETTINGS		REGISTER NAME
	D7	D6	D5	D4	D3	D2	D1	D0	OPERATION DEFINED	DEFAULT SETTINGS (POR)	
0x00	N7U	N6U	N5U	N4U	N3U	N2U	N1U	N0U	—	H17	N-Divider Integer
0x01	MP 0	LI1 0	LI0 0	INT U	F19 U	F18 U	F17 U	F16 U	—	h18	N-Divider Frac2
0x02	F15 U	F14 U	F13 U	F12 U	F1 U	F10 U	F9 U	F8 U	—	h00	N-Divider Frac1
0x03	F7 U	F6 U	F5 U	F4 U	F3 U	F2 U	F1 U	F0 U	—	h00	N-Divider Frac0
0x04	TFS<7>U	TFS<6>U	TFS<5>U	TFS<4>U	TFS<3>U	TFS<2>U	TFS<1>U	TFS<0>U	—	hDB	Tracking Filter Series Caps
0x05	VCO_DIV1 U	VCO_DIV0 U	RFSU	TF_BSU	TFP<3>U	TFP<2>U	TFP<1>U	TFP<0>U	—	h7C	Tracking Filter Parallel Cap
0x06	RDIV U	ICP U	CPS U	ADLY1 0	ADLY0 1	LF_DIV2 U	LF_DIV1 U	LF_DIV0 U	—	h0A	PLL Configuration
0x07	CP_TST2 0	CP_TST1 0	CP_TST0 0	X 0	TURBO 1	LD_MUX2 U	LD_MUX1 U	LD_MUX0 U	—	h08	Test Functions
0x08	X 0	SHDN_BG U	SHDN_PD 1	SHDN_REF U	SHDN_ SYN U	SHDN_ MX U	SHDN_ BB U	SHDN_ RF U	—	h00	Shutdown Control
0x09	VCO1 U	VCO0 U	BS2 U	BS1 U	BS0 U	VAS 1	ADL 0	ADE 0	—	hC0	VCO Control
0x0A	BB_BW3 U	BB_BW2 U	BB_BW1 U	BB_BW0 U	X 0	PD_TH2 U	PD_TH1 U	PD+TH0 U	—	h87	Baseband Control
0x0B	BB_BIA 0	DC_DAC8 0	DC_MO1 1	DC_MO0 1	DC_SP1 1	DC_SP0 0	DC_TH1 0	DC_TH0 0	h38	h40	DC Offset Control
0x0C	DC_DAC7 0	DC_DAC6 0	DC_DAC5 0	DC_DAC4 0	DC_DAC3 0	DC_DAC2 0	DC_DAC1 0	DC_DAC0 0	h00	h00	DC Offset DAC
0x0D	X 0	FUSE_TH 0	X 0	WR 0	TFA <3> U	TFA <2> U	TFA <1> U	TFA <0> U	—	h00	ROM Table Address
0x0E	TFD<7> 0	TFD<6> 0	TFD<5> 0	TFD<4> 0	TFD<3> 0	TFD<2> 0	TFD<1> 0	TFD<0> 0	h00	h00	ROM Table Fuse Data
0x0F	X 0	X 0	X 0	X 0	MX_HR<3> 0	MX_HR<2> 0	MX_HR<1> 0	MX_HR<0> 0	h00	h00	Mixer Harmonic Rejection
0x10	TFR<7>	TFR<6>	TFR<5>	TFR<4>	TFR<3>	TFR<2>	TFR<1>	TFR<0>	N/A	N/A	ROM Table Data Read Back
0x11	POR	VASA	VASE	LD	DC_LO	DC_HI	GKT	PD_OVLD	N/A	N/A	Chip Status Read Back
0x12	VCO1A	VCO0A	BS2A	BS1A	BS0A	ADC2	ADC1	ADC0	N/A	N/A	Autotuner Read Back

Register Descriptions

N-Divider Integer (Register Address 0x00)

N<7:0>: VCO Integer-N Divider Ratio

N-Divider Frac2 (Register Address 0x01)

MP: Minimum CP Pulse Width. Always set to 0 (factory use only).

LI1, LI0; CP Linearity Control. Always set to 00 (factory use only).

INT: Integer Mode ON/OFF. Set to 0 for normal operation.

F<19:16>: MSB of Main Divider Fractional Divide Ratio

N-Divider Frac1, Frac0 (Register Address 0x02, 0x03)

F<15:0> 16 LSB of Main Divider Fractional Divide Ratio

Tracking Filter Series Capacitor (Register Address 0x04)

TFS<7:4>: Tracking Filter Parallel Capacitor.

TFS<3:0>: Tracking Filter Series Capacitor.

See the RF tracking filter description in the *Applications Information* section.

Tracking Filter Parallel Capacitor and VCO Control (Register Address 0x05)

VCO_DIV1, VCO_DIV0: VCO Post Divider

- 00 = Divide by 4 use for RF frequencies of 540MHz to 868MHz
- 01 = Divide by 8 use for RF frequencies of 470MHz to 550MHz
- 10 = Divide by 16 use for RF frequencies of 170MHz to 230MHz
- 11 = Divide by 32 is not used

RFS: RF Input Select

- 0 = RFIN2 selected
- 1 = RFIN selected

TF_BS: Tracking Filter Band Select

- 1 = VHF band
- 0 = UHF band

TFP<4:0>: Tracking Filter Shunt Capacitor

See the RF tracking filter description in the *Applications Information* section.

PLL Configuration (Register Address 0x06)

LF_DIV2, LF_DIV1, LF_DIV0: Prescaler for Internal Low Frequency Clocks

- 000 - 110 = Divided by 8 to 14 for REF crystal frequencies of 15MHz to 28MHz
- 111 = Divide by 2 for REF crystal frequencies of 4MHz

ADLY1, ADLY0: VCO Autotuner Delay Selection

CPS: Charge-Pump Current Mode

- 0 = Controlled by ICP bit
- 1 = Controlled by VCO autotuner

ICP: Charge-Pump Current

- 0 = 600µA
- 1 = 1200µA

RDIV: PLL Reference Divider Ratio

- 0 = Divide by 1
- 1 = Divide by 2

Test Functions (Register Address 0x07)

CP_TST<2:0>: Charge-Pump Test Modes

- 000 = Normal operation
- 100 = Low impedance*
- 101 = Source
- 110 = Sink
- 111 = High impedance

LD_MUX: Lock-Detector Mode

- 000 = Normal operation: high = PLL locked, low = unlocked
- 001 = Monitor N-divider output, post-divided by 2
- 010 = Monitor R-divider output*
- 011 = Modulator test vector output (factory use only)
- 1XX = Bias current trim (factory use only)

**Not production tested.*

Shutdown Control (Register Address 0x08)

SHDN_BG: Main Bandgap

0 = Enabled

1 = Disabled

The main bandgap can and will be shut down once all other blocks are shut down (i.e., all bits in this shutdown register and bits VCO_ in the VCO Control Register and bits DC_MO_ in the DC Offset Control Register are shut down).

SHDN_PD: Baseband Power Detector

For factory use only.

Set to 1 at all times.

SHDN_RF: RF LNA/VGA:

0 = Enabled

1 = Disabled

SHDN_MIX: I/Q Mixer and LO Drivers

0 = Enabled

1 = Disabled

SHDN_BB: Baseband Filters and VGA

0 = Enabled

1 = Disabled

SHDN_SYN: Fractional PLL

0 = Enabled

1 = Disabled

SHDN_REF: Controls the Crystal Oscillator Buffered Output

0 = Enabled

1 = Disabled

The XTAL oscillator activation results from the SHDN_SYN, SHDN_REF bits: If either one is on, the XTAL oscillator runs. The XTAL oscillator is shut down only if both bits are off.

VCO Control (Register Address 0x09)

VCO<1:0>: Selects 1 of 3 VCO Bands. 00 turns off VCO block completely.

BS<2:0>: Selects 1 of 8 VCO Sub-Bands

VAS: VCO Band Autoselect

0 = VCO band select controlled by bits VCO<1:0>

1 = Controlled by autotuner

ADL: VCO ADC Latch Enable Bit

1 = Latches ADC value

0 = Default

ADE: Enable VCO Tune Voltage DAC Read

1 = Enables ADC read

0 = Default

Baseband Control (Register Address 0x0A)

PD_TH<2:0>: Detection Threshold for Baseband Power Detector

BB_BW<3:0>: Baseband Filter Bandwidth. Optimum values for 7MHz and 8MHz wide RF channels can be taken from the ROM table.

DC Offset Control (Register Address 0x0B)

DC_TH<1:0>: DC Offset Correction Thresholds. Keeps output within:

00 = Output within ±0.55V of balanced state

11 = Output within ±0.75V of balanced state

DC_SP<1:0>: DC Offset Correction Speed (or Highpass Corner Frequency).

11 = Fast (~500Hz)

01 = Slow (~20Hz)

00 = Off/hold DAC values

DC_MO<1:0>: Mode of Operation

00 = Off

10/01 = Sets I/Q channel DACs direct from register

11 = Normal operation

DC_DAC<8>: MSB for DC Offset DAC

BB_BIA: Baseband Filter Op-Amp Bias Settings

0 = Low

1 = High

DC Offset DAC (Register Address 0x0C)

DC_DAC<7:0>: Value to Program to I/Q DC Offset DAC. Note that the MSB is located in the previous register.

Tracking Filter ROM Address (Register Address 0x0D)

TFA<3:0>: Tracking Filter ROM Address. See Table 3.

Tracking Filter Write Data (Register Address 0x0E)

TFD<7:0>: Tracking Filter Data for ROM

Tracking Filter ROM Read Back (Read Only) (Register Address 0x10)

TFR<7:0>: Tracking Filter ROM Data Read Back

Status (Read Only, for Factory Use Only) (Register Address 0x11)

POR: Power-On Reset*

0 = Power has not been reset since the last read.

1 = Power has been reset since the last read. Getsreset after reading back address 8'h0C.

VASA, VASE: VCO Autotuner Status*

LD: PLL Lock Detector

0 = PLL unlocked

1 = PLL locked

DC_HI: DC Offset Correction Detected Positive Signal Excursion in Either I or Q Channel*

DC_LO: DC Offset Correction Detected Negative Signal Excursions in Either I or Q Channel*

PD_OVLD: Baseband Power Detector*

0 = Baseband signal below threshold

1 = Baseband signal above threshold

Autotuner Read Back (Read Only, for Factory Use Only) (Register Address 0x12)

VCOA<1:0> VCO Tank Selected by Autotuner*

BSA<1:0> Sub-Band VCO Selected by Autotuner*

ADC<2:0> VCO Tank Voltage ADC*

*Not production tested.

Table 3. MAX3580 Fuse Table

BYTE	7	6	5	4	3	2	1	0	DESCRIPTION
00	Unused			Bias					Bias trim
01	VHF (200MHz) parallel cap				VHF (200MHz) series cap				VHF high series cap
02	Unused				VHF (200MHz) shunt cap				VHF shunt cap
03	UHF low (470MHz) parallel cap				UHF low (470MHz) series cap				UHF low series cap low
04	UHF high (860MHz) shunt cap				UHF low (470MHz) shunt cap				UHF high/low parallel cap
05	UHF high (860MHz) parallel cap				UHF high (860MHz) series cap				UHF high series cap
06	Baseband filter UHF (8MHz) coefficient				Baseband filter VHF (7MHz) coefficient				BB filter bandwidth
07	X	X	X	X	X	X	X	RO	Read only

To Read Back Fuses

IMPORTANT NOTICE: When reading other addresses than 8'h00 (the system trim bits), it is possible that the data going to the bias cells will be disturbed due to the architecture of the fuse bank. This means the bias current could change while reading back fuse data.

1) Write 8'hXX to TFA. XX is the address of the fuse column you want to read.
2) Read 8'hXX from TFR. TFR is the Tracking Filter Read Register.
3) Repeat steps 1 and 2 for other addresses.

2-Wire Serial Interface

The MAX3580 uses a 2-wire I²C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). The serial interface allows communication between the MAX3580 and the master at clock frequencies up to 400kHz. The master initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX3580 behaves as slave devices that transfer and receive data to and from the master. Pull SDA and SCL high with external pullup resistors (1kΩ or greater) for proper bus operation.

One bit is transferred during each SCL clock cycle. A minimum of nine clock cycles are required to transfer a byte in or out of the MAX3580 (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START* and *STOP* Conditions section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX3580 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX3580 has a 7-bit slave address that must be sent to the device following a START condition to initiate communication. The slave address is determined by the state of the ADDR2 pin and is equal to 11000[ADDR2]0 (see Table 4). The eighth bit (R/$\overline{W}$) following the 7-bit address determines whether a read or write operation will occur.

The MAX3580 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/$\overline{W}$ bit (Figure 2).

Table 4. Address Configuration

ADDRESS (WRITE/READ)	ADDR2
$C0/C1_{HEX}$	0
$C4/C5_{HEX}$	1

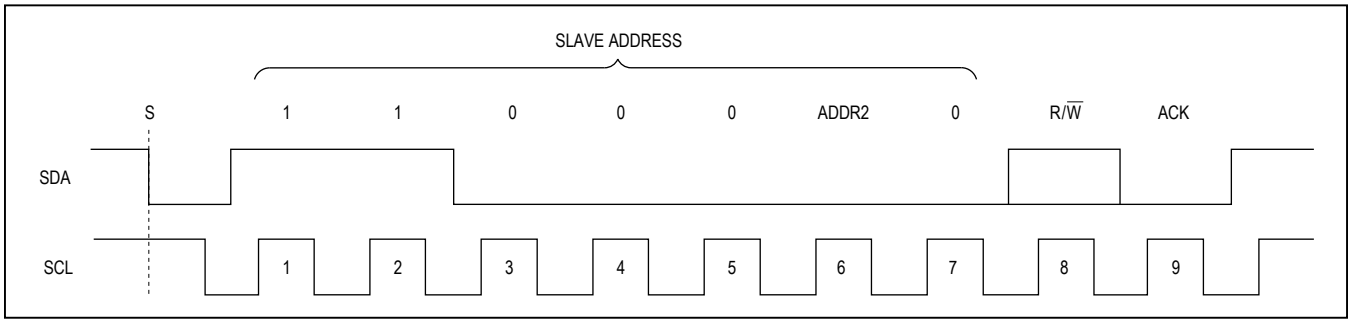


Figure 2. MAX3580 Slave Address Byte

Write Cycle

When addressed with a write command, the MAX3580 allows the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX3580 issues an ACK if the slave address byte is successfully received. The bus master must then send to the slave the address of the first register it wishes to write to. If the slave acknowledges the address, the master can then write one byte to the register at the specified address. Data is written beginning with the most significant bit. The MAX3580 again issues an ACK if the data is successfully written to the register. The master can continue to write data to the successive internal registers with the MAX3580 acknowledging each successful transfer, or it can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

Figure 3 illustrates an example in which Registers 0 through 2 are written with 0x0E, 0xD8, and 0xE1, respectively.

Read Cycle

When addressed with a read command, the MAX3580 allows the master to read back a single register or multiple successive registers.

A read cycle begins with the bus master issuing a START condition followed by the 7 slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX3580 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to read. The slave acknowledges the address. Then a START condition is issued by the master, followed by the 7 slave address bits and a read bit (R/$\overline{W}$ = 1). The MAX3580 issues an ACK if the slave address byte is successfully received. The MAX3580 starts sending data MSB first with each SCL clock cycle. At the 9th clock cycle, the master can issue an ACK, and continues to read successive registers, or the master terminates the transmission by issuing a NACK. The read cycle does not terminate until the master issues a STOP condition. Figure 4 illustrates an example in which Registers 0 through 2 are read back.

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	1100000	0		0x00		0x0E		0xD8		0xE1		

Figure 3. Example: Write Registers 0 through 2 with 0x0E, 0xD8, and 0xE1, respectively

START	DEVICE ADDRESS	R/$\overline{W}$	ACK	REGISTER ADDRESS	ACK	START	DEVICE ADDRESS	R/$\overline{W}$	ACK	REG 00 DATA	ACK	REG 01 DATA	ACK	REG 02 DATA	NACK	STOP
	11000000	0		00000000			11000000	1		xxxxxxxx		xxxxxxxx		xxxxxxxx		

Figure 4. Example: Receive Data from Read Registers

Applications Information

Band Selection

The MAX3580 is designed to be suitable for operation in the 170MHz to 230MHz VHF-III band and in the 470MHz to 878MHz UHF band.

RF Inputs

A switch selects either RFIN or RFIN2 as the input to the single-ended broadband matched LNA. This switch is programmed through the RFS bit (bit 5) of register 0x05. The LNA provides a continuous gain control range of typically 50dB before the signal is downconverted.

For optimal matching above 600MHz, add a 5nH to 6nH inductor in series with a capacitor at either of the RF input. Application Note 3700: *Front End Diplexer Filter for MAX3580* is available, detailing the implementation of a UHF and VHF simple diplexer. This simple diplexer improves strong-signal-handling capabilities of the MAX3580.

DC-Offset Cancellation

The MAX3580 features an on-chip fast-settling, DC-offset cancellation circuitry that requires no off-chip components. Note that the offset correction circuit is not enabled when the device is powered up. To enable the offset correction circuit, program the DC-Offset Control Register to the recommended default setting.

When active, the offset correction circuit creates a high-pass characteristic in the signal path with a typical corner frequency of 200Hz, and the residual DC offset can be as high as ±70mV.

Gain Control

The MAX3580 features two VGA circuits that can be used to achieve the optimum SNR. The two circuits can be driven independently by the baseband controller, which allows balancing the gain based on SNR measurements in the digital demodulator. If only one gain control voltage can be provided by the digital demodulator, see Figure 1. See the *Baseband Power Detector* section. In this operation mode, the baseband gain is set by an amplitude detector in the digital demodulator.

Baseband Power Detector

Maxim recommends disabling this feature. See explanation in the *Shutdown Control (Register Address 0x08)* section and Table 2 (address 0x08, bit D5). For single-loop AGC control, see Figure 1.

Synthesizer Loop Filters

A second-order lowpass loop filter is used to connect the PLL to the RF local oscillator. A loop filter bandwidth of 30kHz is optimal for fractional PLL spurs and integrated LO phase noise. Refer to the MAX3580 Evaluation Kit data sheet for the recommended loop-filter component values.

Crystal-Oscillator Interface

The MAX3580 reference oscillator circuitry can be used either as a high-impedance reference input driven by an external source, or be configured as a crystal oscillator. In the latter case, the resulting frequency can be used to drive the digital demodulator chip through the buffered reference output of the MAX3580. When using an external reference oscillator, drive the XB input through an AC-coupling capacitor with amplitude of approximately $1.5V_{P-P}$, and leave XE unconnected. Note that the phase noise of the external reference needs to exceed -140dBc/Hz at offsets of 1kHz to 100kHz. When connecting directly to a crystal, see the *Typical Application Circuit* for the required topology. For particular capacitor values, possible changes to accommodate for different crystal frequencies, crystal load-capacitance requirements, and crystal power-dissipation requirements, refer to the MAX3580 EV kit data sheet.

RF Tracking Filter

The MAX3580 utilizes two narrowband RF tracking filters, one for VHF and one for UHF. Each filter is comprised of a fixed inductor and three digitally controlled variable capacitors named series, shunt, and parallel capacitors.

The integrated RF tracking filters uses an external inductor between IND1 and IND2 pins to set the filter's center frequency. The inductor value must be 68nH ±2% in order to achieve the corner frequency response. The variable capacitors are factory calibrated to this particular inductor value. The value of each capacitor is also set to compensate for process variation of each individual part and to receive the desired RF channel.

The process variation is factory calibrated by determining the best capacitor values for three discrete frequencies, which are stored in the on-chip ROM table. Upon power-up these values (6 bytes total) have to be read out of the MAX3580 ROM table and stored in the microprocessor local memory.

When tuning the MAX3580 to a given Rx frequency, the correct capacitor value has to be calculated using the following linear formulas and written to the appropriate registers. This is in addition to programming the PLL with the desired frequency.

The formulas differ for VHF and UHF bands but are the same for all three capacitor values. Since the factory calibration coefficients stored on the MAX3580 can differ for each capacitor, the calculations have to be executed for all three capacitor values separately.

VHF: Capacitor = ROM_value_VHF - (RX_frequency_in_MHz - 200MHz)/10MHz

In other words, the capacitor values to be written to the MAX3580 decrease 1 count per 10MHz above 200MHz and increase accordingly below 200MHz.

UHF: Capacitor = ROM_value_UHF_lo - (ROM_value_UHF_lo - ROM_value_UHF_hi) x (RX_frequency_in_MHz - 470MHz)/390MHz

Chip Information

PROCESS: BiCMOS

This means the capacitor values stored in the UHF_lo entries of the MAX3580 ROM table are the correct values for 470MHz reception and the UHF_hi values for 860MHz reception. For any frequency in between, the capacitor values are obtained by a simple linear interpolation.

Note: When tuning to frequencies above 860MHz channel center frequency, do not use the formula above, but rather keep programming the tracking filter with the coefficients obtained for 860MHz.

Examples: Assuming the MAX3580 ROM table entries are C_{SERIES} VHF = 8, C_{SERIES} UHF_lo = 15, C_{SERIES} UHF_hi = 3.

208MHz: C_{SERIES} = 8 - round ((208-200)/10) = 7 (floating point division, round to nearest integer after division)

8 - floor ((208 - 200 + 5)/10) = 7
(all calculations using signed integer values, truncate result of division)

677MHz: C_{SERIES} = 15 - round ((15-3) x (677-470)/390) = 9 (floating point division, round to nearest integer after division) 15 - floor (((15-3) x (677 - 470) + 195)/390) = 9 (all calculations using signed integer values, truncate result of division)

Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at the central V_{CC} node. The V_{CC} traces branch out from this node, with each trace going to separate V_{CC} pins of the MAX3580. Next to each V_{CC} pin is a bypass capacitor with a low impedance to ground at the frequency of interest. Use at least one via per bypass capacitor for a low-inductance ground connection.

The three ground pins (GND_PLL, GND_CP, GND_TUNE) must be connected to the ground plane by separate via holes and must not be directly connected to the exposed pad.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+5	21-0140	90-0013

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/06	Initial release	—
1	5/07	Various changes	1, 4, 5, 20, 21
2	8/07	Various changes	2, 5
3	10/07	Various changes	3, 20, 21
4	3/08	Updated *AC Electrical Characteristics*, corrected *Pin Description*, added Figure 1, updated Figure references, various other changes	1, 2, 5, 7–13, 15, 17–19
5	8/08	Restricted PLL N-divider range and widened I/Q output DC common mode range	3, 5, 15
6	11/08	Added note to *Programmable Registers* section to avoid mistuning the VCO during a channel change	12
7	1/09	Updated Note 1 to specify part tested at hot temperature only	1–5
8	9/90	Corrected Overall Voltage Gain and Phase Noise specifications in the *AC Electrical Characteristics*	3
9	2/10	Updated Overall Voltage Gain, Rejection Ratio, Output DC Offset, and Note 1 in the *AC Electrical Characteristics*; corrected OVLD_DET function in the *Pin Description*; corrected *Programmable Registers* and *Status* (*Read Only, for Factory Use Only*) (*Register Address 0x11*) sections	3, 5, 10, 12, 13, 15
10	5/14	Updated *Applications*	1

