

DDR5 SDRAM RDIMM Addendum

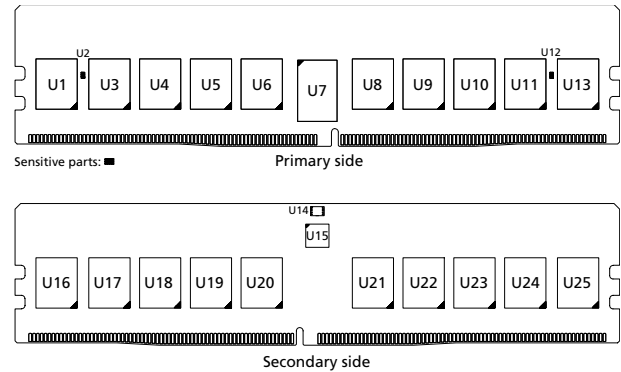
MTC20F1045S1RC – 32GB 16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800
- 32GB (4 Gig x 80)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 288-Pin DDR5 RDIMM (R/C-C0)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Frequency/CAS latency
 - 0.416ns @ CL = 40 (DDR5-4800)

Marking

C
 48B

Table 1: Addressing

Parameter	32GB
Row address ¹	64K (R0-R15)
Column address ¹	2K (C0-C10)
Device bank group address ¹	8 (BG0-BG2)
Device bank address per bank group ¹	4 (BA0-BA1)
Device configuration	16Gb (4Gb x 4), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT60B4G4,¹ 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL _n -RCD _n -RP)
MTC20F1045S1RC48BA2	32GB	4Gb x 80 (EC8)	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on micron.com.



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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3A	154	U3	0	11A	165
	1	0A	7		1	8A	18
	2	1A	9		2	9A	20
	3	2A	152		3	10A	163
U4	0	19A	176	U5	0	27A	187
	1	16A	29		1	24A	40
	2	17A	31		2	25A	42
	3	18A	174		3	26A	185
U6	0	CB3A	198	U8	0	CB3B	243
	1	CB0A	51		1	CB0B	96
	2	CB1A	53		2	CB1B	98
	3	CB2A	196		3	CB2B	241
U9	0	7B	254	U10	0	15B	265
	1	4B	107		1	12B	118
	2	5B	109		2	13B	120
	3	6B	252		3	14B	263
U11	0	23B	276	U13	0	31B	287
	1	20B	129		1	28B	140
	2	21B	131		2	29B	142
	3	22B	274		3	30B	285
U16	0	24B	133	U17	0	16B	122
	1	27B	280		1	19B	269
	2	26B	278		2	18B	267
	3	25B	135		3	17B	124
U18	0	8B	111	U19	0	0B	100
	1	11B	258		1	3B	247
	2	10B	256		2	2B	245
	3	9B	113		3	1B	102
U20	0	CB4B	89	U21	0	CB4A	58
	1	CB7B	236		1	CB7A	205
	2	CB6B	234		2	CB6A	203
	3	CB5B	91		3	CB5A	60



Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U22	0	28A	47	U23	0	20A	36
	1	31A	194		1	23A	183
	2	30A	192		2	22A	181
	3	29A	49		3	21A	38
U24	0	12A	25	U25	0	4A	14
	1	15A	172		1	7A	161
	2	14A	170		2	6A	159
	3	13A	27		3	5A	16



I_{DD} Specifications

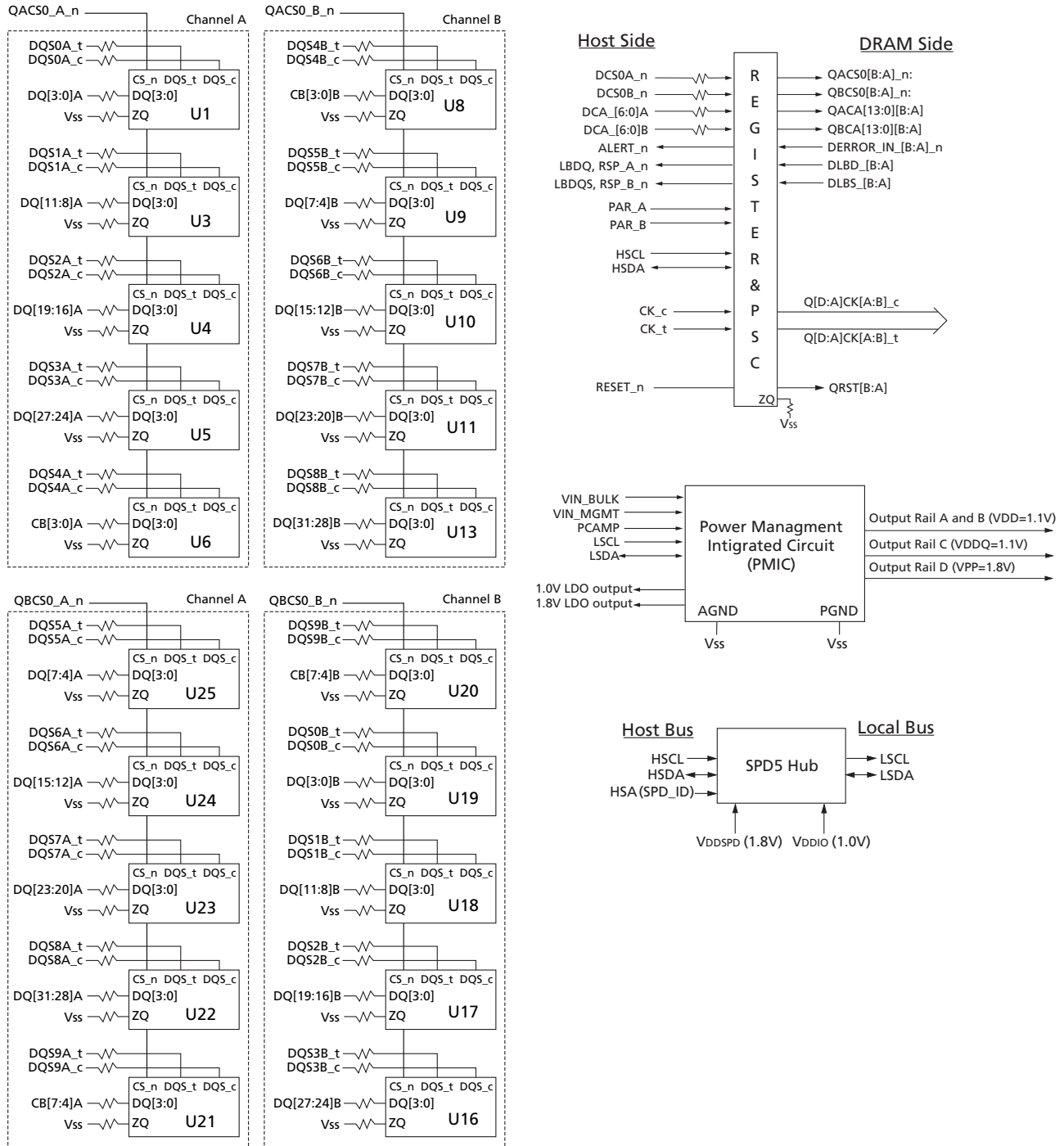
Table 4: DDR5 I_{DD} Specifications and Conditions – 32GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I _{DD0}	191	mA
Operating four bank ACTIVATE-PRECHARGE current	I _{DD0F}	282	mA
Precharge standby current	I _{DD2N}	156	mA
Precharge standby non-target command	I _{DD2NT}	313	mA
Precharge power-down current	I _{DD2P}	144	mA
Active standby current	I _{DD3N}	178	mA
Active power-down current	I _{DD3P}	167	mA
Operating burst read current	I _{DD4R}	645	mA
Operating burst write current	I _{DD4W}	821	mA
Operating burst write with write CRC current	I _{DD4WC}	843	mA
Burst refresh (normal refresh mode) current	I _{DD5B}	519	mA
Burst refresh (fine granularity refresh mode) current	I _{DD5F}	327	mA
Burst refresh (same bank refresh mode) current	I _{DD5C}	239	mA
Self refresh current	I _{DD6N}	74	mA
Operating bank interleave read current	I _{DD7}	749	mA
Maximum power saving deep power down mode current	I _{DD8}	84	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



- Notes:
1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
 2. Functional block diagram is for reference only.



Revision History

Rev. E – 09/2021

- Production Release

Rev. D – 02/2021

- Preliminary Release

Rev. C – 01/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006
208-368-4000, micron.com/support

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.