

## 54FCT573

### Octal D-Type Latch with TRI-STATE® Outputs

#### General Description

The 'FCT573 is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

This device is functionally identical to the 'FCT373 but has different pinouts.

#### Features

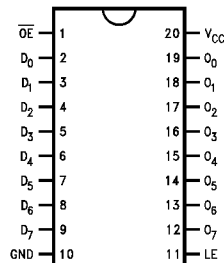
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- TTL input and output level compatible
- CMOS power consumption
- Functionally identical to 'FCT373
- TRI-STATE outputs for bus interfacing
- Output sink capability of 32 mA, source capability of 12 mA
- Standard Microcircuit Drawing (SMD) 5962-8863901

#### Ordering Code

Military	Package Number	Package Description
54FCT573DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT573FMQB	W20A	20-Lead Cerpack
54FCT573LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

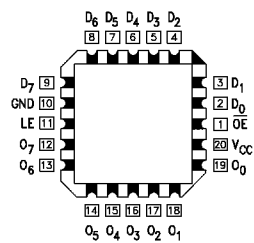
#### Connection Diagram

Pin Assignment  
for DIP and Cerpack



DS100951-1

Pin Assignment  
for LCC



DS100951-39

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

## Functional Description

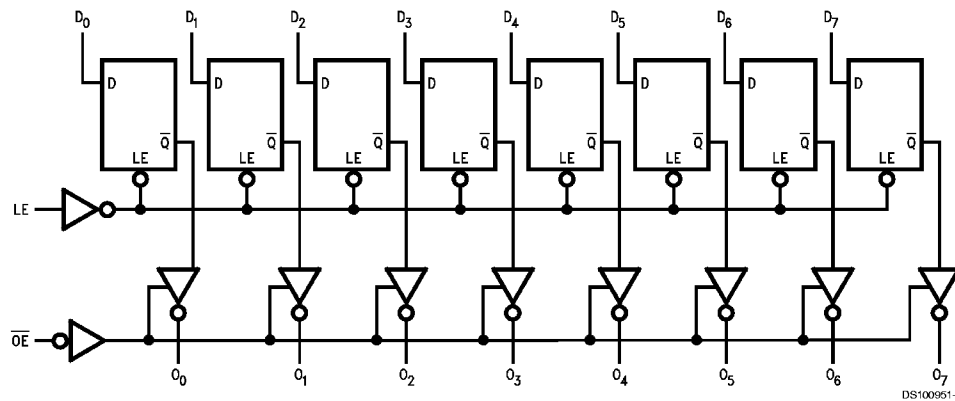
The 54FCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	$O_0$
H	X	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 $O_0$  = Value stored from previous clock cycle

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100951-3

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output	

in LOW State (Max)	Twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	FCT573			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54FCT	4.3		V	Min	I <sub>OH</sub> = -300 μA
		54FCT	2.4				I <sub>OH</sub> = -12 mA
V <sub>OL</sub>	Output LOW Voltage	54FCT		0.2	V	Min	I <sub>OL</sub> = 300 μA
		54FCT		0.5			I <sub>OL</sub> = 32 mA
I <sub>IH</sub>	Input HIGH Current		5		μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>IL</sub>	Input LOW Current		-5		μA	Max	V <sub>IN</sub> = 0.0V
I <sub>OZH</sub>	Output Leakage Current		50		μA	0 – 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}$ = 2.0V
I <sub>OZL</sub>	Output Leakage Current		-50		μA	0 – 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current		-60		mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CCQ</sub>	Quiescent Power Supply Current		1.5		mA	Max	V <sub>IN</sub> < 0.2V or V <sub>IN</sub> 5.3V, V <sub>CC</sub> = 5.5V
ΔI <sub>CC</sub>	Quiescent Power Supply Current		2.0		mA	Max	V <sub>I</sub> = 3.4V, V <sub>CC</sub> = 5.5V
I <sub>CCD</sub>	Dynamic I <sub>CC</sub>		0.4		mA/MHz	Max	Outputs Open, V <sub>CC</sub> = 5.5V, V <sub>IN</sub> 5.3V or V <sub>IN</sub> < 0.2V, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, LE = V <sub>CC</sub>
I <sub>CC</sub>	Total Power Supply Current		6.0		mA	Max	Outputs Open, f <sub>CP</sub> = 10 MHz, V <sub>CC</sub> = 5.5V, V <sub>IN</sub> 5.3V or V <sub>IN</sub> < 0.2V, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, LE = V <sub>CC</sub>

## AC Electrical Characteristics

Symbol	Parameter	54FCT		Units	Fig. No.
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max		
$t_{PLH}$	Propagation Delay	1.0	8.5	ns	Figure 4
$t_{PHL}$	$D_n$ to $O_n$	1.0	8.5		
$t_{PLH}$	Propagation Delay	1.0	15.0	ns	Figure 4
$t_{PHL}$	LE to $O_n$	1.0	15.0		
$t_{PZH}$	Output Enable Time	1.0	13.5	ns	Figure 6
$t_{PZL}$		1.0	13.5		
$t_{PHZ}$	Output Disable Time	1.0	10.0	ns	Figure 6
$t_{PLZ}$	Time	1.0	10.0		

## AC Operating Requirements

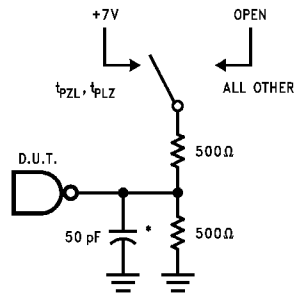
Symbol	Parameter	54FCT		Units	Fig. No.
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max		
$t_s(H)$	Set Time, HIGH	2.0		ns	Figure 7
$t_s(L)$	or LOW $D_n$ to LE	2.0			
$t_h(H)$	Hold Time, HIGH	1.5		ns	Figure 7
$t_h(L)$	or LOW $D_n$ to LE	1.5			
$t_w(H)$	Pulse Width, LE HIGH	6.0		ns	Figure 5

## Capacitance

Symbol	Parameter	Max	Units	Conditions ( $T_A = 25^\circ\text{C}$ )
$C_{IN}$	Input Capacitance	10	pF	$V_{CC} = 0\text{V}$
$C_{OUT}$ (Note 3)	Output Capacitance	12	pF	$V_{CC} = 5.0\text{V}$

**Note 3:**  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$  per MIL-STD-883B, Method 3012.

### AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Test Load

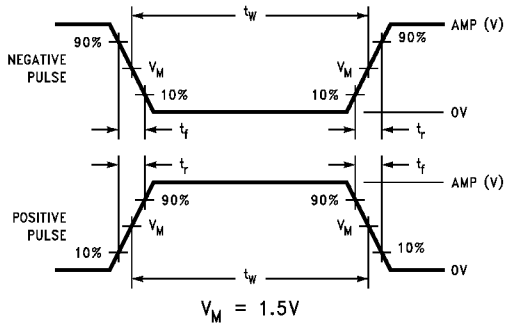


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

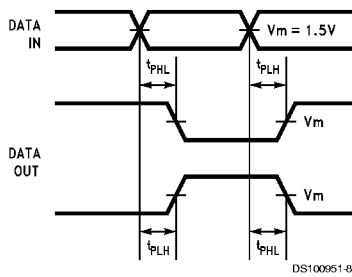


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

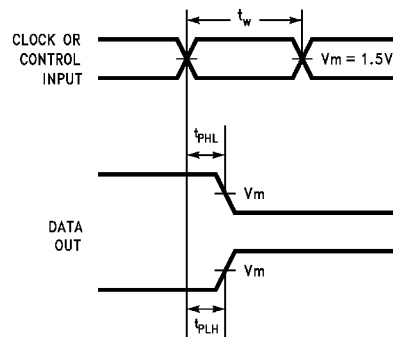


FIGURE 5. Propagation Delay, Pulse Width Waveforms

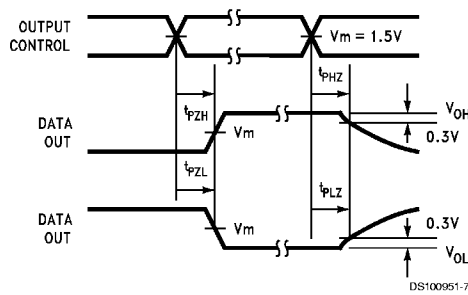


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

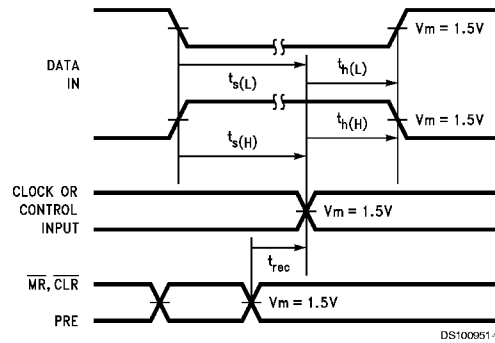
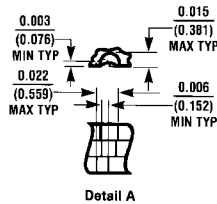
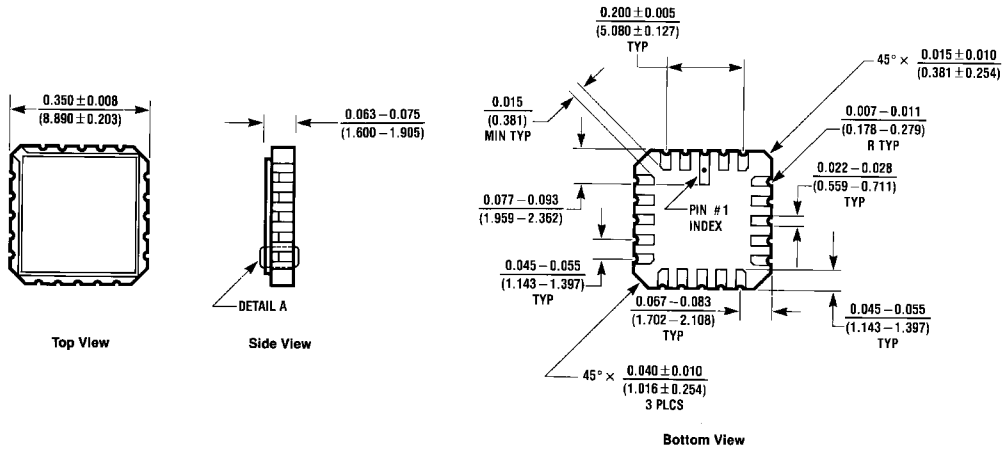


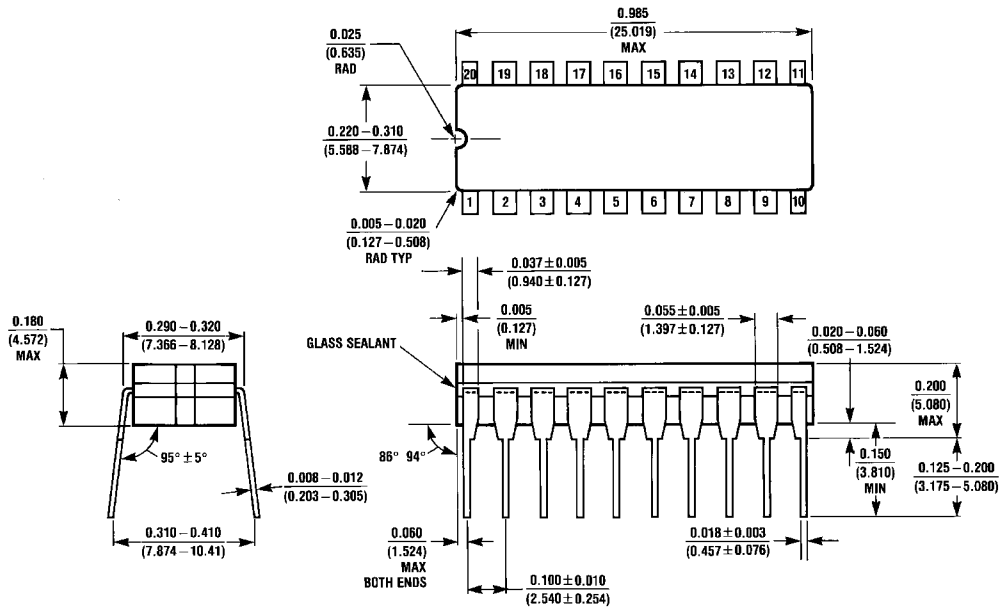
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

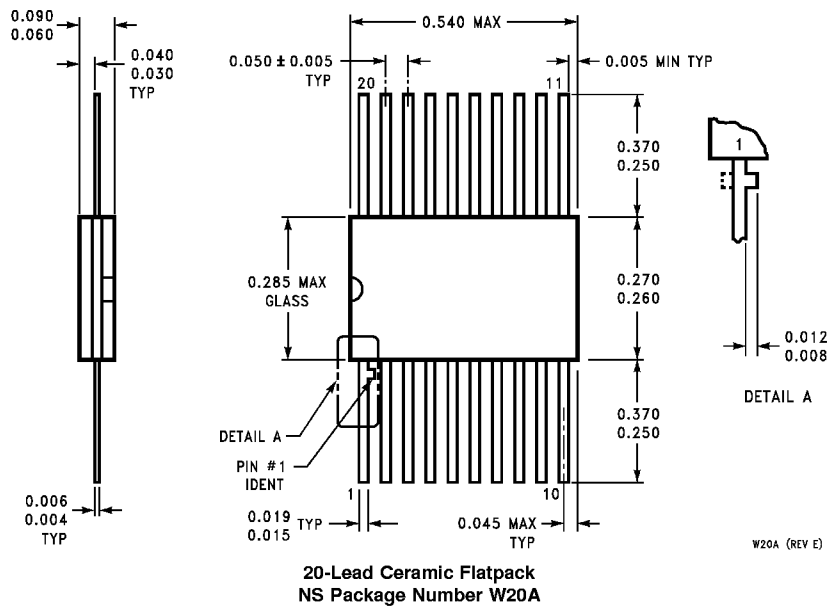
**20-Lead Ceramic Leadless Chip Carrier**  
 NS Package Number E20A



J20A (REV M)

**20-Lead Ceramic Dual-In-Line**  
 NS Package Number J20A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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Americas  
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Fax: 1-800-737-7018  
Email: support@nsc.com

www.national.com

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