

74AC125, 74ACT125

Quad Buffer with 3-STATE Outputs

Features

- I_{CC} reduced by 50%
- Outputs source/sink 24mA
- ACT125 has TTL-compatible outputs

General Description

The AC/ACT125 contains four independent non-inverting buffers with 3-STATE outputs.

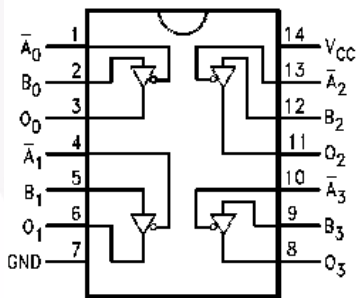
Ordering Information

Order Number	Package Number	Package Description
74AC125SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC125PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT125SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT125PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

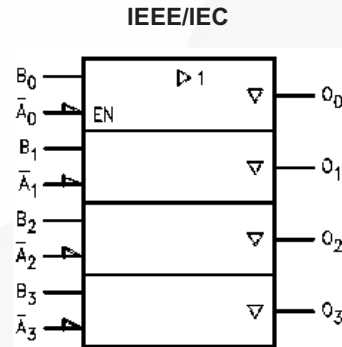
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
\bar{A}_n, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level, L = LOW Voltage Level
Z = HIGH Impedance, X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$	-20mA
	$V_I = V_{CC} + 0.5$	+20mA
V_I	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$	-20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 50mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.1	2.1		V
		4.5		2.25	3.15			
		5.5		2.75	3.85			
V _{IL}	Maximum LOW Level Input Voltage	3.0	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.9	0.9		V
		4.5		2.25	1.35			
		5.5		2.75	1.65			
V _{OH}	Minimum HIGH Level Output Voltage	3.0	I _{OUT} = -50μA	2.99	2.9	2.9		V
		4.5		4.49	4.4			
		5.5		5.49	5.4			
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA		2.56	2.46		
		4.5			3.86	3.76		
		5.5			4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	3.0	I _{OUT} = 50μA	0.002	0.1	0.1		V
		4.5		0.001	0.1			
		5.5		0.001	0.1			
		3.0	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA		0.36	0.44		
		4.5			0.36	0.44		
		5.5			0.36	0.44		
I _{IN} ⁽³⁾	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{OZ}	Maximum 3-STATE Current	5.5	V _I (OE) = V _{IL} , V _{IH} , V _I = V _{CC} , V _{GND} , V _O = V _{CC} , GND		±0.25	±2.5		μA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA
I _{CC} ⁽³⁾	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA		3.86	3.76		
		5.5		V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽⁴⁾		4.86	4.76	
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA		0.36	0.44		
		5.5		V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾		0.36	0.44	
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{OZ}	Maximum 3-STATE Current	5.5	V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND		±0.5	±5.0		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V ⁽⁶⁾	0.6		1.5		mA
I _{OLD}	Minimum Dynamic Output Current ⁽⁵⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			-75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- May be measured per the JEDEC Alternate Method.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) ⁽⁷⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay, Data to Output	3.3	1.0	6.5	9.0	1.0	10.0	ns
		5.0	1.0	5.5	7.0	1.0	7.5	
t _{PHL}	Propagation Delay, Data to Output	3.3	1.0	6.5	9.0	1.0	10.0	ns
		5.0	1.0	5.0	7.0	1.0	7.5	
t _{PZH}	Output Enable Time	3.3	1.0	6.0	10.5	1.0	11.0	ns
		5.0	1.0	5.0	7.0	1.0	8.0	
t _{PZL}	Output Enable Time	3.3	1.0	7.5	10.0	1.0	11.0	ns
		5.0	1.0	5.5	8.0	1.0	8.5	
t _{PHZ}	Output Disable Time	3.3	1.0	7.5	10.0	1.0	10.5	ns
		5.0	1.0	6.5	9.0	1.0	9.5	
t _{PLZ}	Output Disable Time	3.3	1.0	7.5	10.5	1.0	11.5	ns
		5.0	1.0	6.5	9.0	1.0	9.5	

Note:

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) ⁽⁸⁾	T _A = +25°C, C _L = 50pF			T _A = -40°C to +85°C, C _L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay, Data to Output	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay, Data to Output	5.0	1.0	7.0	9.0	1.0	10.0	ns
t _{PZH}	Output Enable Time	5.0	1.0	6.0	8.5	1.0	9.5	ns
t _{PZL}	Output Enable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns
t _{PHZ}	Output Disable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns
t _{PLZ}	Output Disable Time	5.0	1.0	7.5	10.0	1.0	10.5	ns

Note:

8. Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0V	45.0	pF

Physical Dimensions

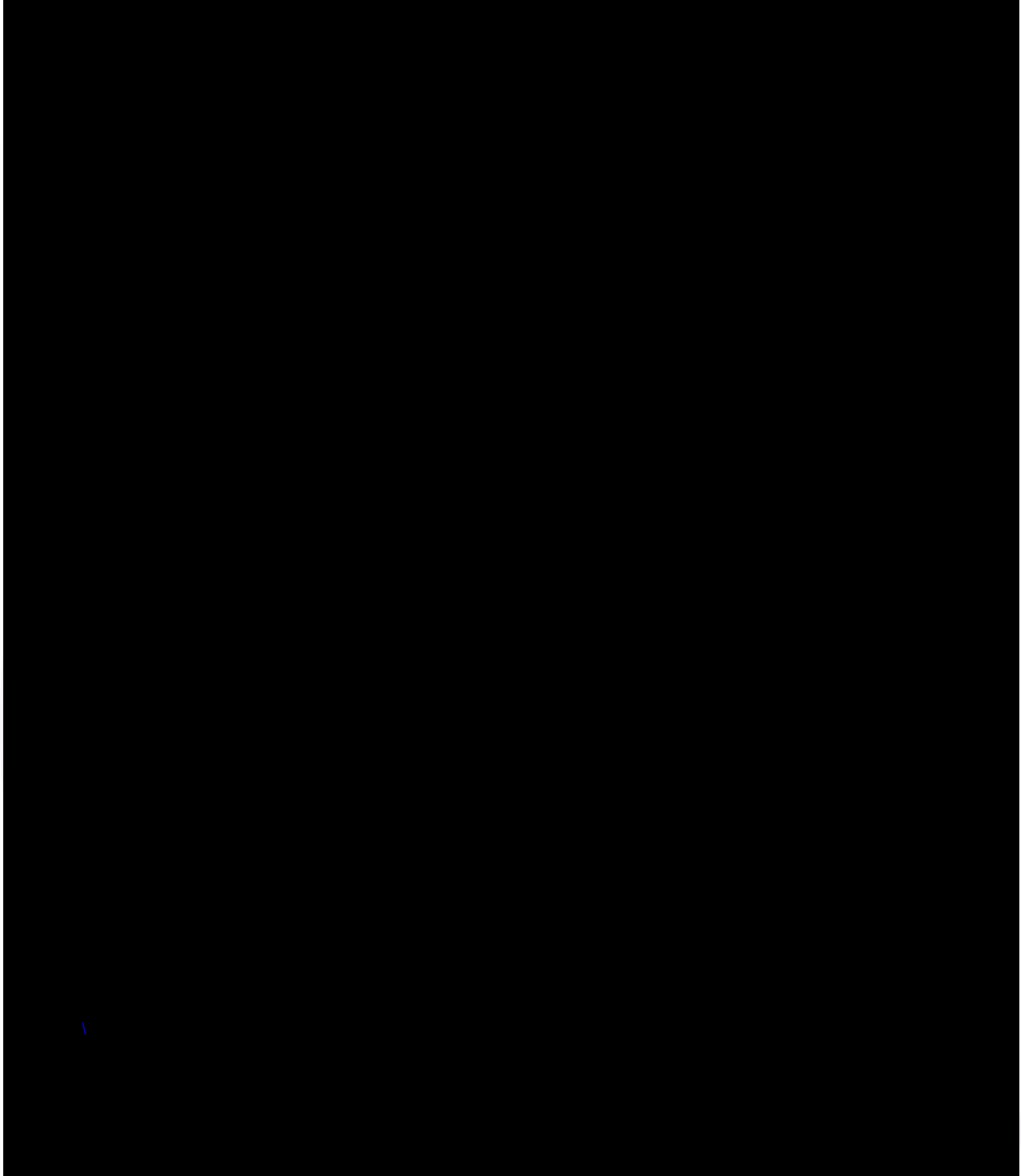


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)

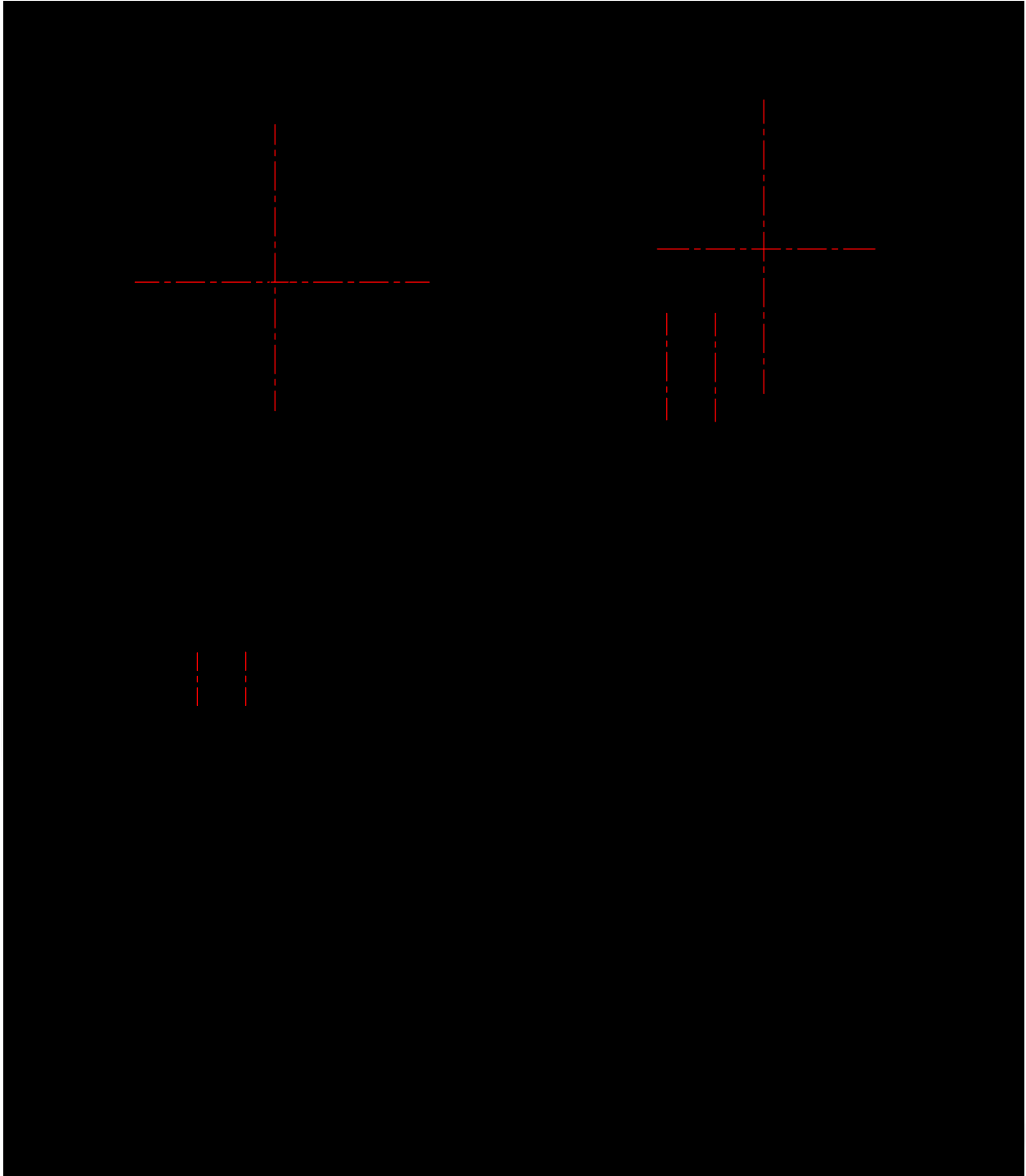


Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

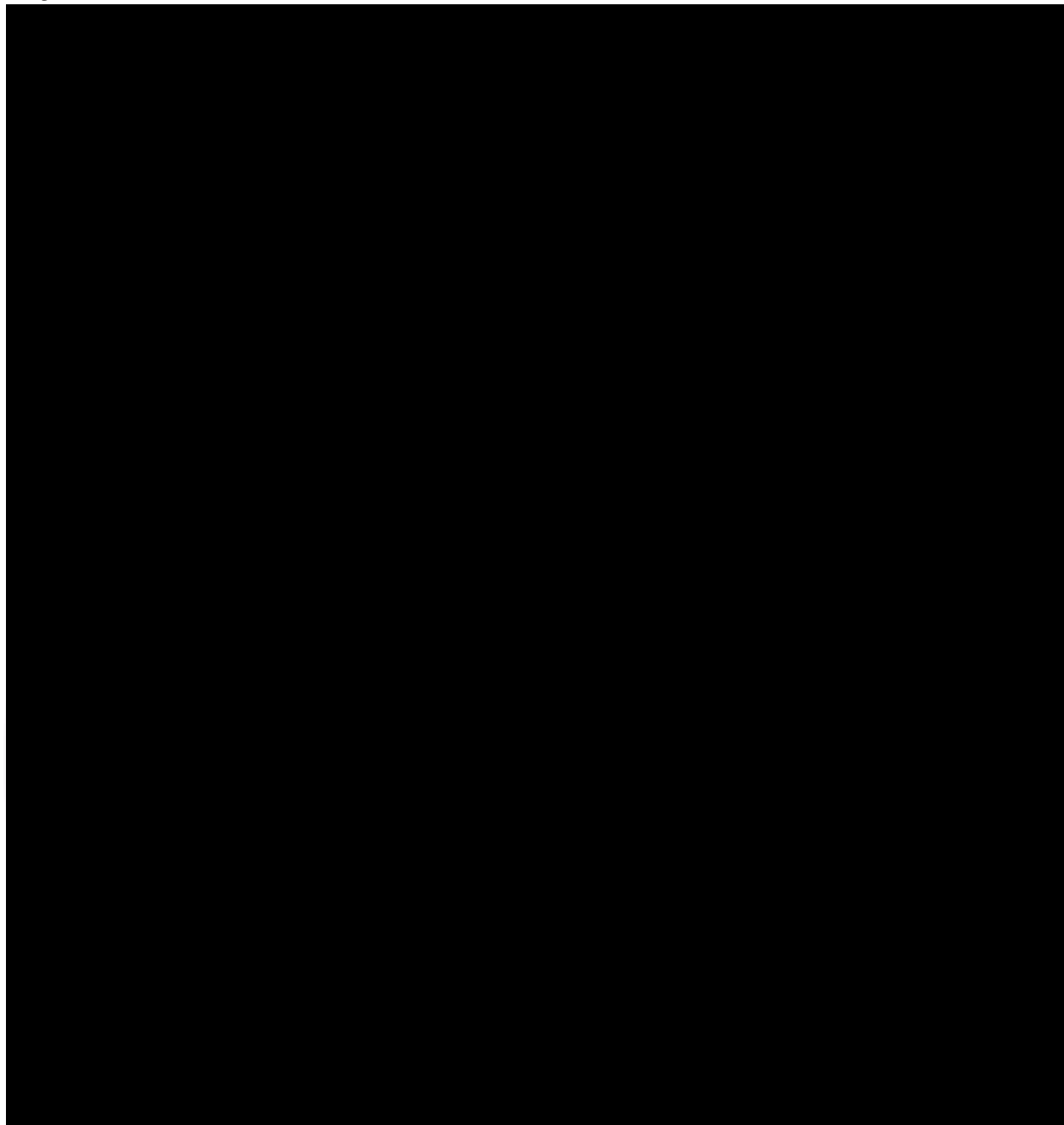
Physical Dimensions (Continued)

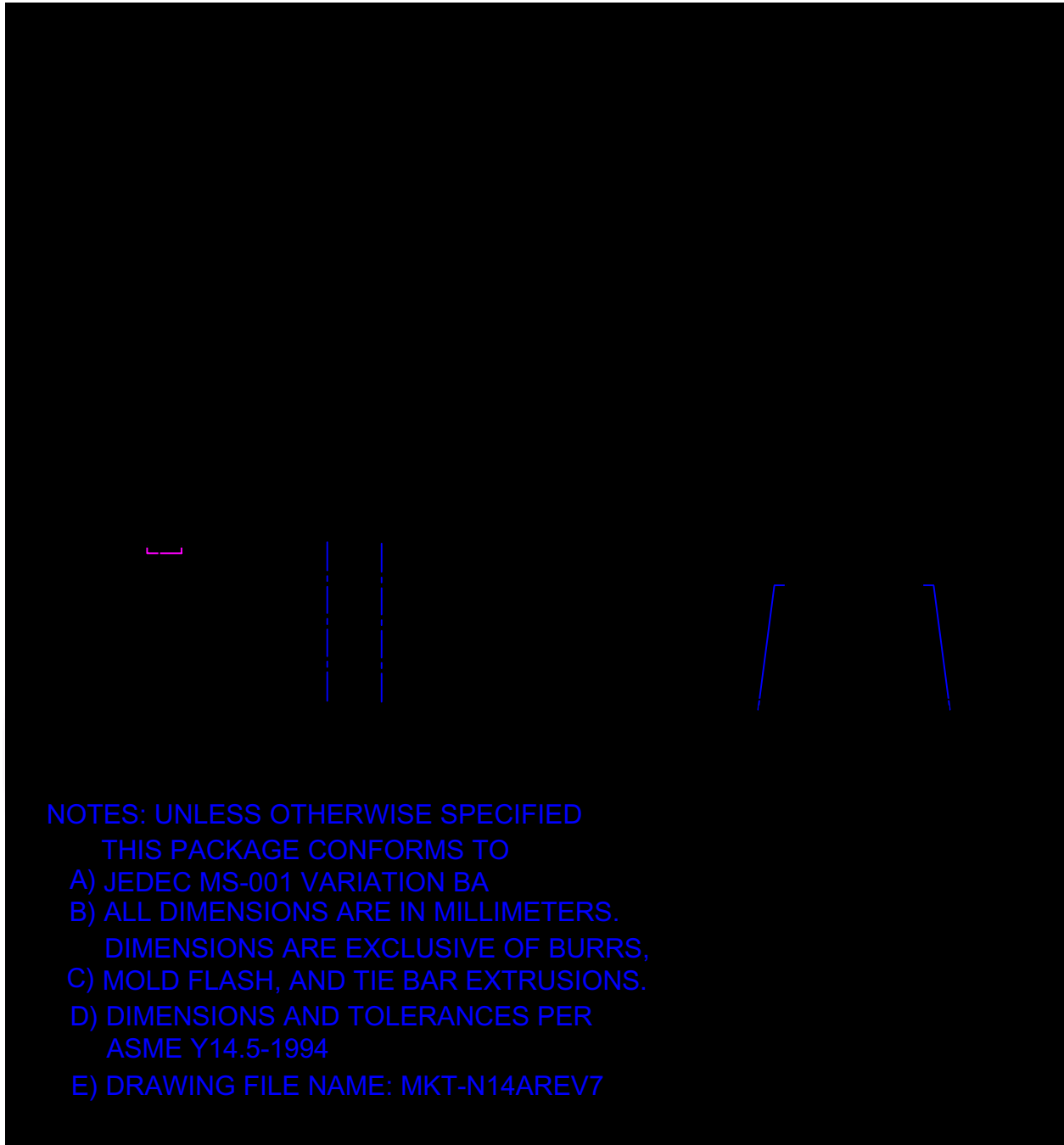
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED
 THIS PACKAGE CONFORMS TO
 A) JEDEC MS-001 VARIATION BA
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 DIMENSIONS ARE EXCLUSIVE OF BURRS,
 C) MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D) DIMENSIONS AND TOLERANCES PER
 ASME Y14.5-1994
 E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide



Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|---|--|--|----------------------------------|
| ACE [®] | FPST [™] | PDP-SPM [™] | SyncFET [™] |
| Build it Now [™] | FRFET [®] | Power220 [®] | SYSTEM [®] |
| CorePLUS [™] | Global Power Resource SM | Power247 [®] | GENERAL [®] |
| CROSSVOLT [™] | Green FPS [™] | POWEREDGE [®] | The Power Franchise [®] |
| CTL [™] | Green FPS [™] e-Series [™] | Power-SPM [™] | the power [™] |
| Current Transfer Logic [™] | GTO [™] | PowerTrench [®] | franchise |
| EcoSPARK [®] | i-Lo [™] | Programmable Active Droop [™] | TinyBoost [™] |
| EZSWITCH [™] * | IntelliMAX [™] | QFET [®] | TinyBuck [™] |
|  ™ | ISOPLANAR [™] | QS [™] | TinyLogic [®] |
|  ™ | MegaBuck [™] | QT Optoelectronics [™] | TINYOPTO [™] |
| Fairchild [®] | MICROCOUPLER [™] | Quiet Series [™] | TinyPower [™] |
| Fairchild Semiconductor [®] | MicroFET [™] | RapidConfigure [™] | TinyPWM [™] |
| FACT Quiet Series [™] | MicroPak [™] | SMART START [™] | TinyWire [™] |
| FACT [®] | MillerDrive [™] | SPM [®] | SerDes [™] |
| FAST [®] | Motion-SPM [™] | STEALTH [™] | UHC [®] |
| FastvCore [™] * | OPTOLOGIC [®] | SuperFET [™] | Ultra FRFET [™] |
| FlashWriter [®] * | OPTOPLANAR [®] | SuperSOT [™] -3 | UniFET [™] |
| | | SuperSOT [™] -6 | VCX [™] |
| | | SuperSOT [™] -8 | |

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to