

# ACPL-K30T

## Automotive Photovoltaic MOSFET Driver with R<sup>2</sup>Coupler™ Isolation



### Data Sheet



#### Description

The ACPL-K30T is specially designed to drive high-voltage MOSFETs. It consists of an AlGaAs infrared Light-Emitting Diode (LED) input stage optically coupled to an output detector circuit. The detector consists of a high-speed photovoltaic diode array and a turn-off circuit. The photovoltaic driver is turned on (contact closes) with a minimum input current of 5 mA through the input LED. The relay driver is turned off (contact opens) with an input voltage of 0.8 V or less.

ACPL-K30T is available in the stretched SO-8 package outline, designed to be compatible with standard surface mount processes.

Avago R<sup>2</sup>Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high-temperature industrial applications.

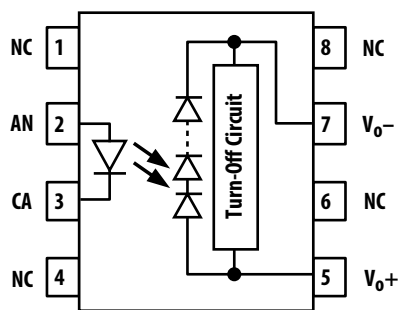


Figure 1. ACPL-K30T Functional Diagram

#### Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- Photovoltaic Driver for High Voltage MOSFETs for Automotive Application
- Open Circuit Voltage: 7 V Typical at I<sub>F</sub> = 10 mA
- Short Circuit Current: 5 μA Typical at I<sub>F</sub> = 10 mA
- Logic Circuit Compatibility
- Switching Speed: 0.8 ms (T<sub>ON</sub>), 0.04 ms (T<sub>OFF</sub>) Typical at I<sub>F</sub> = 10 mA, C<sub>L</sub> = 1 nF
- Configurable to wide portfolio of high voltage MOSFETs
- Galvanic Isolation
- High Input-to-Output Insulation Voltage
- Safety and Regulatory Approvals
  - IEC/EN/DIN EN 60747-5-5 Maximum Working Insulation Voltage 1140 V<sub>PEAK</sub>
  - 5000 V<sub>RMS</sub> for 1 minute per UL1577
  - CSA Component Acceptance

#### Applications

- Battery Insulation Resistance Measurement/Leakage Detection
- BMS Flying Capacitor Topology for Sensing Batteries
- Solid State Relay Module

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.

## Typical Application Circuit

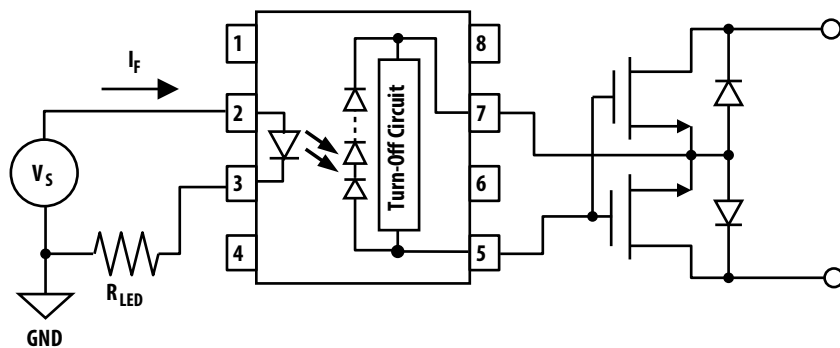
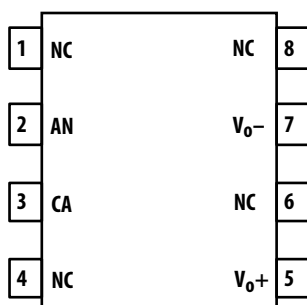


Figure 2. Application Circuit

## Package Pinout



## Pin Description

Pin No.	Pin Name	Description
2	AN	Anode
3	CA	Cathode
5	V <sub>O+</sub>	Positive Output
7	V <sub>O-</sub>	Negative Output
1, 4, 6, 8	NC	Not Connected

## Ordering Information

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 V <sub>RMS</sub> / 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K30T	-000E	Stretched	X		X		80 per tube
	-060E	SO-8	X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

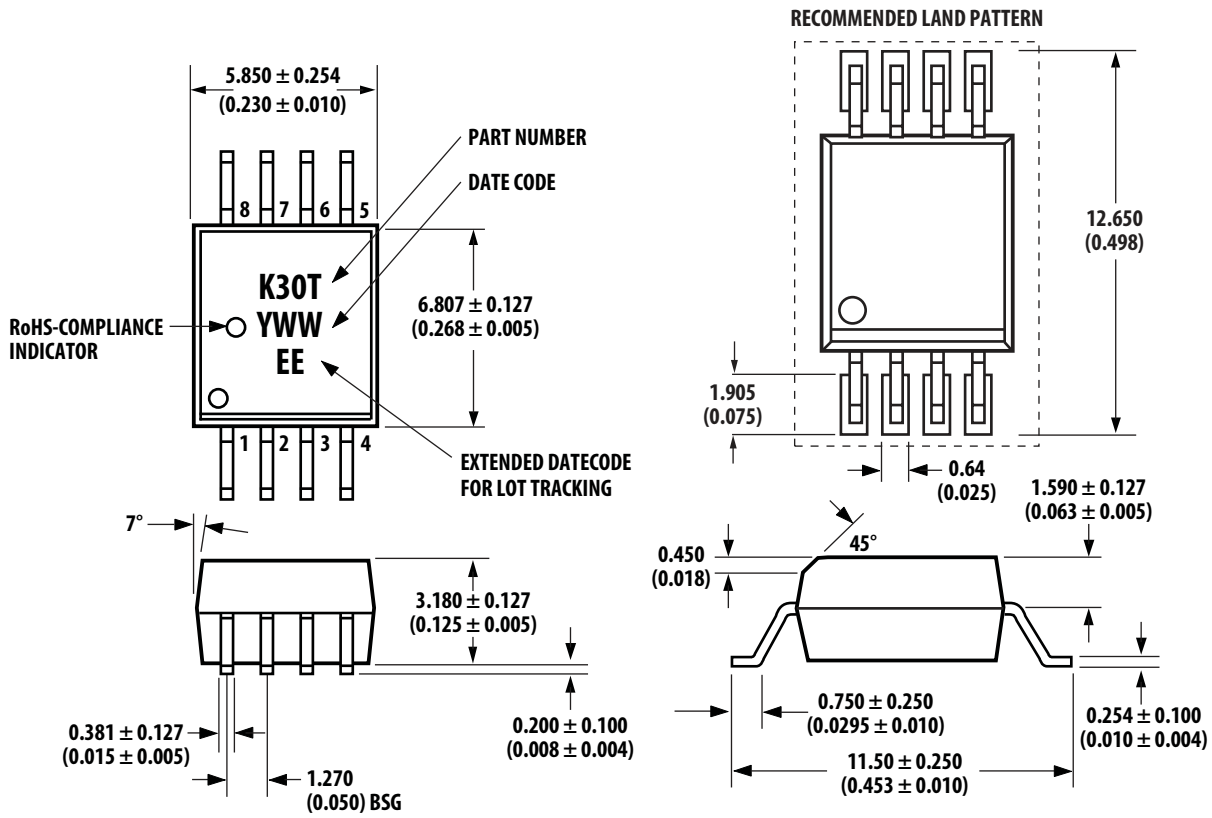
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-K30T-560E: to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings (Stretched S08)



Dimensions in millimeters and (inches).

Notes:  
 Lead coplanarity = 0.1 mm (0.004 inches).  
 Floating lead protrusion = 0.25 mm (10 mils) max.

## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard J-STD-020 (latest revision).

Note: Non-halide flux should be used.

## Regulatory Information

The ACPL-K30T is approved by the following organizations:

### UL

UL 1577, component recognition program up to  $V_{ISO} = 5 \text{ kV}_{RMS}$

### CSA

Approved under CSA Component Acceptance Notice #5

### IEC/EN/DIN EN 60747-5-5

IEC 60747-5-5  
 EN 60747-5-5  
 DIN EN 60747-5-5

## Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-K30T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

## IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060 and 560 only)

Description	Symbol	Option 060 and 560	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage < 600 V <sub>RMS</sub> for rated mains voltage < 1000 V <sub>RMS</sub>		I - IV I - III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V <sub>IORM</sub>	1140	V <sub>PEAK</sub>
Input to Output Test Voltage, Method b V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 sec Partial Discharge < 5 pC	V <sub>PR</sub>	2137	V <sub>PEAK</sub>
Input to Output Test Voltage, Method a V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and sample test, t <sub>m</sub> = 10 sec, Partial Discharge < 5 pC	V <sub>PR</sub>	1824	V <sub>PEAK</sub>
Highest Allowable Overvoltage (Transient Overvoltage, t <sub>ini</sub> = 60 sec)	V <sub>IOTM</sub>	8000	V <sub>PEAK</sub>
Safety Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T <sub>S</sub>	175	°C
Input Current	I <sub>S,INPUT</sub>	230	mA
Output Power	P <sub>S,OUTPUT</sub>	600	mW
Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V	R <sub>S</sub>	>10 <sup>9</sup>	Ω

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T <sub>S</sub>	-55	150	°C	
Operating Ambient Temperature	T <sub>A</sub>	-40	125	°C	
Input Current	Average		30	mA	
	Surge (50% duty cycle)		60	mA	
	Transient (≤ 1 μs pulse width, 300 pps)		1	A	
Reversed Input Voltage	V <sub>R</sub>		6	V	
Input Power Dissipation	P <sub>IN</sub>		60	mW	
Lead Soldering Cycle	Temperature		260	°C	
	Time		10	s	
Solder Reflow Temperature Profile	Recommended reflow condition as per JEDEC Standard J-STD-020 (latest revision)				

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Input Current (ON)	$I_{F(ON)}$	10	20	mA	
			30		Pulse width < 1 s, duty cycle < 50%
Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V	
Operating Temperature	$T_A$	-40	125	°C	

## Electrical Specifications (DC)

Unless otherwise stated, all minimum/maximum specifications are over recommended operating conditions. All typical values are at  $T_A = 25\text{ °C}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figures	Notes
Open Circuit Voltage	$V_{OC}$	4.0	7		V	$I_F = 10\text{ mA}, I_O = 0\text{ mA}$	3, 4	
		4.5				$I_F = 10\text{ mA}, I_O = 0\text{ mA}, T_A = 105\text{ °C}$		
		4.5	7.5			$I_F = 20\text{ mA}, I_O = 0\text{ mA}$	3, 4	
Temperature Coefficient of Open Circuit Voltage	$\Delta V_{OC}/\Delta T_A$		-21		mV/°C	$I_F = 10\text{ mA}, I_O = 0\text{ mA}$	4	
Short Circuit Current	$I_{SC}$	2.0	5.0		$\mu\text{A}$	$I_F = 10\text{ mA}, V_O = 0\text{ V}$	5, 6	
		4.0	10.0			$I_F = 20\text{ mA}, V_O = 0\text{ V}$	5, 6	
Input Forward Voltage	$V_F$	1.25	1.55	1.85	V	$I_F = 10\text{ mA}$		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.5		mV/°C	$I_F = 10\text{ mA}$		
Input Reverse Breakdown Voltage	$BV_R$	6			V	$I_R = 10\text{ }\mu\text{A}$		

## Switching Specifications (AC)

Unless otherwise stated, all minimum/maximum specifications are over recommended operating conditions. All typical values are at  $T_A = 25\text{ °C}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figures	Notes
Turn-On Time	$T_{ON}$		0.8	2.0	ms	$I_F = 10\text{ mA}, C_L = 1\text{ nF}$	7,10,11	
			0.4	1.0		$I_F = 20\text{ mA}, C_L = 1\text{ nF}$		
Turn-Off Time	$T_{OFF}$		0.04	0.12	ms	$I_F = 10\text{ mA}/20\text{ mA}, C_L = 1\text{ nF}$	8, 9,11	

## Package Characteristics

Unless otherwise stated, all minimum/maximum specifications are over recommended operating conditions. All typical values are at  $T_A = 25\text{ °C}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figures	Notes
Input-Output Momentary Withstand Voltage*	$V_{ISO}$	5000			$V_{RMS}$	$RH \leq 50\%, t = 1\text{ minute}, T_A = 25\text{ °C}$		1, 2
Input-Output Resistance	$R_{I-O}$	$10^9$	$10^{14}$		$\Omega$	$V_{I-O} = 500\text{ V}_{DC}$		1
Input-Output Capacitance	$C_{I-O}$		0.6		pF	$f = 1\text{ MHz}, V_{I-O} = 0\text{ V}_{DC}$		1

\* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

Notes:

- Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
- In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage > 6000  $V_{RMS}$  for 1 second.

## Typical Characteristic Plots and Test Conditions

Unless otherwise stated, all typical values are at  $T_A = 25\text{ }^\circ\text{C}$ .

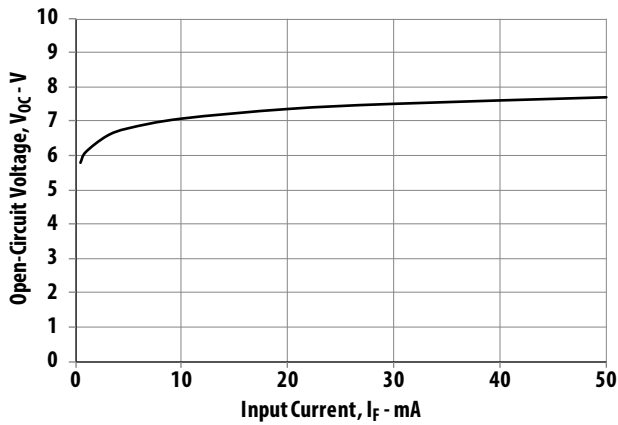


Figure 3. Open Circuit Voltage vs. Input LED Current

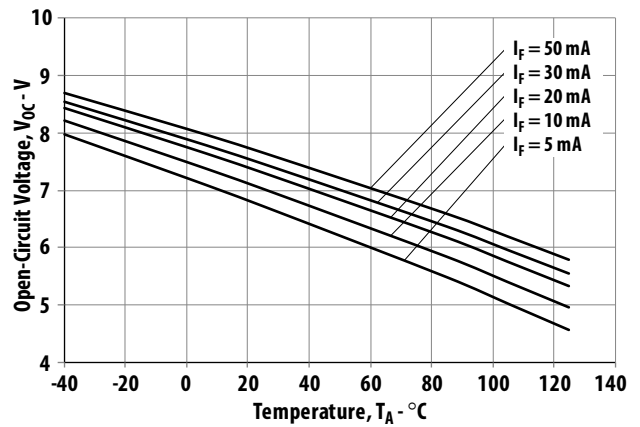


Figure 4. Open Circuit Voltage vs. Temperature

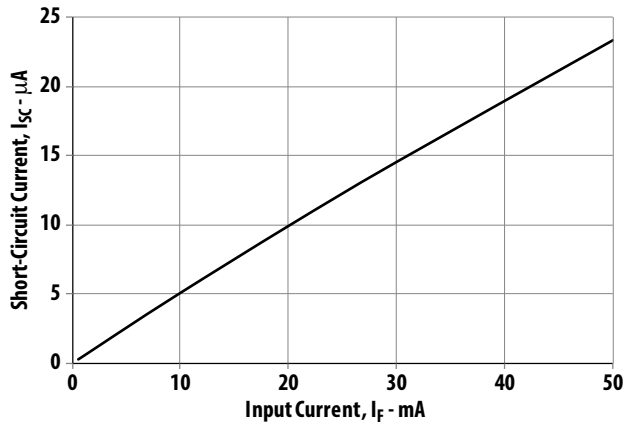


Figure 5. Short Circuit Current vs. Input LED Current

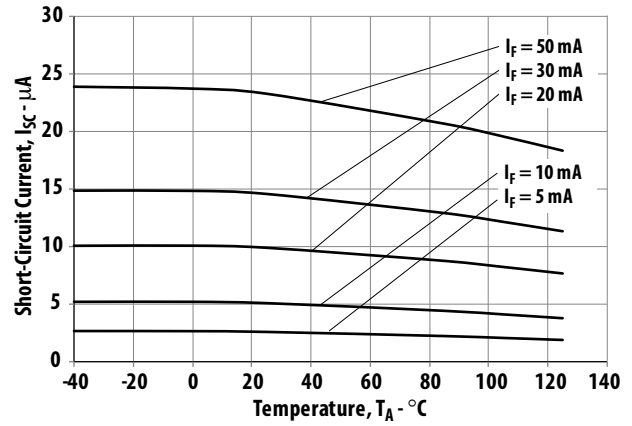


Figure 6. Short Circuit Current vs. Temperature

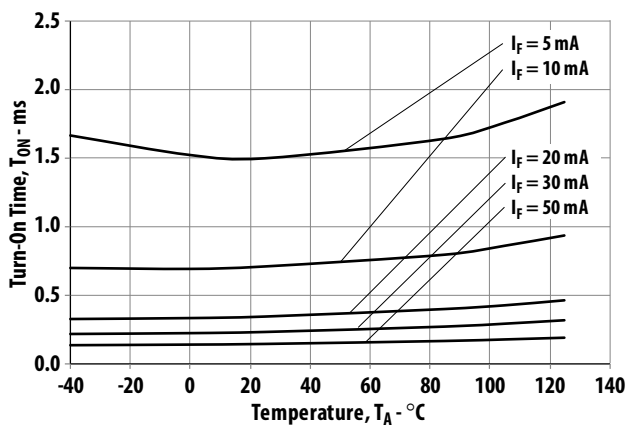


Figure 7. Turn-On Time vs. Temperature

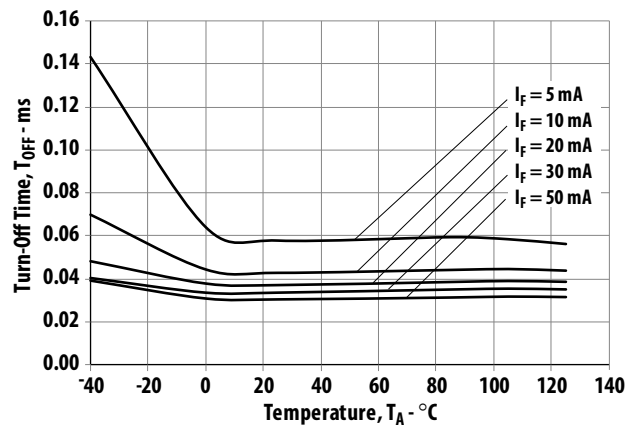


Figure 8. Turn-Off Time vs. Temperature

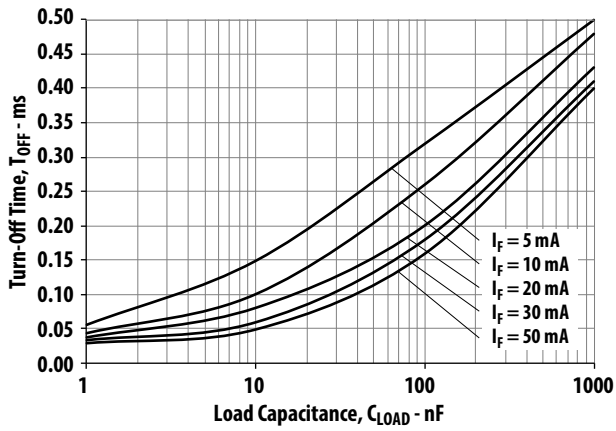


Figure 9. Turn-Off Time vs. Load Capacitance

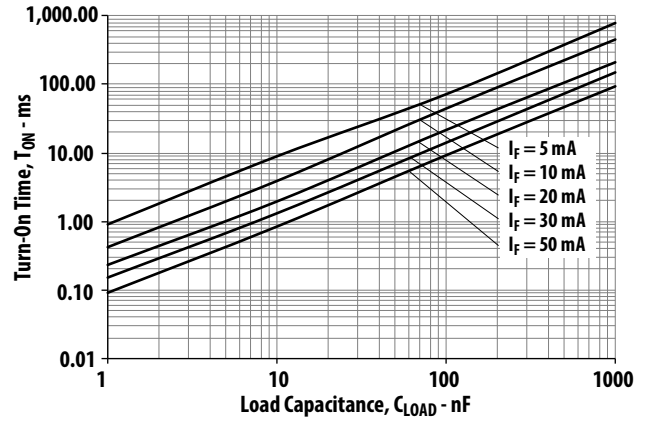


Figure 10. Turn-On Time vs. Load Capacitance

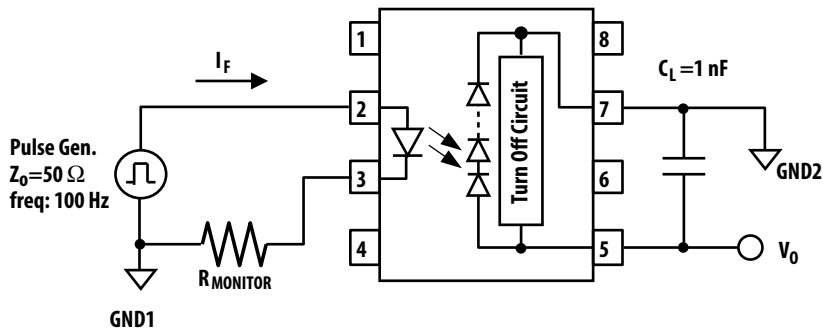
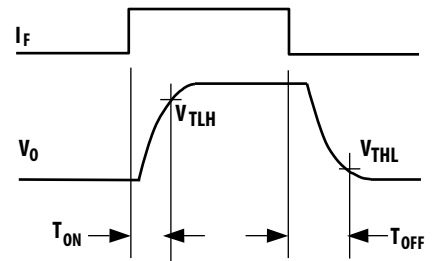


Figure 11. Switching Time Test Circuit and Waveform



Note: These are the test conditions:  
 $T_A = -40^\circ\text{C}$ ,  $V_{TLH} = 3.6\text{V}$ ,  $V_{THL} = 1.2\text{V}$   
 $T_A = 25^\circ\text{C}$ ,  $V_{TLH} = 3.6\text{V}$ ,  $V_{THL} = 1.0\text{V}$   
 $T_A = 125^\circ\text{C}$ ,  $V_{TLH} = 3.6\text{V}$ ,  $V_{THL} = 0.8\text{V}$

## Application Information

The ACPL-K30T automotive photovoltaic (PV) driver is a device that is paired with MOSFETs to form basic building block of several types of application. It consists of an Al-GaAs LED input that is optically coupled to a photovoltaic diode array. This becomes a voltage source with galvanic isolation. The advantage of photovoltaic driver is its simple design which does not require bias supply.

## Basic Construction

As shown in Figure 12, the input side of the PV Driver is LED driven. A current limiting resistor is required to limit the current through the LED. Recommended input forward current is 10 mA to 20 mA. The LED is optically coupled through a photodiode stack (D1 to D12) consisting of 12 photodiodes connected in series. When current is driven into the Light-Emitting Diode (LED) on the input side, the light from the LED generates photo current on the string of photodiodes to charge the gate of the MOSFETs, generating a photo-voltage proportional to the number of photodiodes, to switch and keep the power device on.

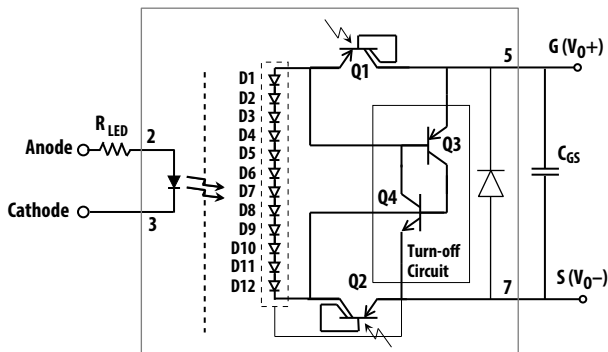


Figure 12. Basic Construction of Photovoltaic Driver

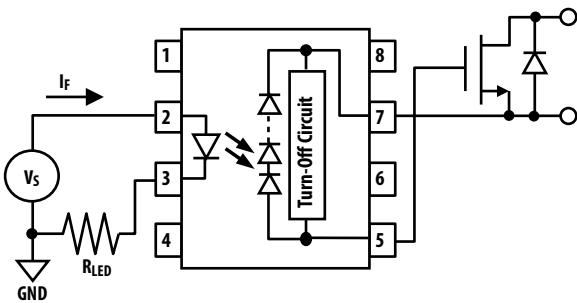


Figure 13. Photovoltaic Driver + Single External MOSFET

## PV Driver and MOSFET Configurations

The photovoltaic driver is a device that is combined with high voltage MOSFETs to form a solid-state relay. The photovoltaic driver can be configured with a single MOSFET or two MOSFETs (back to back) for bidirectional application. Pin 5 is connected to the Gate and Pin 7 is connected to the Source. Figure 13 and 14 are sample application circuits for the two configurations.

## Turn-Off Circuit

The photovoltaic driver has a built in turn-off circuit, which decreases the turn-off time. This circuit instantaneously discharges the gate capacitance of MOSFETs once the photovoltaic driver is turned off. The turn-off circuit is activated when the photovoltaic voltage is collapsing.

The sequence of operation of the turn-off circuit:

When LED is ON:

1. Q1 and Q2 are saturated.
2. SCR (Q3 and Q4) is disabled.
3. Photodiode array is connected to Gate and Source.

When LED is OFF:

1. Q1 and Q2 cease to conduct.
2. Photodiode array is disconnected from Gate and Source.
3. SCR (Q3 and Q4) is triggered and Gate capacitance ( $C_{GS}$ ) is discharged rapidly.

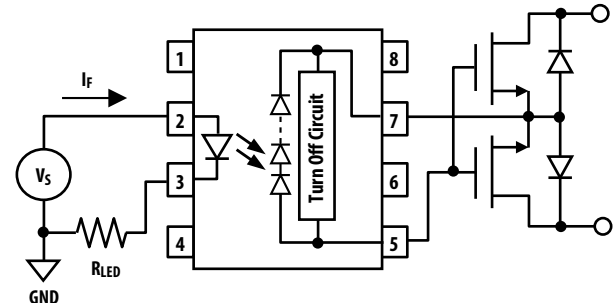


Figure 14. Photovoltaic Driver + Two Back-to-Back MOSFETs



## V<sub>OC</sub> and MOSFET V<sub>GS(TH)</sub>

ACPL-K30T has typical V<sub>OC</sub> of 7 V and minimum V<sub>OC</sub> of 4 V at 125 °C. This is sufficient to drive most logic gate level MOSFETs, with threshold voltages V<sub>GS(TH)</sub> of 4 V or less. The V<sub>OC</sub> has a typical temperature coefficient of -21 mV/°C. To serve as a guide in the design at different temperatures, Figure 15 shows the ACPL-K30T's minimum V<sub>OC</sub> vs. the MOSFET's maximum V<sub>GS(TH)</sub>.

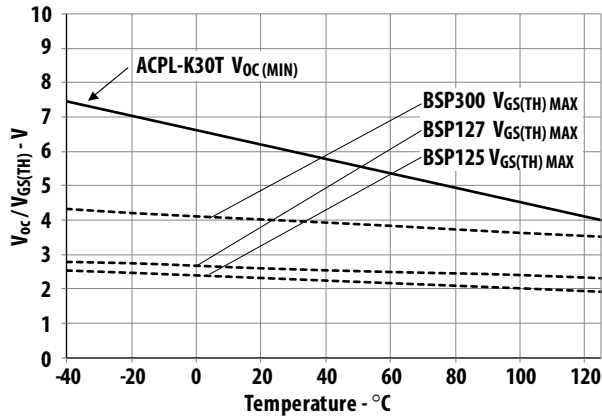


Figure 15. V<sub>OC</sub> minimum vs. MOSFET V<sub>GS(TH)</sub> maximum

## Two PV Drivers in Series

For high voltage MOSFETs that require higher V<sub>GS(TH)</sub>, two ACPL-K30T devices can be connected in series. Figure 16 shows the connection for this configuration. Two PV drivers in series will give 2× higher V<sub>OC</sub> (Typical = 14 V) compared with a single PV driver.

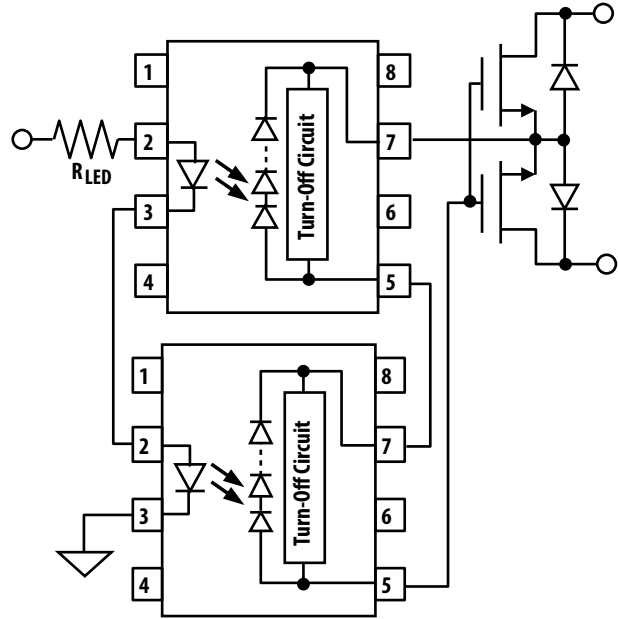


Figure 16. Two PV Drivers in Series

## Thermal Resistance Model for ACPL-K30T

The diagram of ACPL-K30T for measurement is shown in Figure 17. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

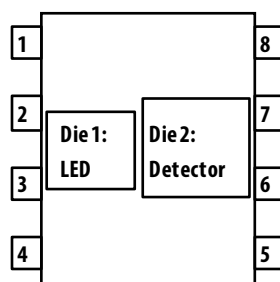


Figure 17. Diagram of ACPL-K30T for measurement

$$\begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} = \begin{bmatrix} \Delta T_1 \\ \Delta T_2 \end{bmatrix}$$

$R_{11}$ : Thermal Resistance of Die1 due to heating of Die1

$R_{12}$ : Thermal Resistance of Die1 due to heating of Die2.

$R_{21}$ : Thermal Resistance of Die2 due to heating of Die1.

$R_{22}$ : Thermal Resistance of Die2 due to heating of Die2.

$P_1$ : Power dissipation of Die1 (W).

$P_2$ : Power dissipation of Die2 (W).

$T_1$ : Junction temperature of Die1 due to heat from all dice (°C).

$T_2$ : Junction temperature of Die2 due to heat from all dice.

$T_A$ : Ambient temperature.

$\Delta T_1$ : Temperature difference between Die1 junction and ambient (°C).

$\Delta T_2$ : Temperature difference between Die2 junction and ambient (°C).

$$T_1 = R_{11} \times P_1 + R_{12} \times P_2 + T_A$$

$$T_2 = R_{21} \times P_1 + R_{22} \times P_2 + T_A$$

Measurement data on a low K (connectivity) board:

$$R_{11} = 258 \text{ } ^\circ\text{C/W}$$

$$R_{12} = 121 \text{ } ^\circ\text{C/W}$$

$$R_{21} = 119 \text{ } ^\circ\text{C/W}$$

$$R_{22} = 201 \text{ } ^\circ\text{C/W}$$

Measurement data on a high K (connectivity) board:

$$R_{11} = 194 \text{ } ^\circ\text{C/W}$$

$$R_{12} = 59 \text{ } ^\circ\text{C/W}$$

$$R_{21} = 53 \text{ } ^\circ\text{C/W}$$

$$R_{22} = 136 \text{ } ^\circ\text{C/W}$$

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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TECHNOLOGIES