HMC998APM5E

v04.0121

GaAs pHEMT MMIC
2 WATT POWER AMPLIFIER, DC - 22 GHz

Typical Applications

The HMC998APM5E is ideal for:

- Test Instrumentation
- Military & Space
- Fiber optics

Features

P1dB Output Power: +32 dBm

Psat Output Power: +34 dBm

High Gain: 15 dB

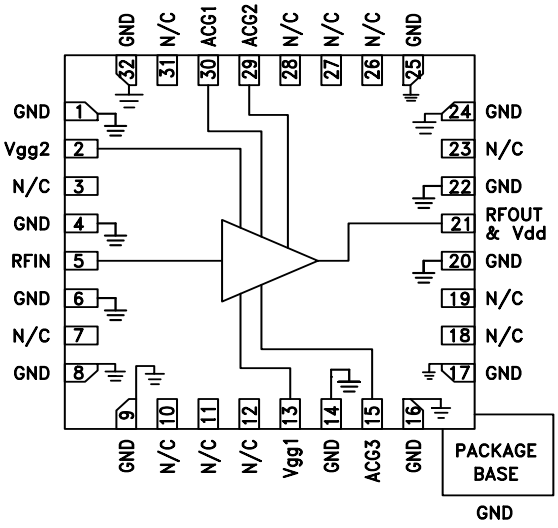
Output IP3: 42 dBm

Supply Voltage: Vdd = +15V @ 500 mA

50 Ohm Matched Input/Output

32 Lead 5x5 mm LFCSP Package: 25 mm²

Functional Diagram



General Description

The HMC998APM5E is a GaAs pHEMT MMIC Distributed Power Amplifier which operates from DC to 22 GHz. The amplifier provides +15 dB of gain, +42 dBm output IP3, and +32 dBm of output power at 1dB gain compression while requiring only 500mA from a +15V supply. The HMC998APM5E exhibits a slightly positive gain slope from 3 to 17 GHz making it ideal for military and space and test equipment applications. The HMC998APM5E amplifier I/Os are internally matched to 50 Ohms and is housed in a RoHS compliant, 5x5 mm leadless QFN surface mount package.

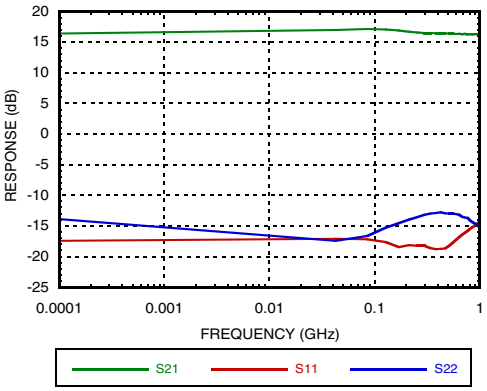
Electrical Specifications, T_A = +25° C, Vdd = +15V, Vgg2 = +9.5V [1], Idq = 500 mA [2]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ..	Max.	Units
Frequency Range		DC - 2			2 - 18			18 - 22		GHz
Gain	13	15		13	15		13	15		dB
Gain Flatness		±0.50			±0.45			±0.30		dB
Gain Variation Over Temperature		0.005			0.005			0.004		dB/ °C
Input Return Loss		15			22			22		dB
Output Return Loss		14			17			16		dB
Output Power for 1 dB Compression (P1dB)	27	30		29	32		28	31		dBm
Saturated Output Power (Psat)		34			34			32		dBm
Output Third Order Intercept (IP3) Pout/tone = +18dBm		42			42			40		dBm
Noise Figure		8			3			4		dB
Supply Current (Idd)		500			500			500		mA
Supply Voltage (Vdd)	11	15	15	11	15	15	11	15	15	V

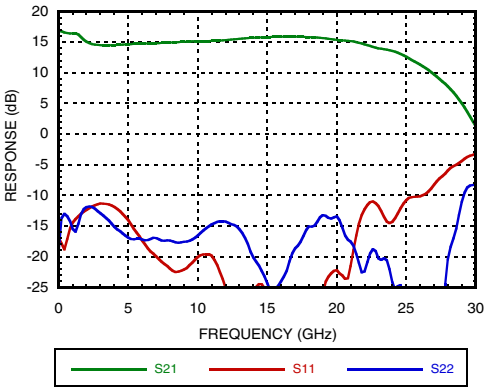
[1] Refer to application circuit section NOTE 5 for the Vgg2 bias for different Vdd levels.
[2] Adjust Vgg1 to achieve Idq = 500 mA typical; Vgg1 = -0.58V typical.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

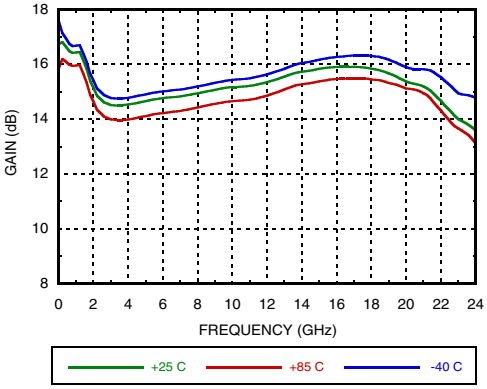
Low Frequency Gain & Return Loss



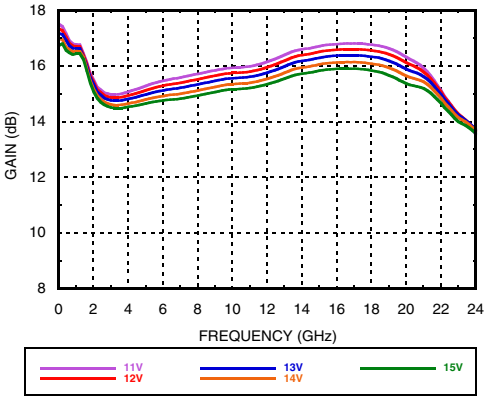
Gain & Return Loss



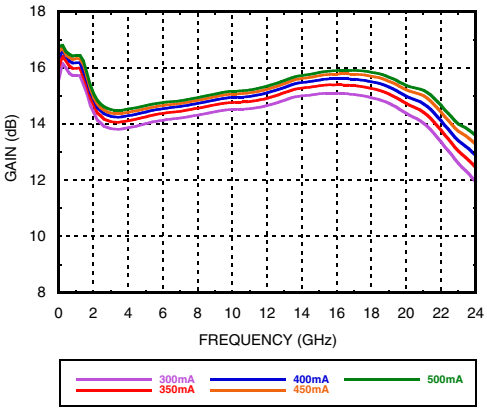
Gain vs. Temperature



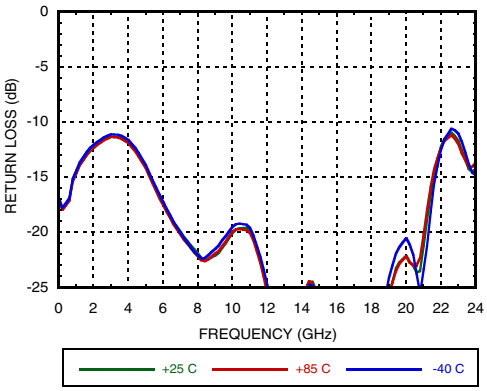
Gain vs. Vdd



Gain vs. Idq



Input Return Loss vs. Temperature



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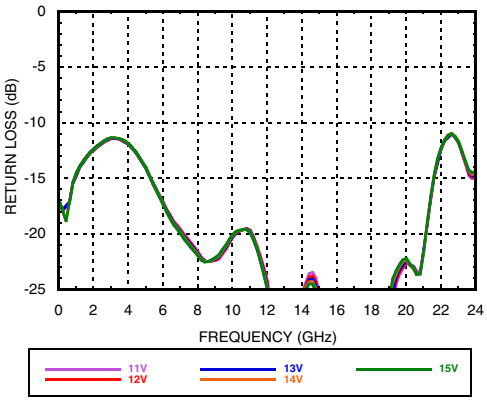
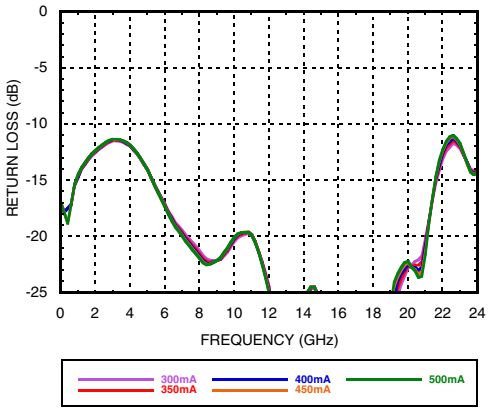
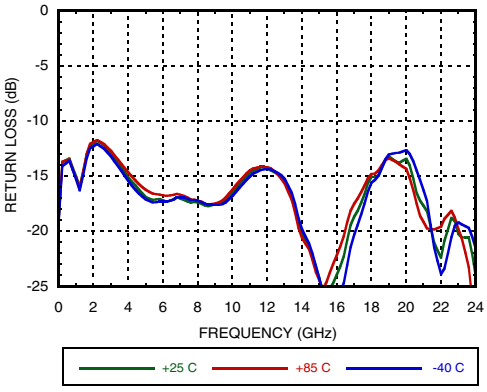
Input Return Loss vs. Vdd



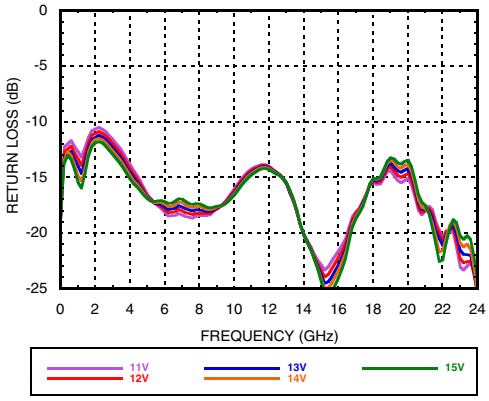
Input Return Loss vs. Idq



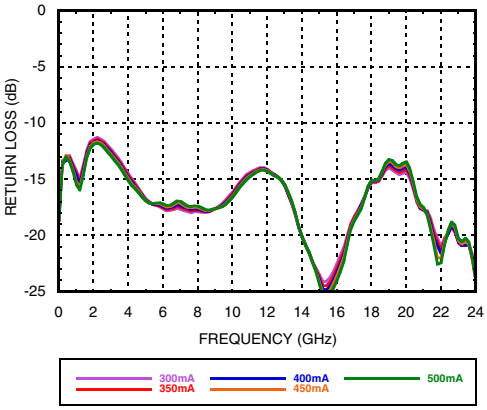
Output Return Loss vs. Temperature



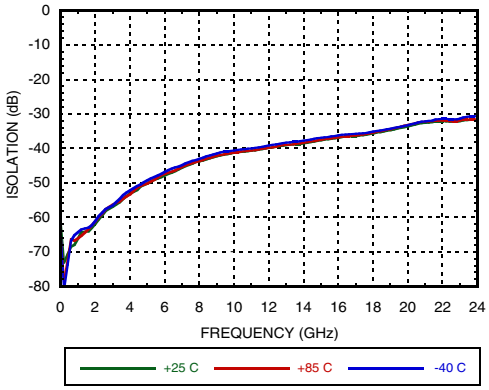
Output Return Loss vs. Vdd



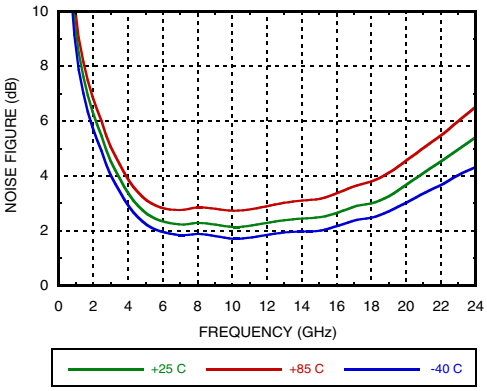
Output Return Loss vs. Idq



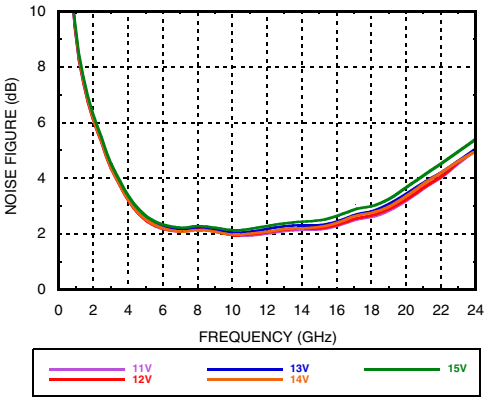
Reverse Isolation vs. Temperature



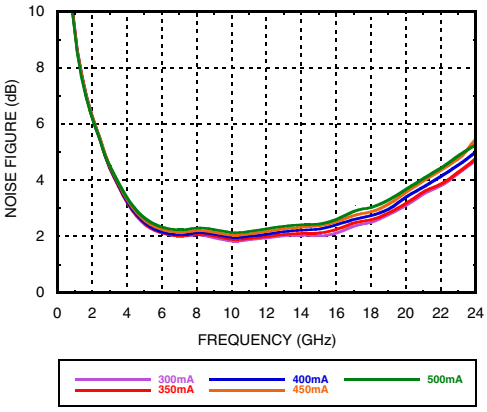
Noise Figure vs. Temperature



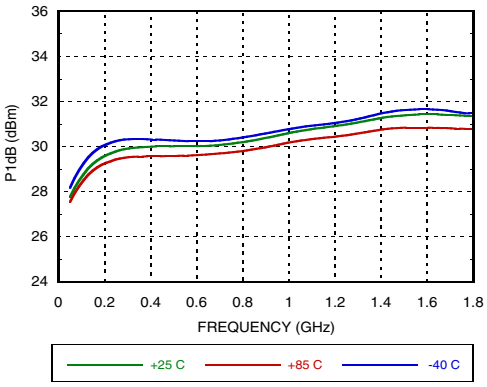
Noise Figure vs. Vdd



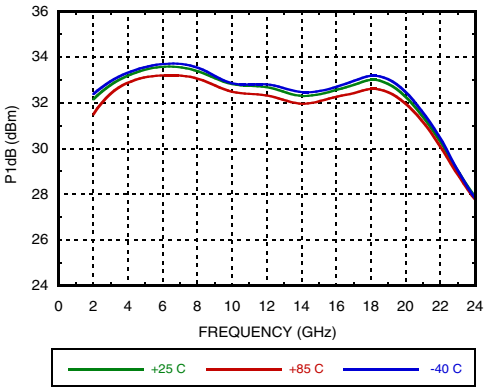
Noise Figure vs. Idq



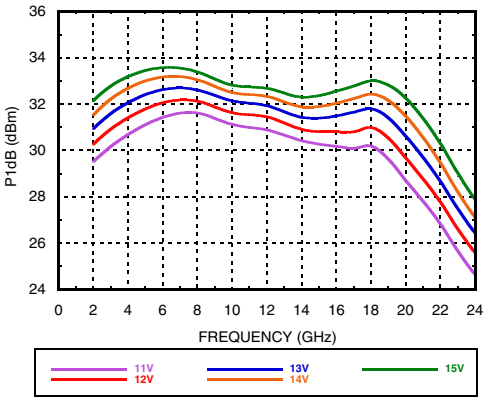
Low Frequency P1dB vs. Temperature



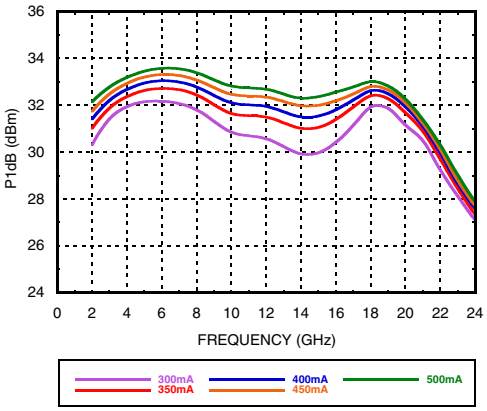
P1dB vs. Temperature



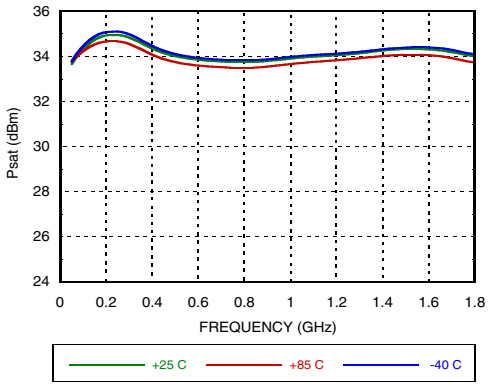
P1dB vs. Vdd



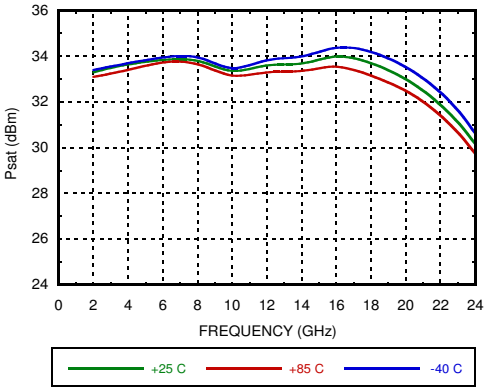
P1dB vs. Idq



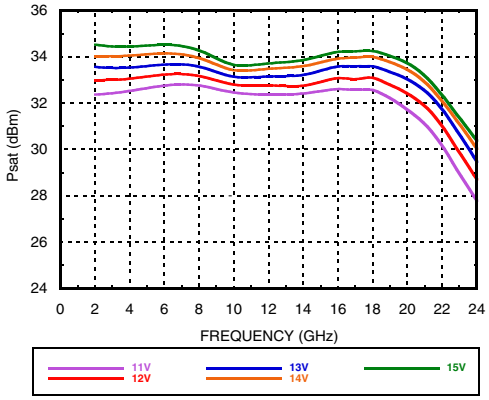
Low Frequency Psat vs. Temperature



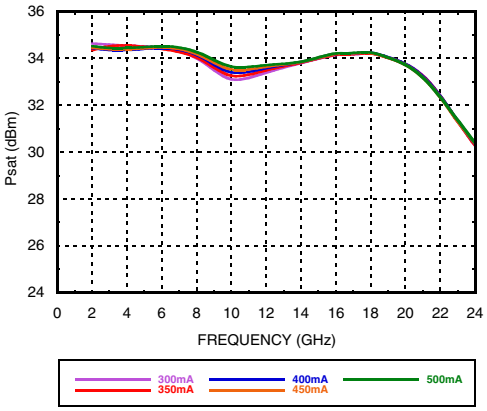
Psat vs. Temperature



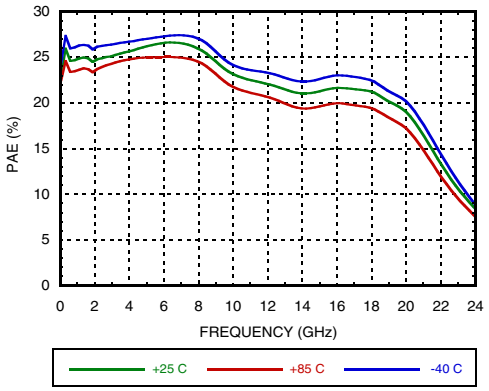
Psat vs. Vdd



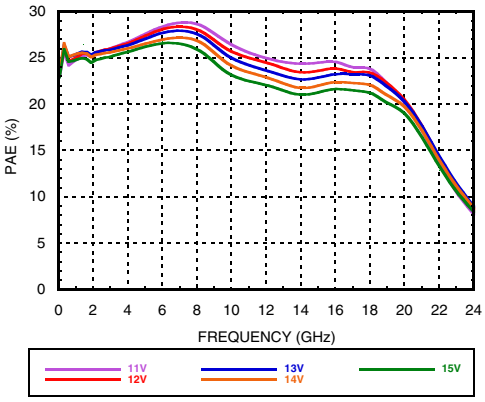
Psat vs. Idq



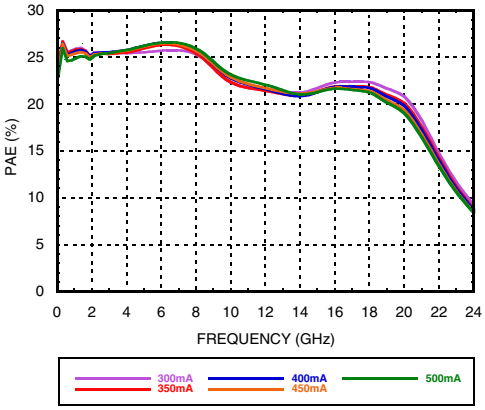
PAE @ Psat vs. Temperature



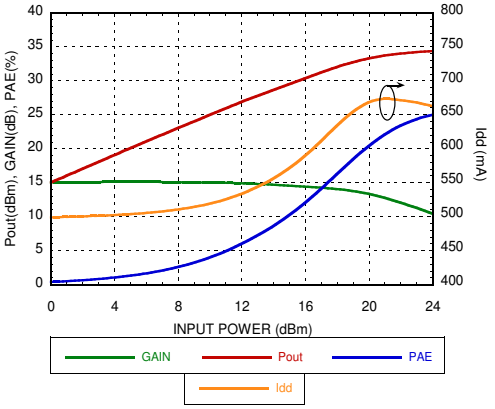
PAE @ Psat vs. Vdd



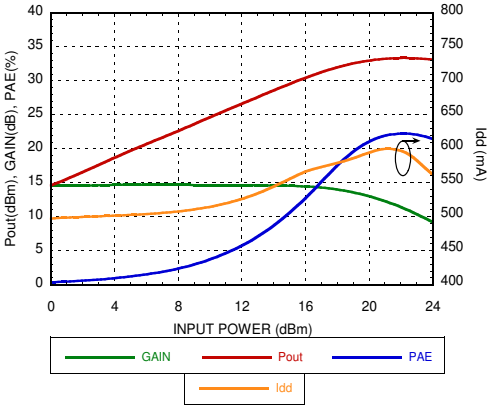
PAE @ Psat vs. Idq



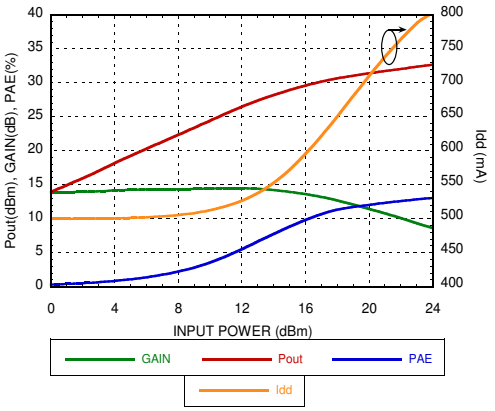
Power Compression @ 2 GHz



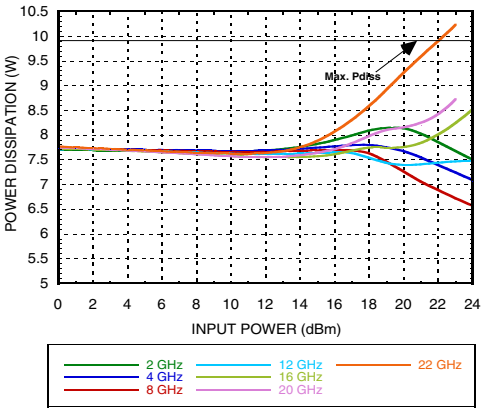
Power Compression @ 10 GHz



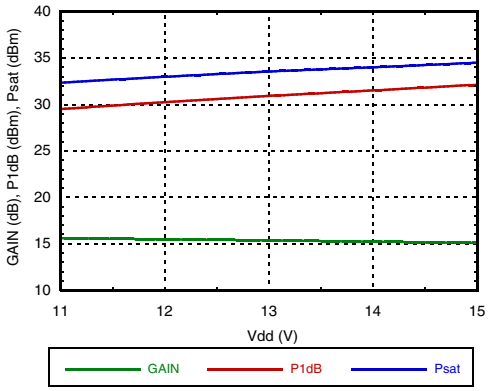
Power Compression @ 22 GHz



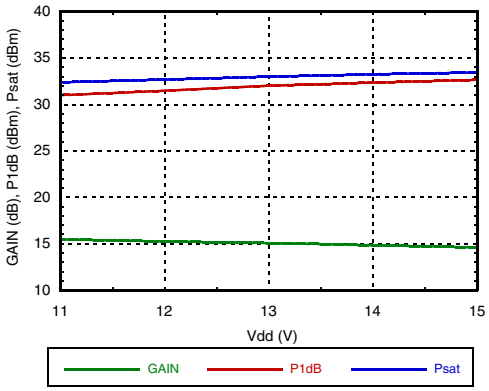
Power Dissipation @ 85C



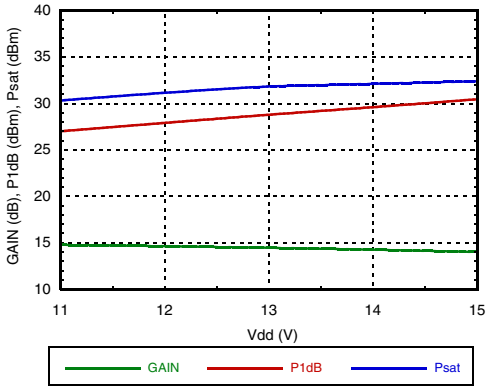
Gain & Power vs. Vdd @ 2 GHz



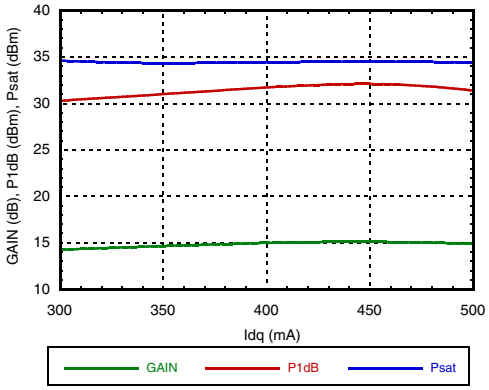
Gain & Power vs. Vdd @ 10 GHz



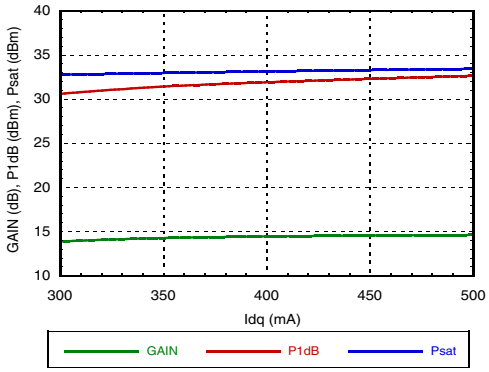
Gain & Power vs. Vdd @ 22 GHz



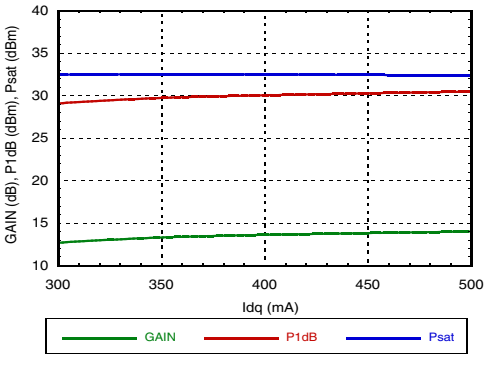
Gain & Power vs. Idq @ 2 GHz



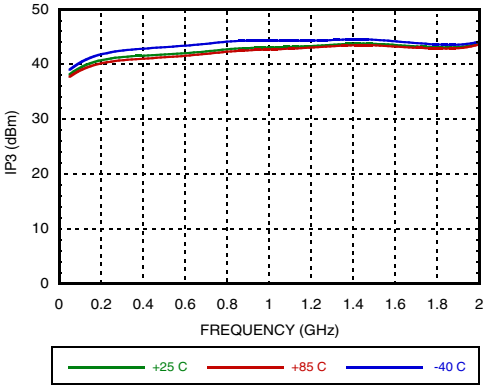
Gain & Power vs. Idq @ 10 GHz



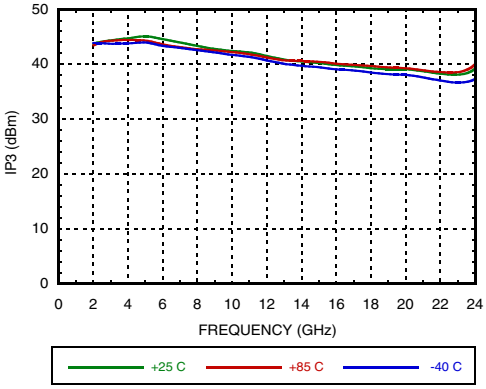
Gain & Power vs. Idq @ 22 GHz



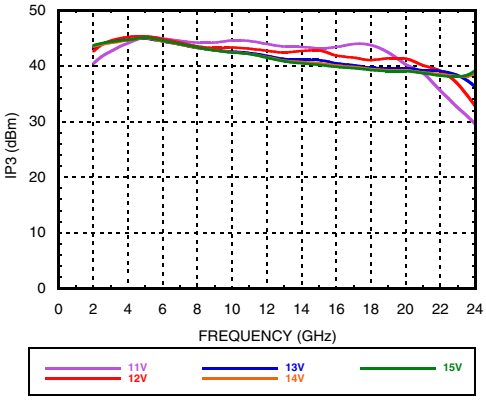
Low Frequency OIP3 vs. Temperature @ Pout/Tone = +18dBm



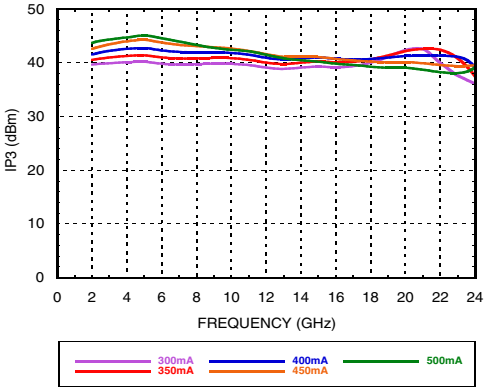
OIP3 vs. Temperature @ Pout/Tone = +18dBm



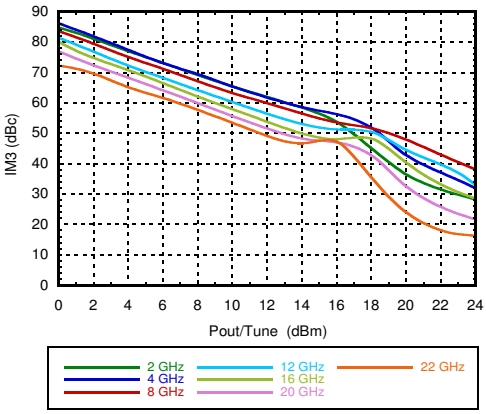
OIP3 vs. Vdd @ Pout/Tone = +18dBm



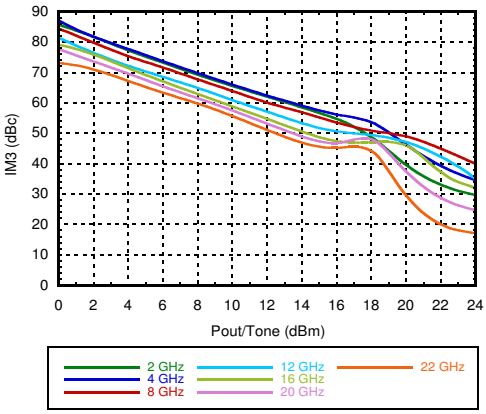
OIP3 vs. Idq @ Pout/Tone = +18dBm



Output IM3 @ Vdd = +11V



Output IM3 @ Vdd = +12V



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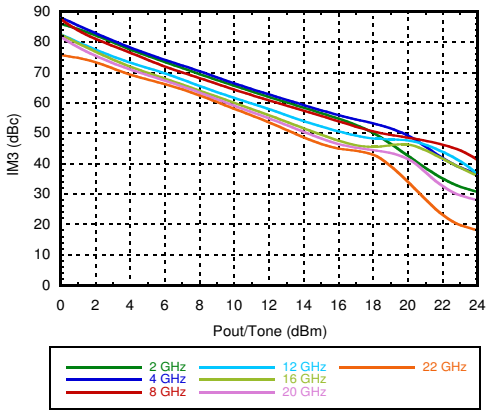
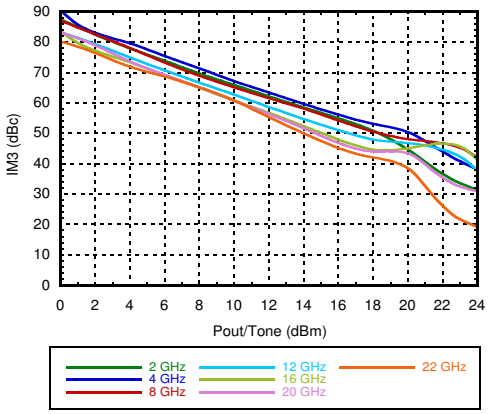
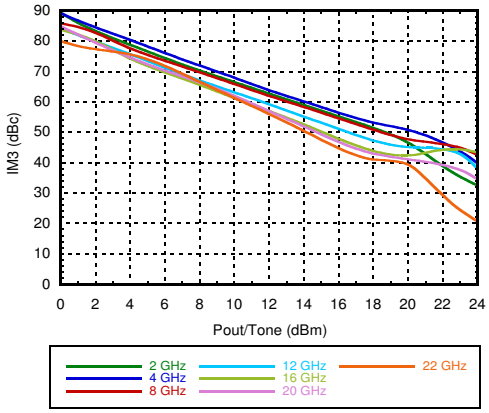
Output IM3 @ Vdd = +13V



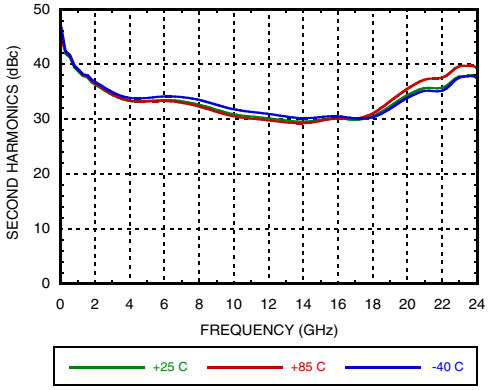
Output IM3 @ Vdd = +14V



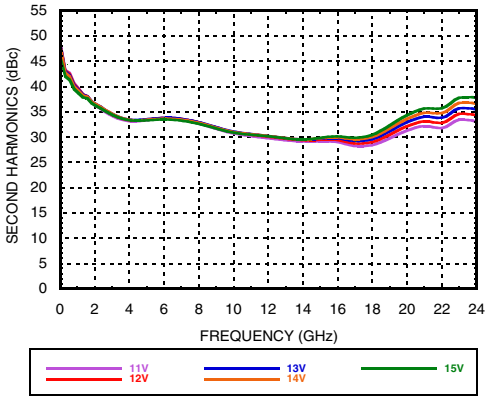
Output IM3 @ Vdd = +15V



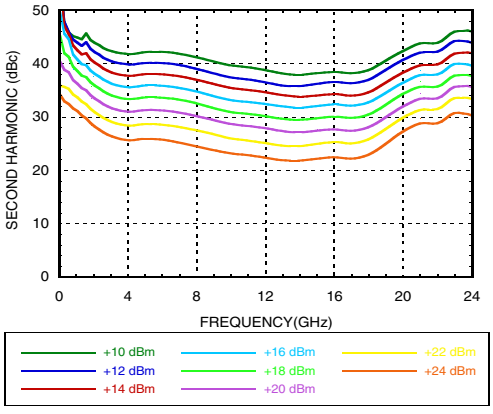
Second Harmonics vs. Temperature @ Pout = +18dBm



Second Harmonics vs. Vdd @ Pout = +18dBm



Second Harmonics vs. Pout



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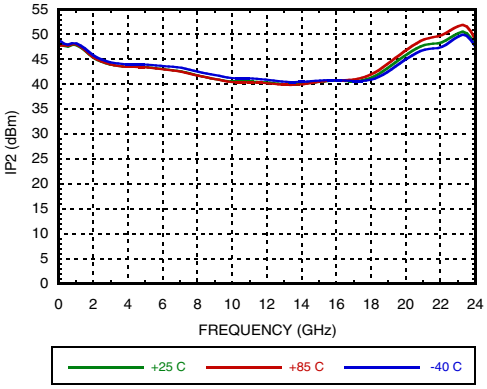
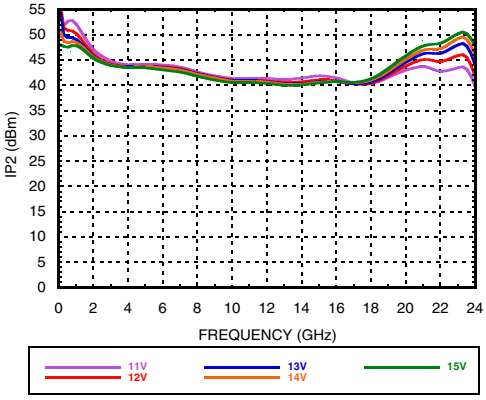
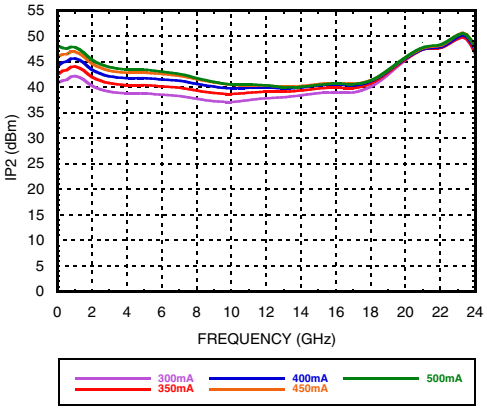
OIP2 vs. Temperature @ Pout/Tone = +18dBm



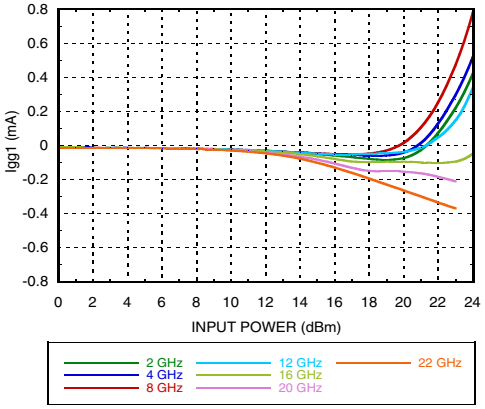
OIP2 vs. Vdd @ Pout/Tone = +18dBm



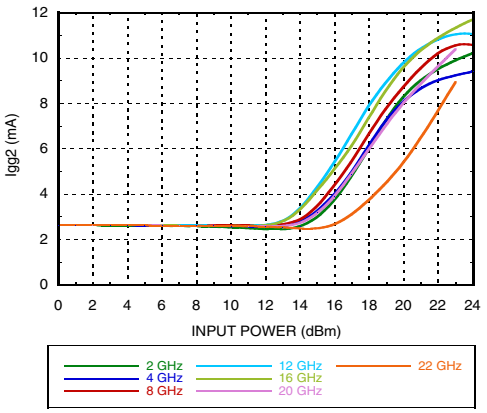
OIP2 vs. Idq @ Pout/Tone = +18dBm



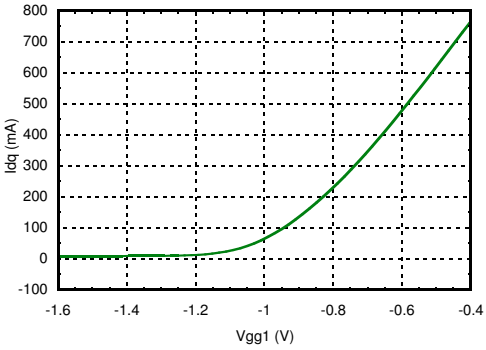
Igg1 vs. Input Power



Igg2 vs. Input Power



Idq vs. Vgg1 Representative of a Typical Device



GaAs pHEMT MMIC
2 WATT POWER AMPLIFIER, DC - 22 GHz

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+16 Vdc
Gate Bias Voltage (Vgg1)	-3 to 0 Vdc
Gate Bias Voltage (Vgg2)	(Vdd-6V) up to +11.5 Vdc
RF Input Power (RFIN)	+27 dBm
Continuous Pdiss (T= 85 °C) (derate 109.89 mW/°C above 85 °C)	9.9 W
Output Load VSWR	7:1
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class 1A
Max Peak Reflow Temperature	260 °C

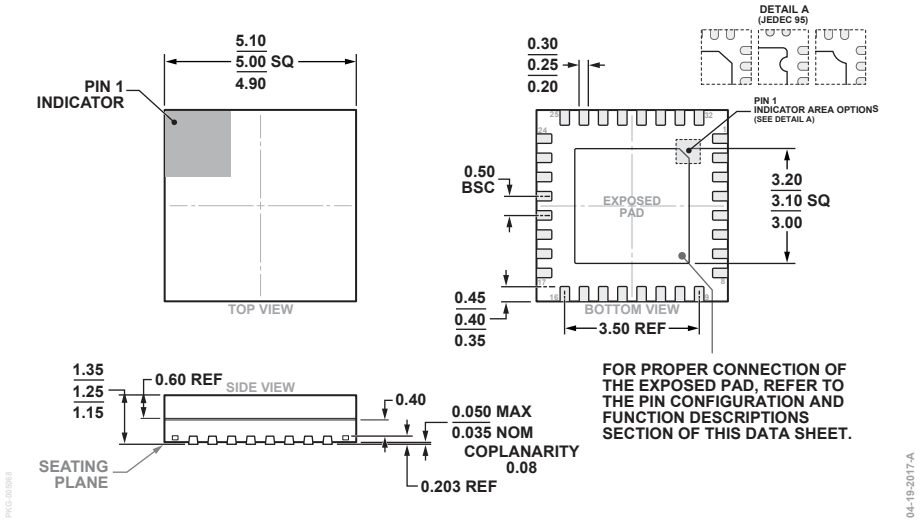
Reliability Information

Channel Temperature to Maintain 1 Million Hour MTTF	175 °C
Nominal Channel Temperature (T=85 °C, Vdd = 15 V)	153.25°C
Thermal Resistance (channel to ground paddle)	9.1 °C/W

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Outline Drawing



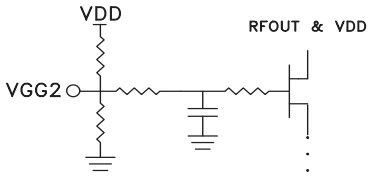
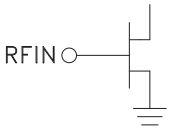
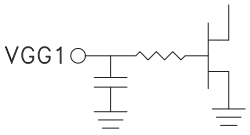
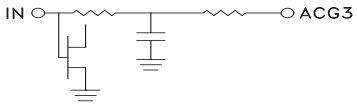
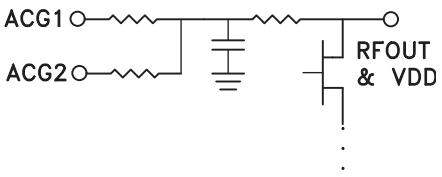
32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5mm × 5mm and 1.25mm Package Height
(CG-32-2)
Dimensions shown in millimeters.

Package Information

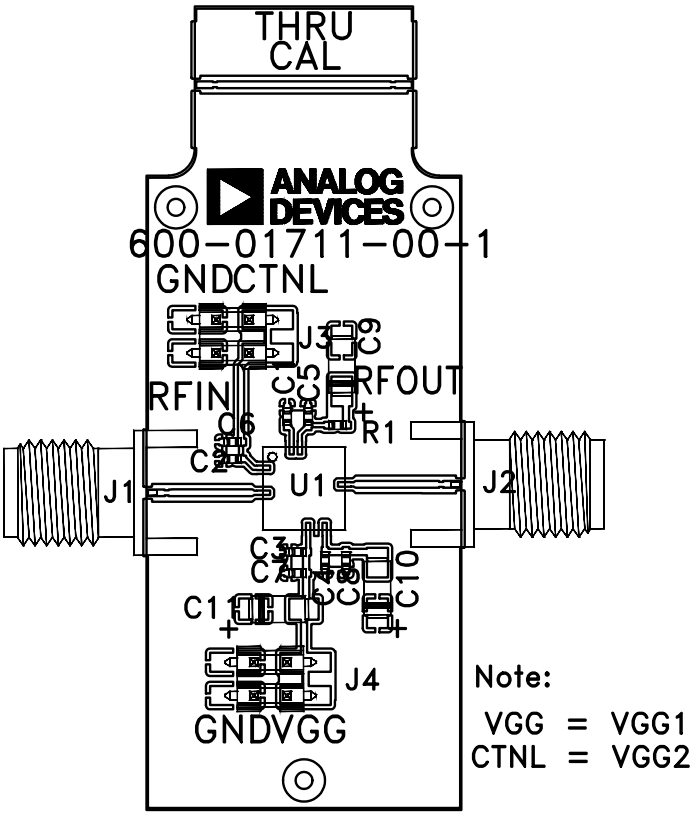
Part Number	Package Body Material	Lead Finish	MSL Rating [1]	Package Marking
HMC998APM5E	RoHS-compliant Low Stress Pre-Molded Plastic	NiPdAu	MSL3	HMC998A

[1] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 6, 8, 9, 14, 16, 17, 20, 22, 24,25, 32 Package Bottom	GND	These pins & exposed ground paddle must be connected to RF/DC ground.	
2	VGG2	Gate control 2 for amplifier. External bypass capacitor required per application circuit herein. For nominal bias of 15V, +9.5V should be applied to Vgg2. Refer to application circuit section NOTE 5 for the Vgg2 bias for different Vdd levels.	
3, 7, 10, 11, 12, 18, 19, 23, 26, 27, 28, 31	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
5	RFIN	This pin is DC coupled and matched to 50 Ohms. Blocking capacitor is required.	
13	VGG1	Gate control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow “MMIC Amplifier Biasing Procedure” application note.	
15	ACG3	Low Frequency termination. Attach bypass capacitor per application circuit herein.	
21	RFOUT & Vdd	RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein	
30	ACG1		

Evaluation PCB



Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC998APM5E Evaluation PCB	EV1HMC998APM5[1]

[1] Reference this number when ordering Evaluation PCB Only

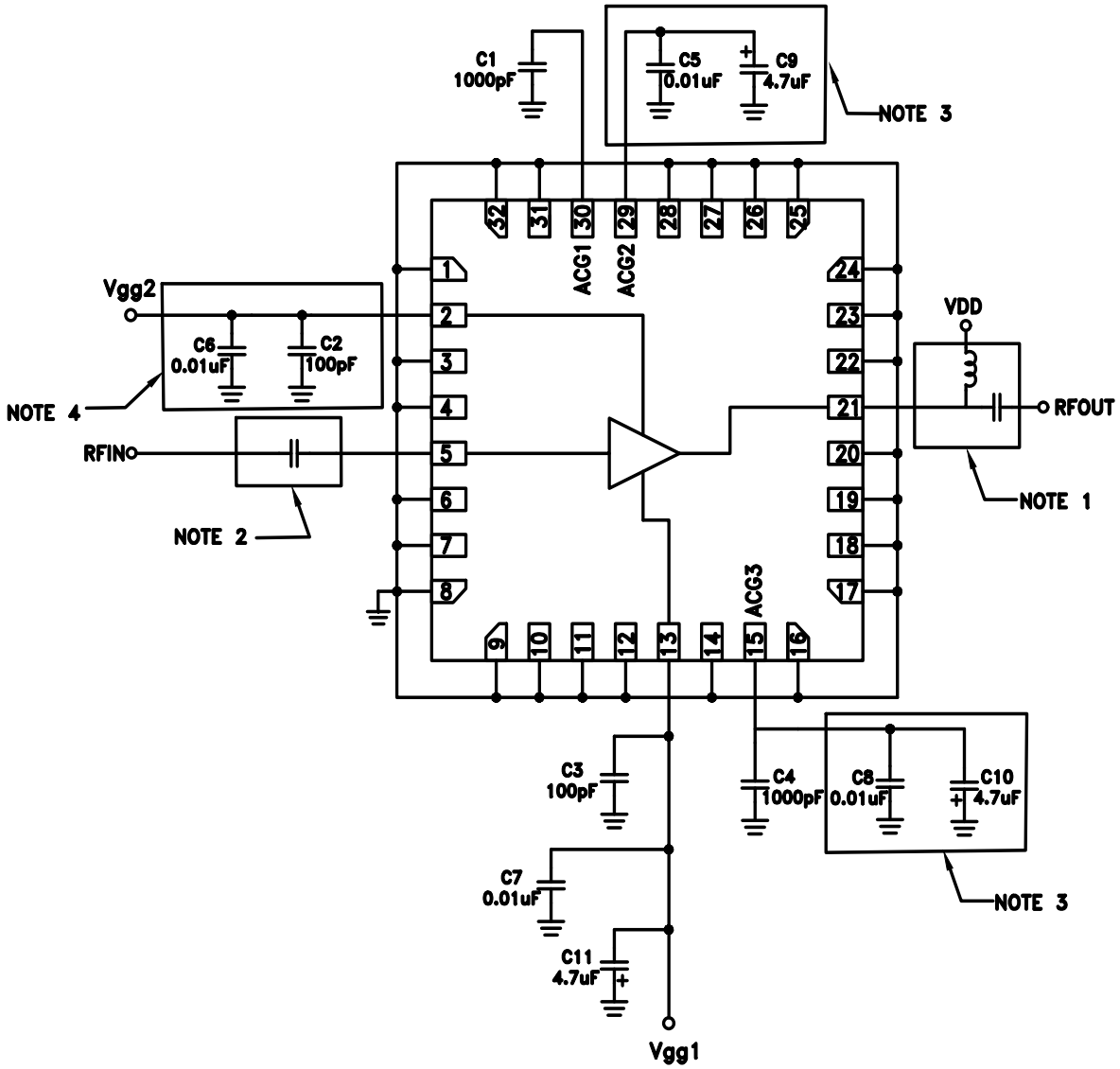
List of Materials for Evaluation Board EV1HMC998APM5

Item	Description
J1, J2	PCB Mount K Connector
J3, J4	DC Pins Connector
C1, C2, C3, C4	100pF Capacitor, 0402 Pkg.
C5 - C8	0.01uF Capacitor, 0402 Pkg.
C9 - C11	4.7 uF Capacitor, Tantalum.
R1	0 Ohm Resistor, 0402 Pkg.
U1	HMC998APM5E
PCB [1]	600-01711-00 Evaluation PCB.

[1] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of vias should be used to connect the top and bottom ground planes, including the grounds directly beneath the ground paddle, to provide for adequate electrical and thermal conduction. Use of a heatsink on the bottom side of the PCB is recommended.

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.
NOTE 2. External DC block required at RF input.
NOTE 3: Optional capacitors to be used if part is to be operated below 200MHz.
NOTE 4: External capacitors required to maintain nominal gain at low frequency band.
NOTE 5: Refer to table below for the recommended Vgg2 bias for different Vdd supply voltage.

Vdd (V)	Vgg2 (V)
11	7
12	7.6
13	8.2
14	8.9
15	9.5