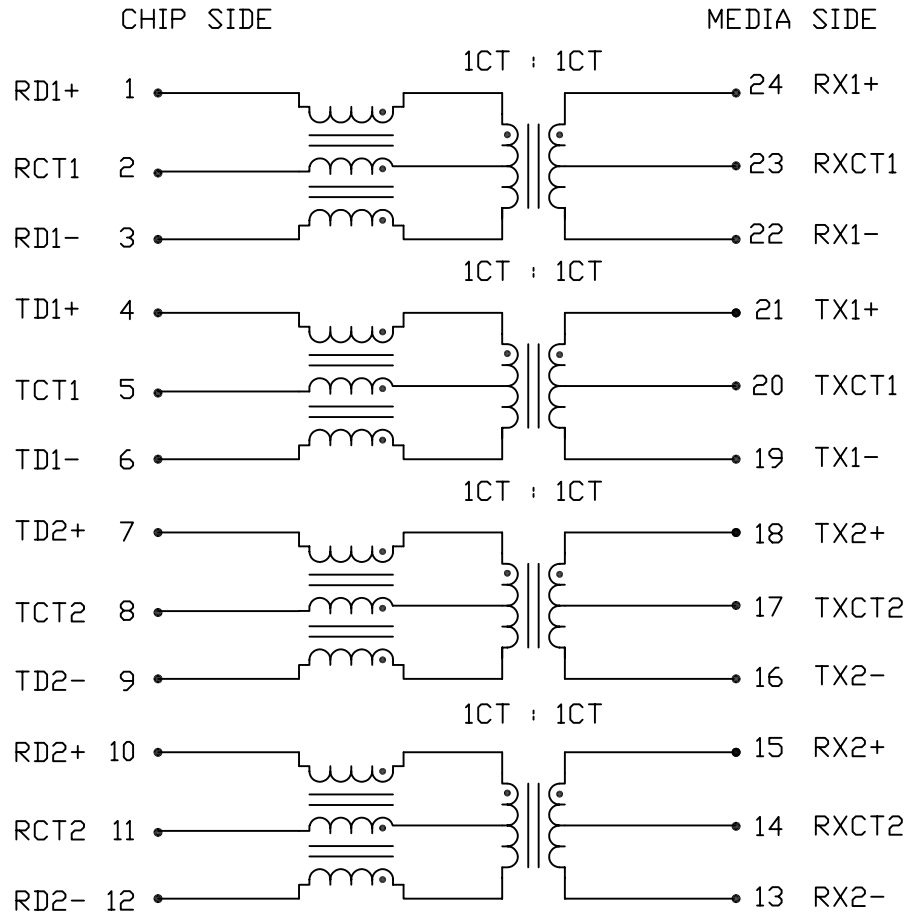


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SCHEMATIC

ELECTRICAL CHARACTERISTICS (@25°C)



<p>TURN'S RATIO CHIP SIDE : MEDIA SIDE</p> <p>POLARITY</p> <p>□CL MEDIA SIDE</p> <p>INSERTION LOSS 300kHz 1MHz TO 100MHz 125MHz</p> <p>RETURN LOSS 1MHz TO 30MHz 30MHz TO 80MHz 100MHz</p> <p>CROSSTALK 1MHz 10MHz TO 100MHz</p> <p>DM TO CM REJECTION 2MHz 30MHz TO 200MHz</p> <p>HIPOT</p>	<p>1CT : 1CT</p> <p>PER DOT CONVENTION</p> <p>350μH MIN @100kHz, 100mVrms WITH 8mA DC BIAS</p> <p>1.2dB MAX 1.0dB MAX 3.0dB MAX</p> <p>18dB MIN 12-20LOG(F/80MHz) dB MIN 10dB MIN</p> <p>55dB MIN 55-24LOG(F/10MHz) dB MIN</p> <p>60dB MIN 40-22LOG(F/30MHz) dB MIN</p> <p>PER HAND-WORK-03</p>
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NOTES:
DESIGN FOR 10/100/1000BT WITH PoE APPLICATION

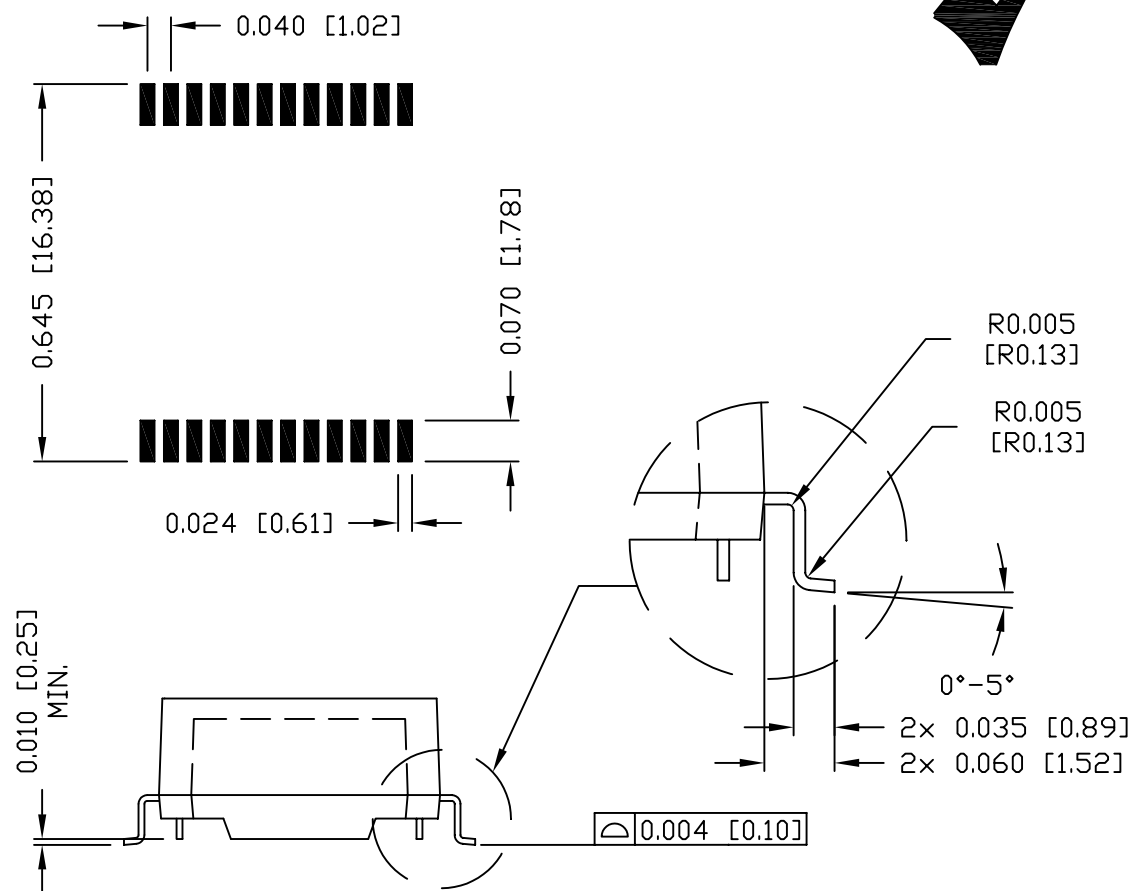
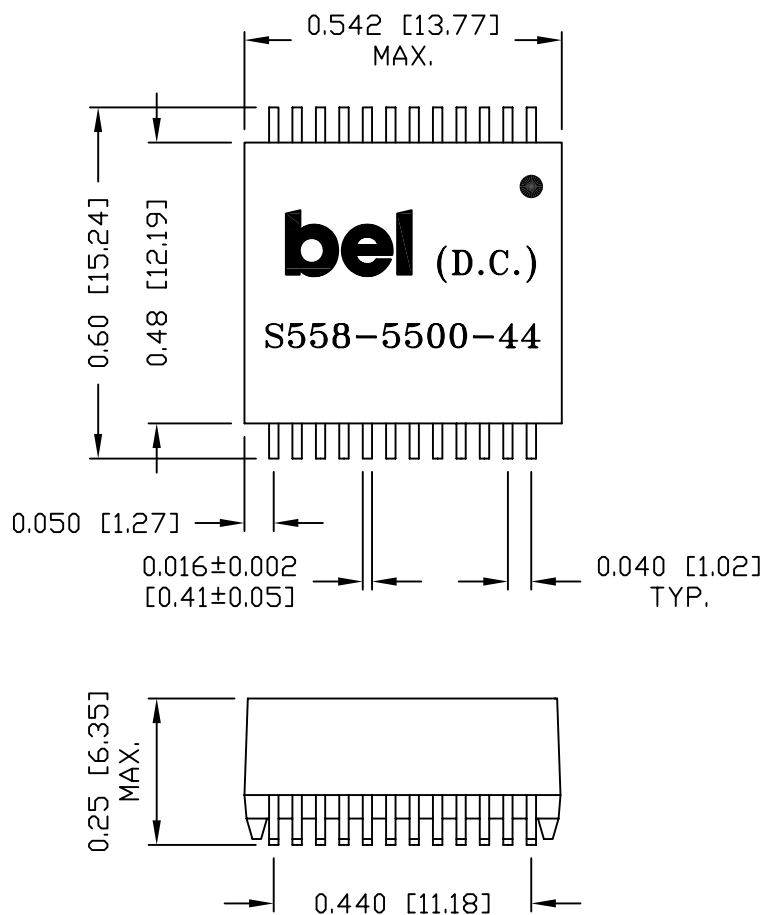
REV. : C PAGE : 2

ORIGINATED BY	DATE	TITLE ELECTRICAL SPECIFICATION S558-5500-44	PART NO. / DRAWING NO.	STANDARD DIM. [] METRIC DIM. AS REF.	 POWER PROTECT CONNECT	
Alice Pang	2015-01-26		X558-5500-44	TOL. IN INCH		UNIT : INCH [mm]
DRAWN BY	DATE		FILE NAME	.X		SCALE : N/A
ZC Guo	2015-01-26	X558550044C.DWG	.XX	SIZE : A4		
			.XXX			

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SUGGESTED PCB PAD LAYOUT



NOTES:

1. STANDARD MARKING REFER TO DOC. HAND-WORK-04.
2. PACKAGE CODE: "QSS001".

REV. : C PAGE : 2

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM. [] METRIC DIM. AS REF.	
Lawrence Tsang	2015-01-26	MECHANICAL OUTLINE S558-5500-44	X558-5500-44	TOL. IN INCH	UNIT : INCH [mm]
DRAWN BY	DATE		FILE NAME	.X	SCALE : N/A
ZC Guo	2015-01-26		X558550044C.DWG	.XX ±0.01	SIZE : A4
				.XXX ±0.005	

