TAS5706EVM2

This manual describes the operation of the TAS5706EVM2 to evaluate the performance of the TAS5706A. This main contents of this document are:

- Details on how to properly connect a TAS5706A Evaluation Module (TAS5706EVM2) and the details of the EVM.
- Details on how to install and use the GUI to program the TAS5706A.
- Details on how to use the audio processing features like EQ and DRC.
- Quick-Start Guide for the common modes in which TAS5706EVM2 can be used

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1 Overview

The TAS5706A evaluation module (TAS5706EVM2) demonstrates the TAS5706A device from Texas Instruments.

The TAS5706A combines a high-performance PWM processor with a class-D audio power amplifier. This EVM can be configured with two bridge-tied loads (BTL) (2.0) or two single-ended (SE) and one BTL sub (2.1) or four SE (4.0) modes. When operated with an external subwoofer power stage such as the TAS5601EVM4. TAS5706A supports two bridge-tied channels plus a bridge-tied subwoofer using an external TAS5601amplifier.For detailed information about the TAS5706A device, review the device data sheet, document number SLOS606. Pulse Width Modulator (PWM) is based on TI's Equibit™ technology. Review the board schematic and TAS5601EVM4 documents for additional information, and more specific application information on the subwoofer daughter card and connectors between the two boards.

The EVM software with its graphic user interface facilitates evaluation by providing access to the TAS5706A registers through a USB port. Refer to the *Using the EVM Software* section for further details.

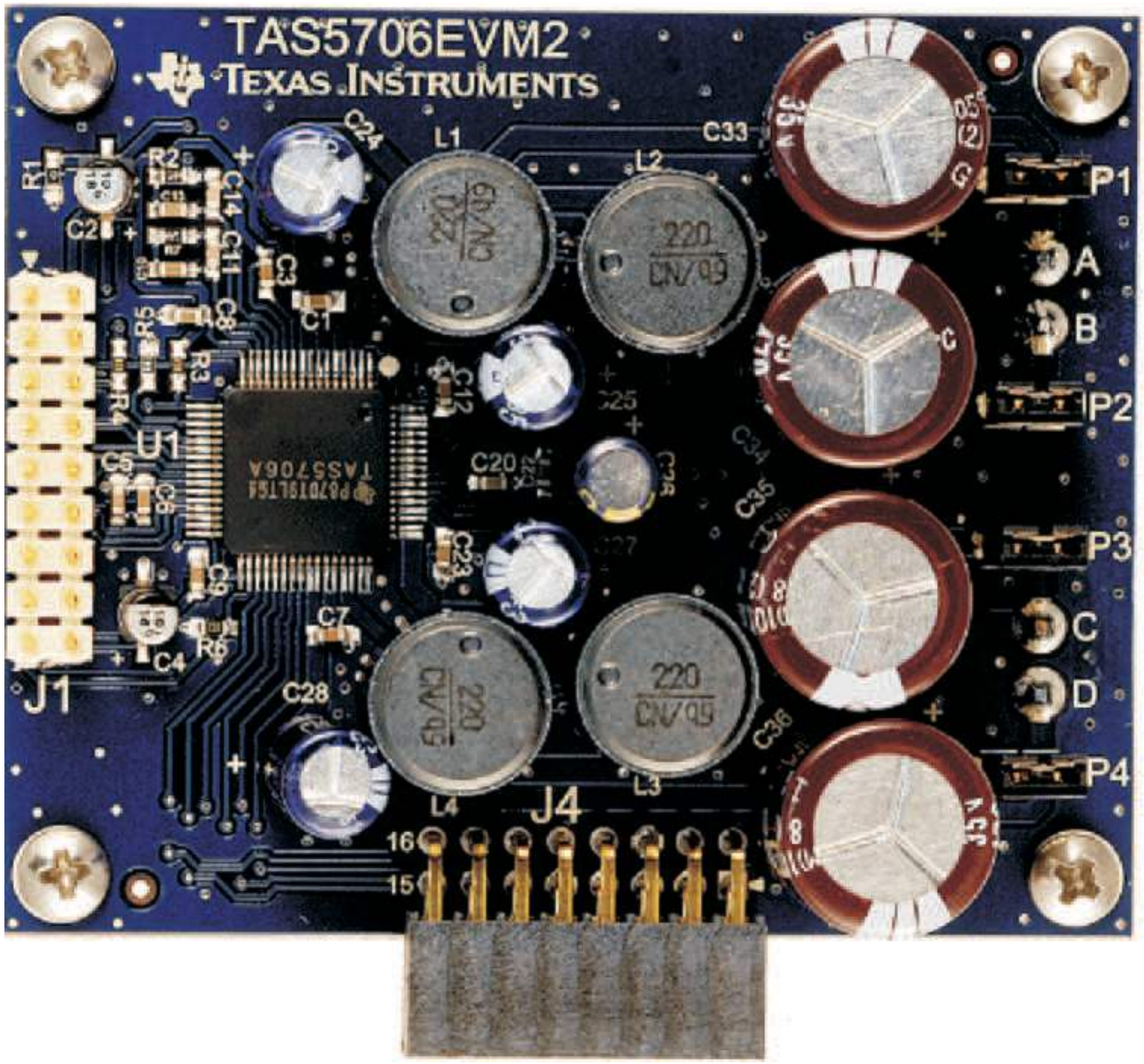


Figure 1. TAS5706EVM2 Printed-Circuit Board

The TAS5706EVM2, together with other TI components on this board, is a complete 2.1-channel digital audio amplifier system. The MC57XXPSIA Controller board includes a USB interface, a digital input (SPDIF), analog inputs via the ADC (PCM1808), power inputs and other features like a mute function and power down.

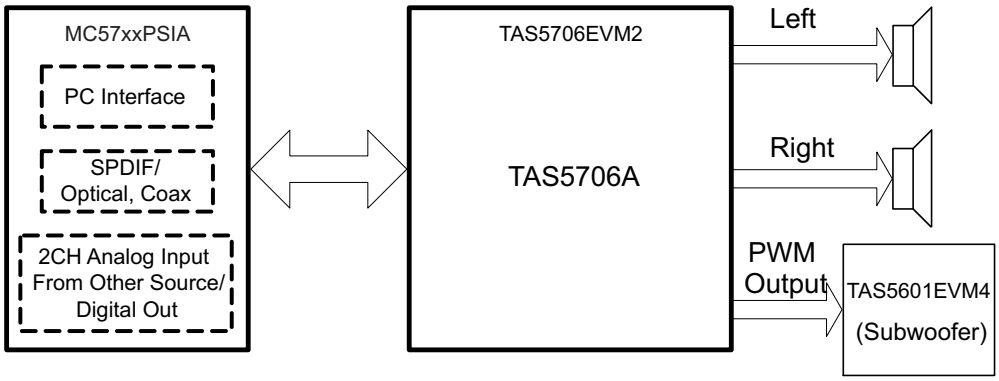


Figure 2. Complete System and EVM Signal Path Overview

1.1 TAS5706EVM2 and MC57xxPSIA Features

- Channel evaluation module design.
- Self-contained protection systems and control pins
- USB interface
- Standard I^2S data input using optical or coaxial inputs
- Analog input through analog to digital converter
- Subwoofer connection—the PWM terminal provides the PWM signal and power to an external subwoofer board
- Double-sided plated-through PCB, 1-oz copper
- Access to control signal gain and data format through EVM-software graphic user interface (GUI)

2 Installation

This section describes the EVM and software installation.

2.1 EVM Installation

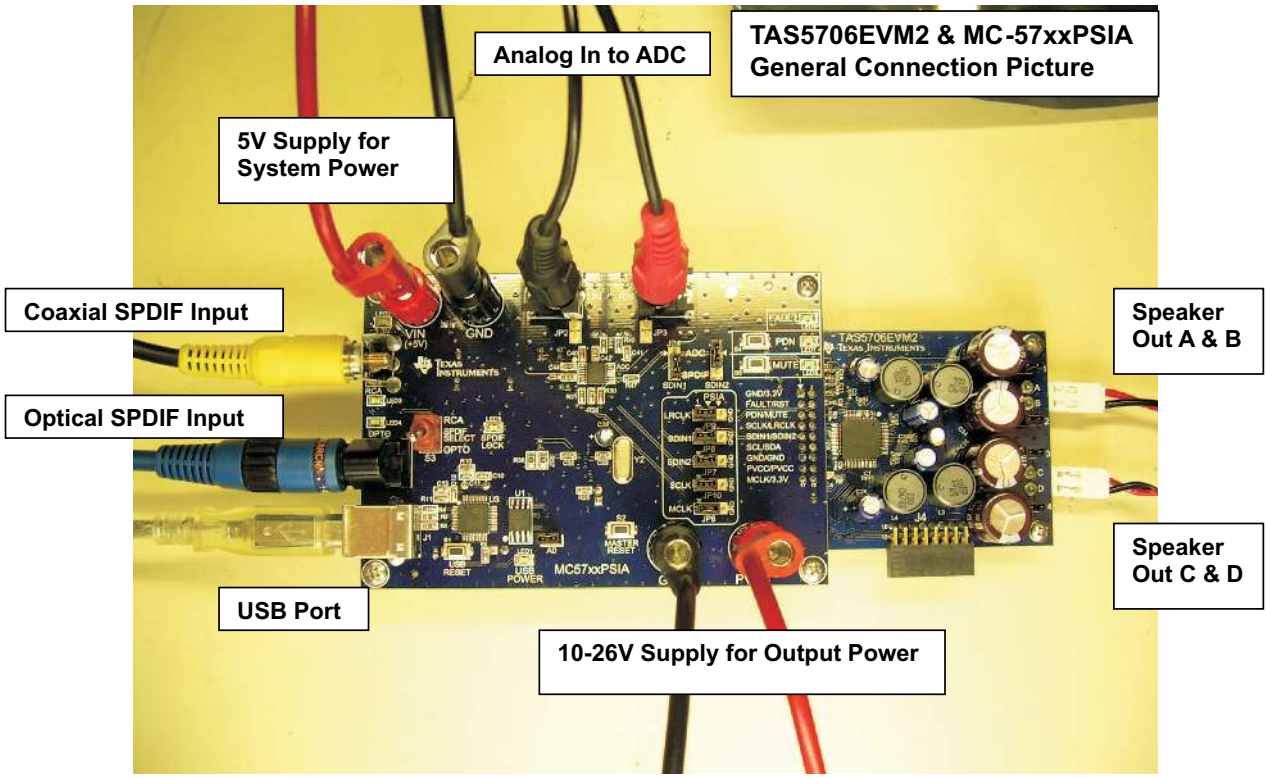


Figure 3. General Connection Picture

The following are the basic tools for the initial EVM power up.

- 5-V, 1-A power supply (VIN)
- 10–26-V, 4-A power supply (PVCC)
- Banana-style test leads for power supplies and speakers
- Optical or coaxial cable for SPDIF interface based on signal source
- USB cable
- EVM software
- Two 8-Ω speakers or loads

The following sections describe the TAS5706EVM2 board in regards to power supply (PSU) and system interfaces.

2.1.1 Connecting the TAS5706EVM2 to MC57xxPSIA

On the right side of the MC57xxPSIA is a terminal block and another on the left of the TAS5706EVM2 (labeled J1). Carefully place the MC57xxPSIA block above the TAS5706EVM2 block and gently push down.

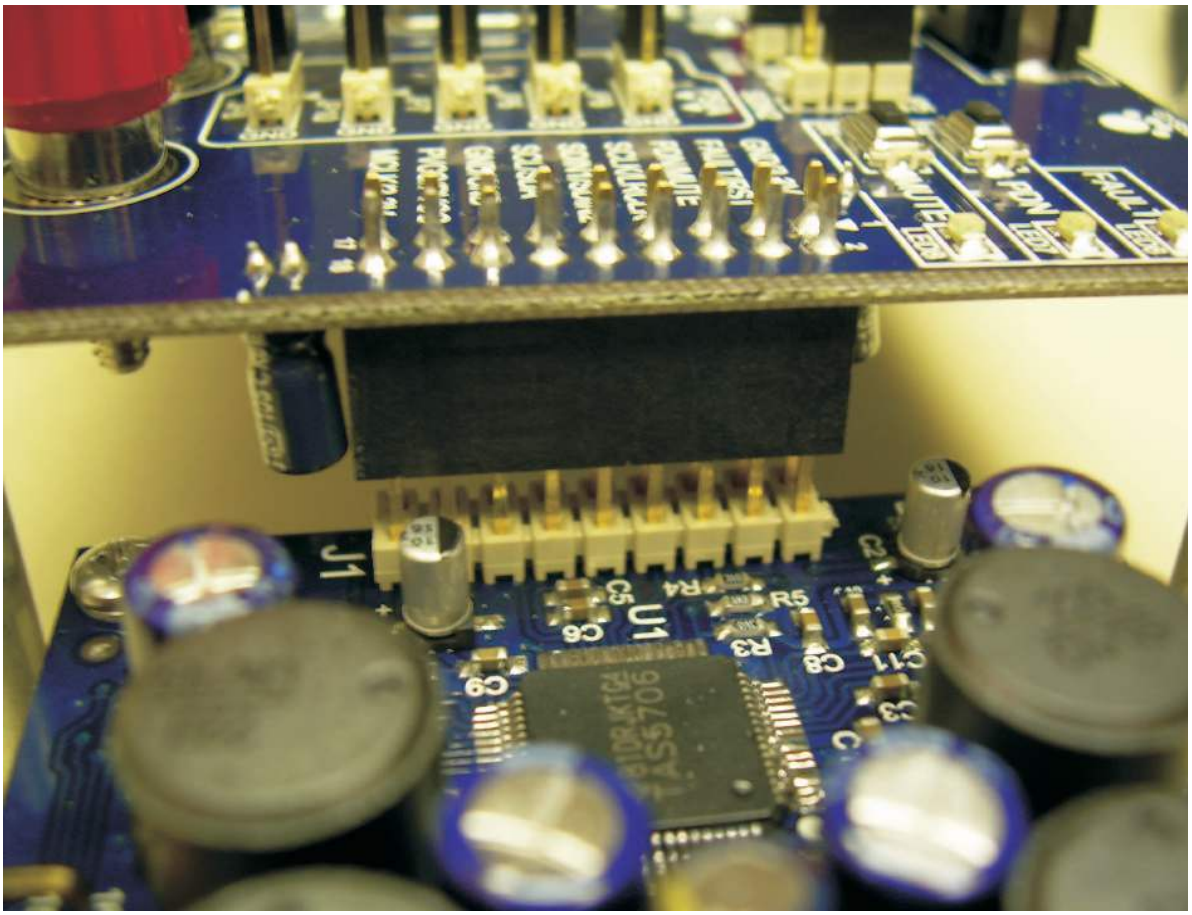


Figure 4. Connecting TAS5706EVM2 to MC57xxPSIA

2.1.2 PSU Interface

The TAS5706EVM2 is powered by two power supplies connected to the MC57xx controller board: a 5-V power supply (VIN) and a 10-V to 26-V (PVCC) power supply. The 3.3-V level is generated on the board by a voltage regulator from the 5-V supply.

Note: The power-supply cable length must be minimized. Increasing the length of the PSU cable increases the distortion of the amplifier at high output levels and low frequencies

The maximum output-stage supply voltage depends on the speaker load resistance. Check the recommended maximum supply voltage in the TAS5706A (SLOS606) data sheet.

Table 1. Recommended Power Supplies

Description	Voltage Limitations (8-Ω Load)	Current Recommendations
System power supply	5 V	1 A
Output power stage supply	10–26 V	4 A[(1)]

(1) The rated current corresponds to two channels, full scale.

2.1.3 Loudspeaker Connectors

CAUTION

All speaker outputs are biased at Vcc/2 and may not be connected to ground (e.g., through an oscilloscope ground).

Loudspeaker connections vary by device setup. Consult the quick-start guide (Section 7) for more details. However, the following is a general guideline:

When connecting a speaker in BTL mode, connect the speaker's two terminals ("+" and "-") across two outputs on the TAS5706EVM2. Ensure that the jumper (JP1 - JP4) on each output is in place.

When connecting a speaker in Single-Ended (SE) mode, connect the speaker's "+" terminal to one EVM output, and the speaker's "–" terminal must be grounded at the output power ground (next to PVCC on the MC-57xxPSIA). Ensure that the jumper (JP1 - JP4) on each output is removed.

Speakers or loads can be connected to the outputs A-D with clip leads, or cables can be made with female connectors (JST VHR-2N) that can mate to male connectors on the EVM board.

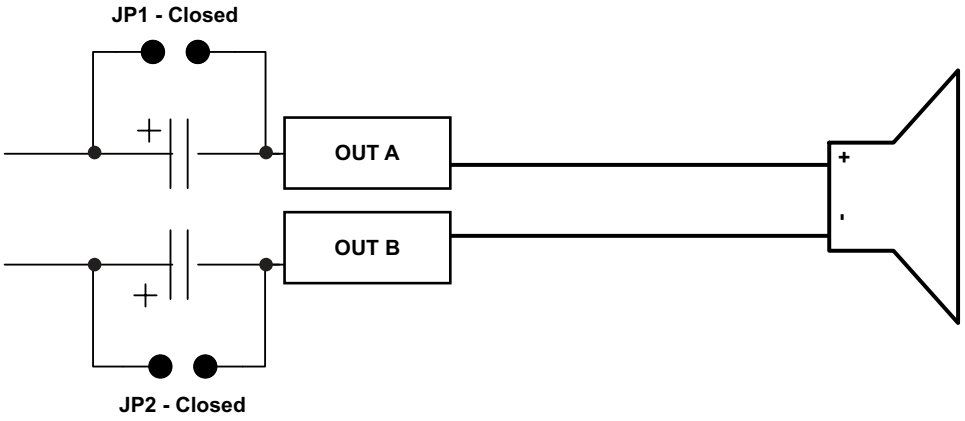


Figure 5. BTL Connection

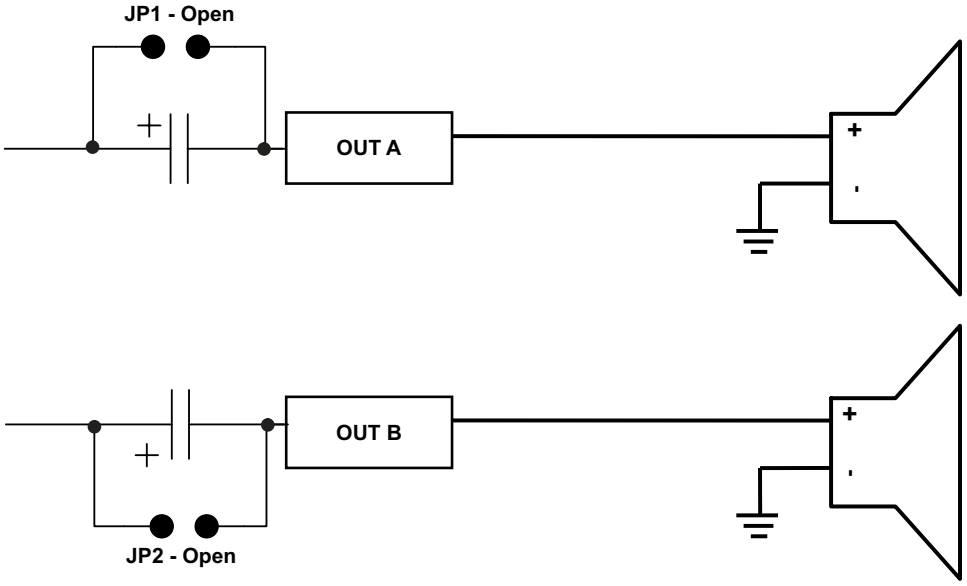


Figure 6. Single-Ended Connection

2.1.4 USB Interface

The TAS5706A registers are accessed through I²C™ bus lines SDA and SCL. The USB circuit and USB connector on the MC57xxPSIA board facilitates the connection between a host computer and the device. The EVM USB circuit is powered by the 5-V USB line of the host PC and is independent of the power supplies available on the board. The USB device that is used is a TAS1020B from Texas Instruments.

2.1.5 Digital Audio Interface SPDIF (RCA/OPTO)

The Digital Audio Interface accepts digital audio data using the I²S protocol. See the TAS5706A data sheet (SLOS606) for more information.

The RCA connector and the OPTO connector are the two SPDIF interfaces on the MC57xxPSIA board. The switch S3 toggles between the OPTO and RCA connector to accommodate the signal source. When the RCA cable or optical cable is connected and the signal source is powered up, verify that the SPDIF lock indicator (blue LED5) illuminates, confirming that a viable signal is available to the device. Install a jumper on JP4 across the middle pin and the pin marked SPDIF to connect the digital source to SDIN1.Install jumper on JP5 to connect the digital source to SDIN2.

For detailed information on how the data and clocks are provided to the TAS5706A, see the schematic appearing at the end of this document and the DIR9001 device data sheet (SLES198).

2.1.6 ADC Interface

In the absence of a digital signal source, the PCM1808 ADC can be used to convert an analog audio signal to a digital signal to the TAS5706A. The DIR9001 still provides clock signals to the ADC in this process. The DIR9001 oscillator frequency (Y2) determines the sampling frequency in the absence of a digital signal. If the OSC frequency is 24 MHz, the sampling frequency is set at 96 kHz; if the OSC is set at 12 MHz, the sampling frequency defaults to 48 kHz when no signal is on the SPDIF input terminals. A 12-MHz crystal is installed on the MC57xxPSIA board. The ADC is an additional feature of this board to provide flexibility in sourcing an audio signal to the TAS5706A. Review the PCM1808 data sheet (SLES177) for a detailed description of the ADC on this EVM. Install the jumper on JP4 across the middle pin and the pin marked ADC to select ADC as the source for SDIN1.Do the same for JP5 to select the ADC as the source for SDIN2. The jumpers JP2 and JP3 on MC57xxPSIA board are IN for 1 Vrms analog input and OUT for 2 Vrms inputs.

2.1.7 Board Power Up General Guidelines

Connect the MC-57xx and the TAS5706EVM2 boards by locating pin 1 on each board, indicated by a small white triangle. The MC-57xx plugs down onto the TAS5706EVM2 board (i.e., the TAS5706EVM2 board fits underneath the MC57xxPSIA board). Pin 1 on each board must be connected to each other.

Install the EVM software on the PC before powering up the board. After connecting the loudspeakers or other loads, power supplies, and the data line, power up the 5-V power supply first; then power up the PVCC power supply. It is recommended initially to set the PVCC level to 10 V, then ramp it up to 20 V to verify cable connections.

2.2 Software Installation

Download the TAS570X GDE from the CD or from the TI Web site, which always has the latest release of the GUI. Check versions for any updates to the GUI on the TI website.

Execute the GUI install program, Setup_TAS570X_version_number.exe

Once the program is installed, the program group and shortcut icon is created in Start → Program → Texas Instruments Inc → TAS570X GDE.

THE GUI come ups as shown in Figure 7.

Select the appropriate tab; in this case, select the TAS5705/TAS5706 tab.

It has two subwindows. One shows the Process Flow window. From the Process Flow window, each of the signal processing function tools can be selected by clicking on it. The Biquad GUI and the DRC GUI can be opened by using the right button of the mouse. This window also shows input select, Mode select, Channel, and Master Volume. All functions are shown in the order that they are in the device.

The other subwindow, Properties window, has the properties where a user can update by selecting from the available options. The properties that are available depends on the device selected. From the main window, the user must set three properties before connecting to the EVM.

Select the device, Enable/Disable auto bank switch function and set the sample rate. The TAS5706A automatically detects sample rates. The setting here is simply to synchronize the GUI and the device.

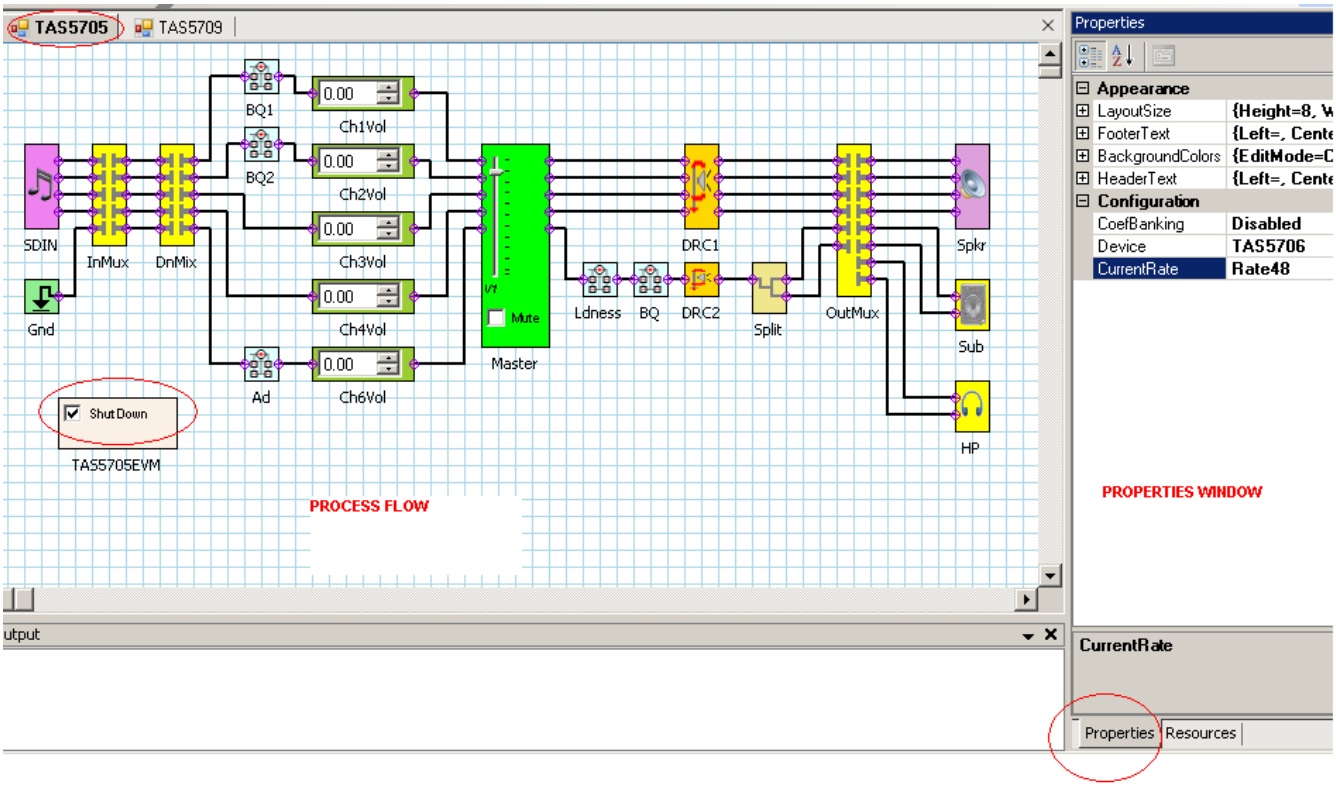


Figure 7. Graphical User Interface Initial Window

3 Using the EVM Software

3.1 Connect the GUI to the EVM

Once the properties window selections have been made, go to the menu Target → Connect.

This sends the initialization commands to the device. Master volume is in mute. Select the master volume function. Type the required volume in the properties window. For TAS5706A, type –12 dB. For TAS5705, type 0 dB. The difference is due the power stage gain in both devices. At this time, audio, if connected properly, plays through the device. Check All channel shutdown button. It must be un-checked. When the Connect command is issued, if an error appears that indicates a USB problem. Check the connections and press USB RESET button on the controller board. Then disconnect and re-connect from the Target menu.

3.2 I2C Memory Tool

This tool can be opened from GDE (Tools → I2C Memory Tool) or independent of GDE from Start → Program → Texas Instruments Inc → Memory Tool

Select I2C as show in Figure 8.

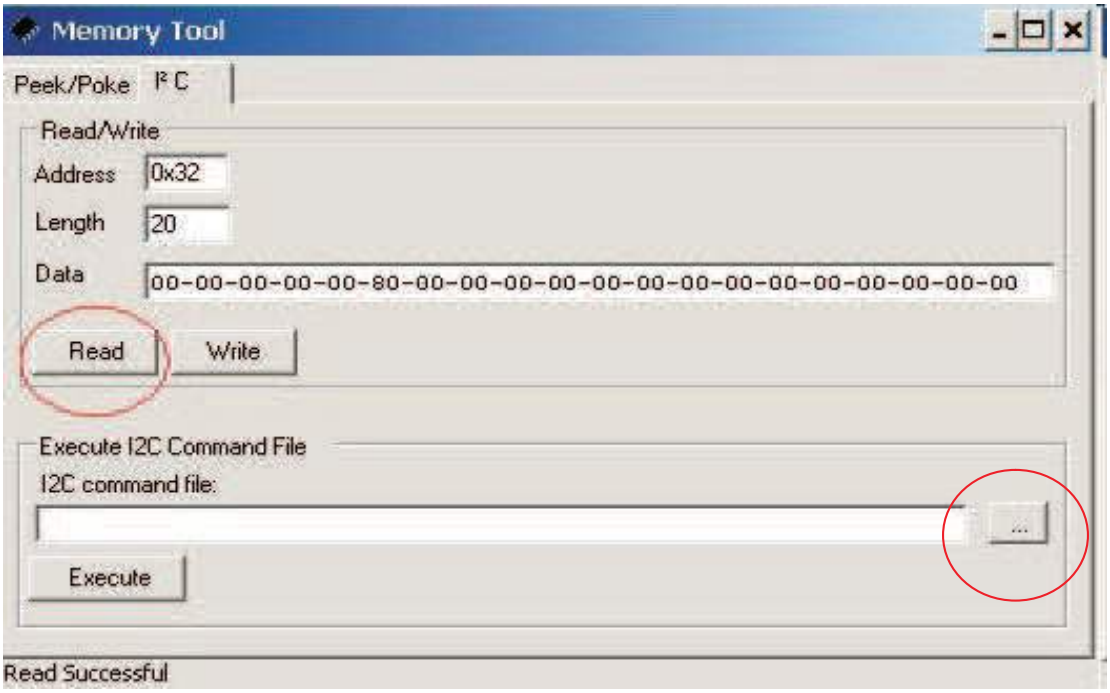


Figure 8. Memory Tool Window

I2C registers can be written or read using this tool. I2C command file can be sent by selecting the command file and *Execute* command.

3.3 Volume Function

Individual and Master volume can be selected, and the required volume value can be entered by typing on the property Window after selecting the function with the mouse (see Figure 9).

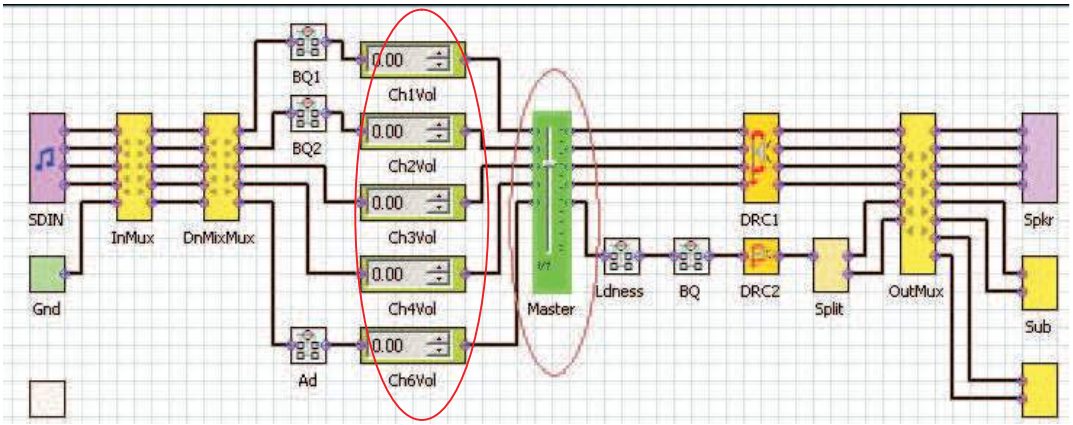


Figure 9. Volume Control

3.4 Biquad GUI

Using the right button of mouse, select Biquad GUI (Figure 10).

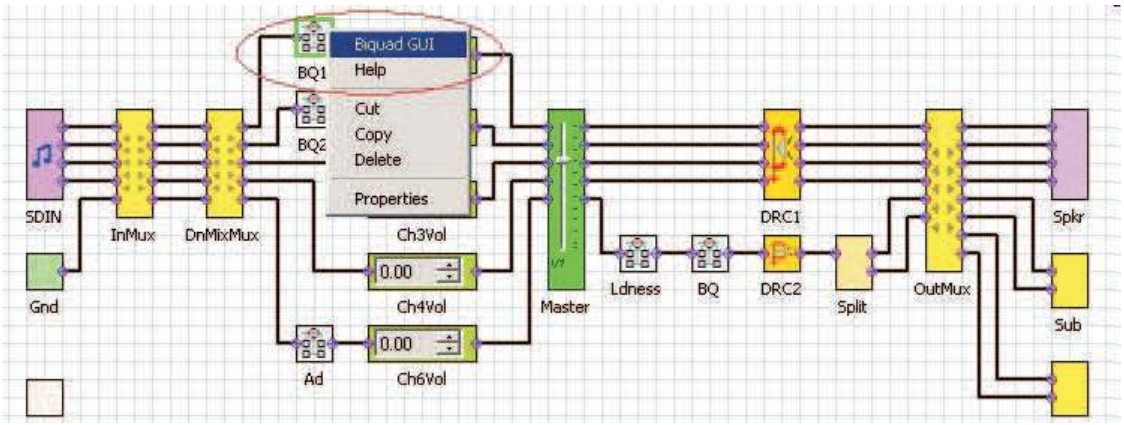


Figure 10. Selecting Biquad GUI

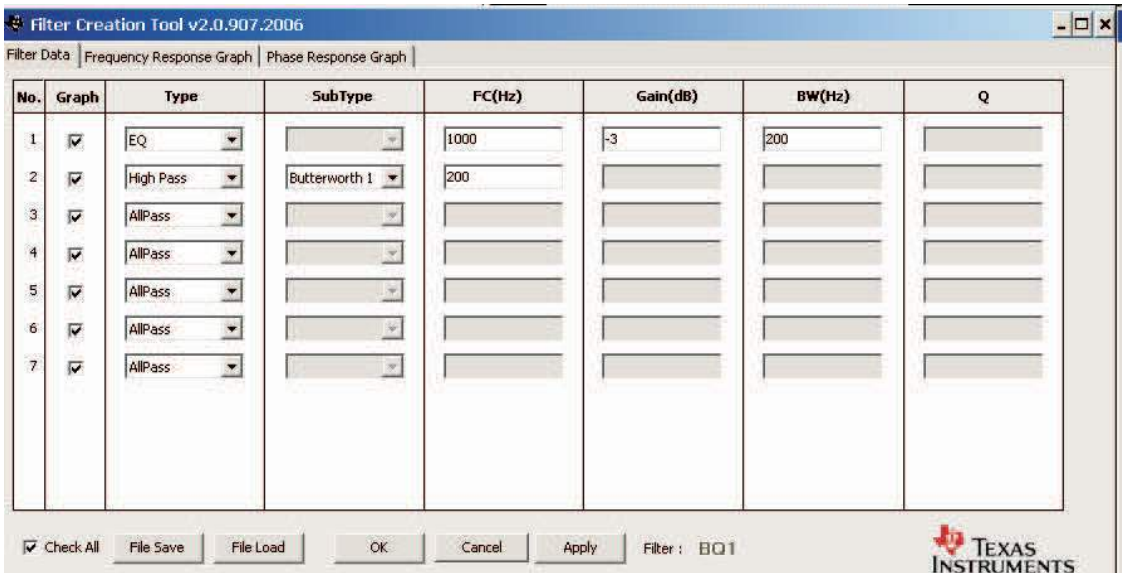


Figure 11. Filter Creation Tool Window

Check mark selects the Biquad. If not selected, the Biquad is in ALL PASS Mode.

Frequency response for the current settings can be viewed and adjusted in **Frequency Response Window** Tab (Figure 11). Individual Biquad Gains must be within ±12 db.

Apply from the filter data window sends all the three banks of coefficients (providing auto bank is enabled).

3.5 DRC GUI

Clicking on the function selects DRC GUI (Figure 12). Click on the DRC function, and check to see if DRC is enabled in the property window.

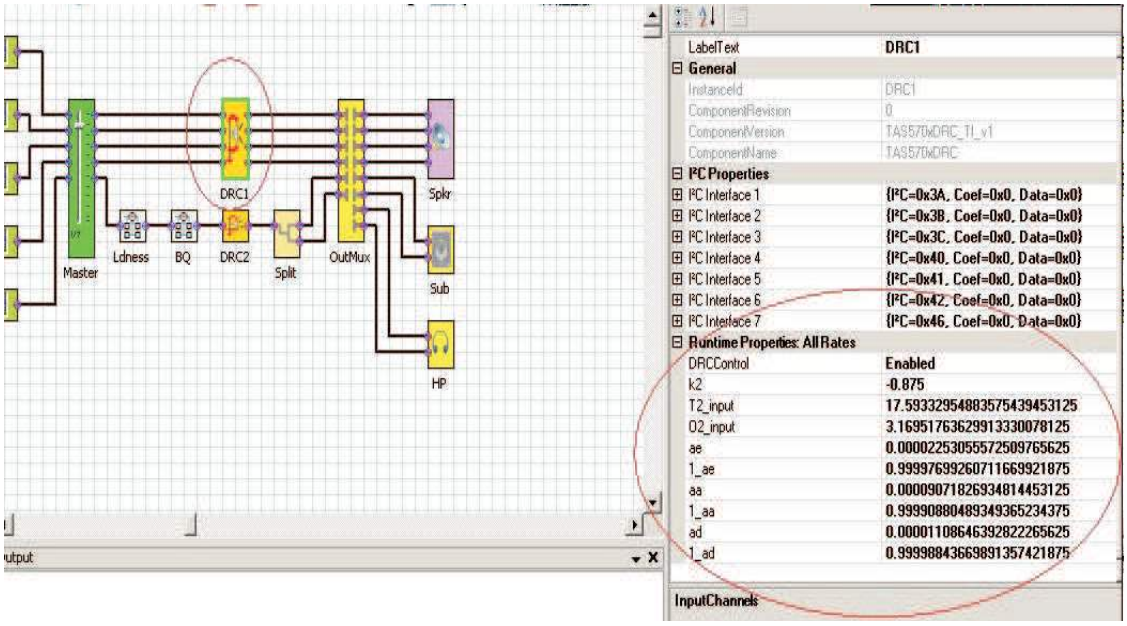


Figure 12. DRC Parameters

Next, using the right button of the mouse, select **Activate DRC GUI** (Figure 13).

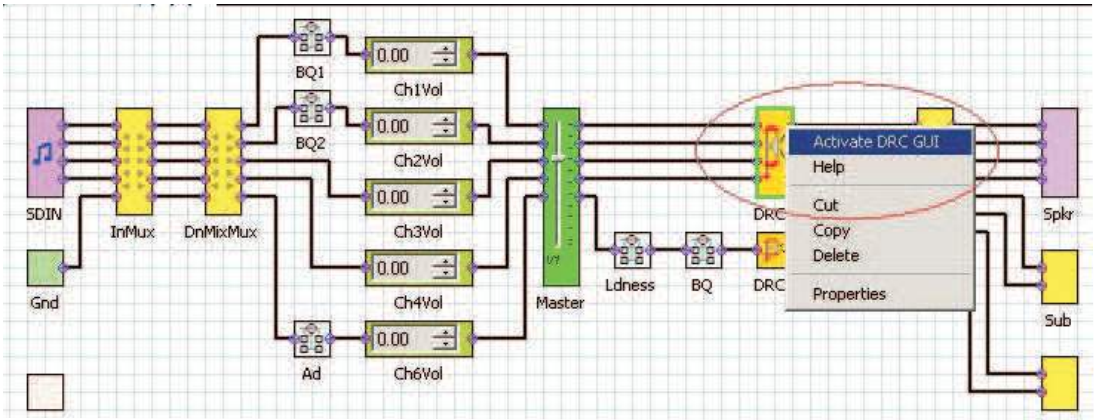


Figure 13. Activating the DRC GUI

Set the **compression ratio** to a value between 1 and 50.

The **offset** has a range of ±6 dB. *A value of 0* is illegal. If no offset is required, set the offset to 0. Offset is generally not required in a DRC application because is just provides a gain.

Threshold is selected with a value of 0 to –72 dB.

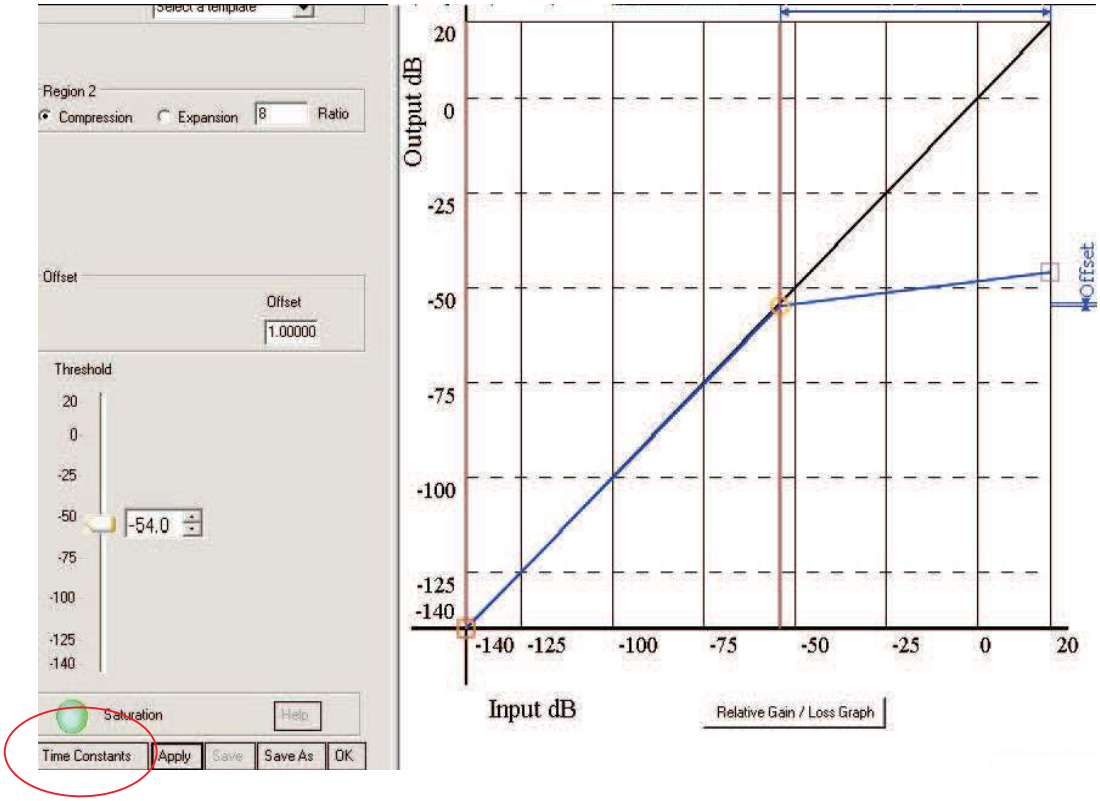


Figure 14. Time Constants Button

Time constants: Select the time constants to adjust the energy, attack, and decay filters (Figure 14).

3.6 Disable Biquads

The Biquads on channel1 and channel2 can be disabled from the GUI (Figure 15). Ensure that this is properly enabled before using Biquad GUI. Otherwise, changes on the GUI do not appear on the device output because the biquads (channel1 and channel2) are bypassed.

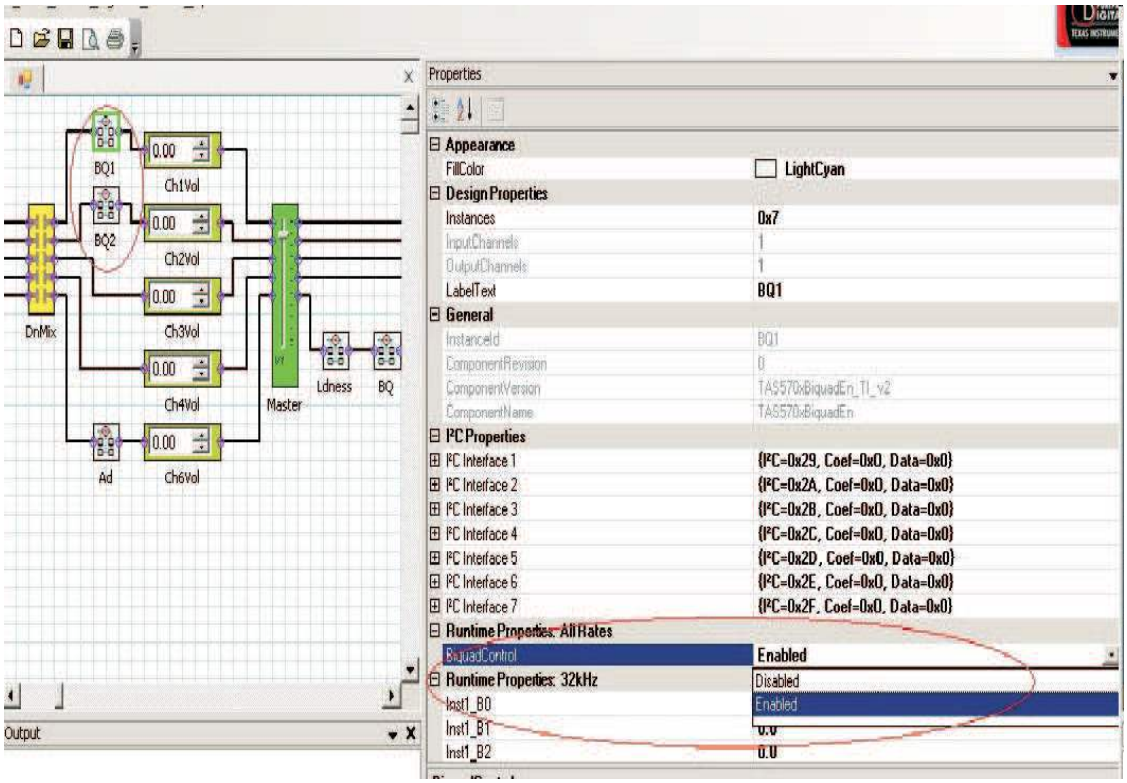


Figure 15. Disabling the Biquads

4 TAS5706EVM2 Quick-Start Setup Guide

This section discusses the five most common configurations of the TAS5706EVM2, and how to enable the headphone mode. For faster setup, you can load the I^2C initialization script of each configuration from the CD. Directions for loading initialization scripts follow this section.

Common Configurations:	Corresponding I^2C script
1. 2 × BTL BD	TAS5706_BD_2xBTL.ini
2. 2.1 AD (2 × SE via OutA and OutB) + 1 × BTL via OutC and OutD)	TAS5706_AD_2_1_2xSE_1BTL.ini
3. 2.1 BD (2 × BTL + 1 × BTL via J4 and external TAS5601EVM4)	TAS5706_BD_2_1_BTL_TAS5601.ini
4. 4 × SE AD	TAS5706_AD_4xSE.ini
5. 4.1 AD (4 × SE + 1 × BTL via J4 and external TAS5601EVM4)	TAS5706_AD_4_1_4xSE.ini
6. Headphone mode (J4)	HP_mode.ini
7. 2.1 and Lineout AD (2xBTL + 1 Subwoofer + 1 Lineout)	AD_BTL_subout_Lineout.ini

8.	2.1 and Lineout BD (2xBTL + 1 Subwoofer + 1 Lineout)	BD_BTL_subout_Lineout.ini

See Section 7 for details on how to set up each of these modes.

Note:

AD : AD Modulation- Outputs are 180° out of phase

BD : BD Modulation

BTL : Bridge-Tied Load

SE: Single-Ended Load

5 Jumpers and Control Utilities on MC57xxPSIA board

5.1 RCA/OPTICAL Jumpers

Select the jumper to reflect the source whether it is RCA or OPTICAL.

5.2 Switches

Reset is an active-low function. Pressing the master reset switch (S2) resets the TAS5706A resets device, USB RESET (S1) reset the USB bus, PDNZ(S4) power down TAS5706A and MUTE(S5) mutes (volume mute) TAS5706A.

5.3 LED Indicators

LED1 : USB Power connector installed at J1

LED2 : 3.3V Power is valid

LED3: RCA connection made

LED4: Optical connection made

LED5: SPDIF signal locked

LED6: FAULT (Not used with TAS5706EVM2)

LED7: PDN switch (S4) is depressed

LED8: MUTE switch (S5) is depressed

6 Board Layouts, Bill of Materials, and Schematic

6.1 TAS5706EVM2 and MC57xxPSIA Board Layouts

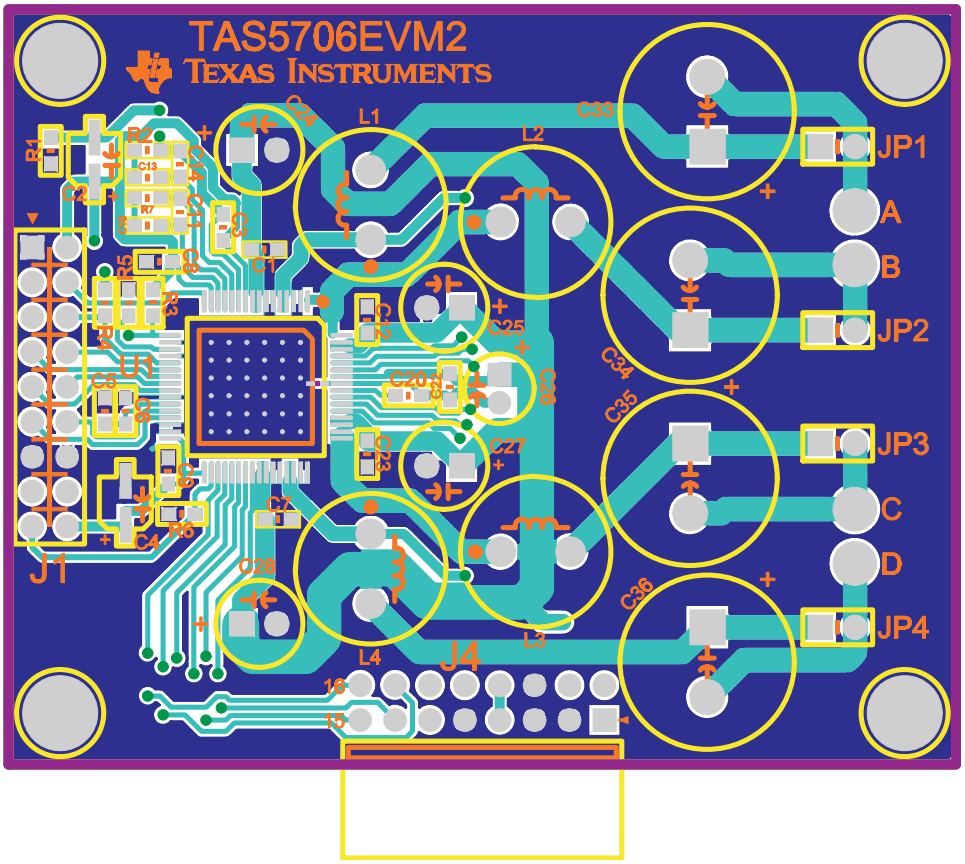


Figure 16. TAS5706EVM2 Top Assembly

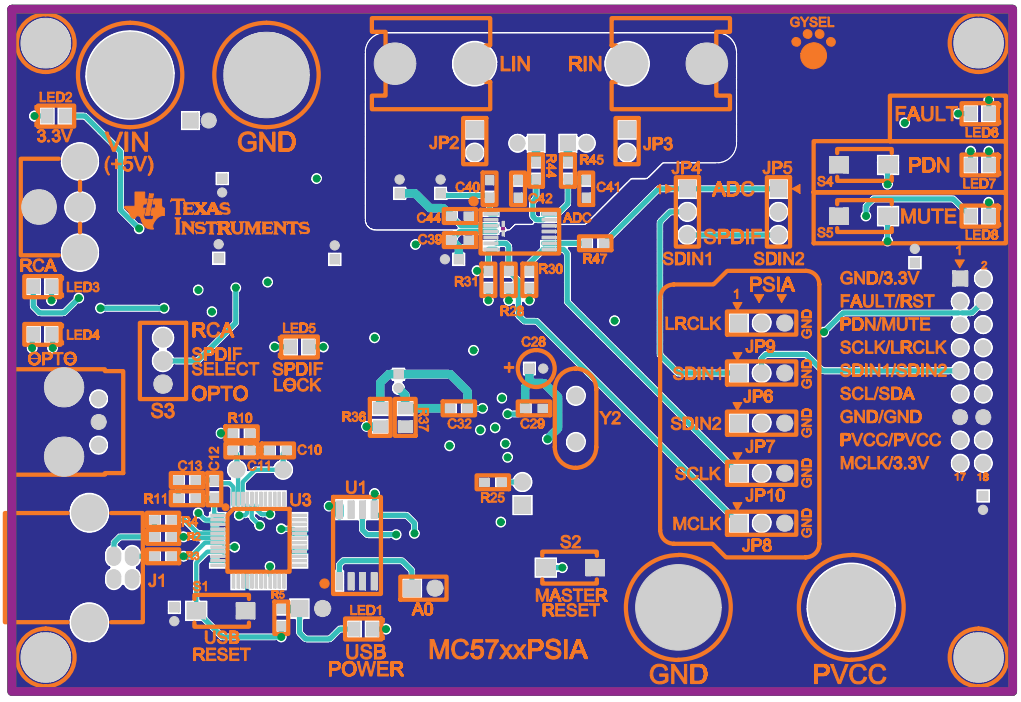


Figure 17. MC57xxPSIA Top Assembly

6.2 Bill of Materials

Table 2. Bill of Materials for TAS5706EVM2

TI SEMICONDUCTORS								
Item	**Description**	**Ref Des**	**Qty**	**MFG**	**MFG:Part No.**	**Vendor**	**Vendor: Part No.**	**Alt. Part No.**
1	Modulator/HBRIDGE TQFP64-PAP	U1	1	Texas Instruments	TAS5706APAP	Texas Instruments	TAS5706APAP	No Alt. Part Num
CAPACITORS								
2	CAP 4700PFD 50V CERM 0603 X7R	C11, C14	2	Panasonic	ECJ-1VB1H472K	Digi-Key	PCC1780TR	PCC1780CT
3	CAP 0.047UFD 16V CERM 0603 X7R	C10, C13	2	Panasonic	ECJ-1VB1C473K	Digi-Key	PCC1758TR	PCC1758CT
4	CAP 0.1UFD 16V CERM 0603 X7R	C3, C6, C8, C9	4	Panasonic	ECJ-1VB1C104K	Digi-Key	PCC1762TR	PCC1762CT
5	CAP 0.1UFD 50V CERM 0603 X7R	C1, C7, C12, C22, C23	5	Murata	GRM188R71H104KA93D	Digi-Key	490-1519-2	490-1519-1
6	CAP 0.22UFD 25V CERM 0603 X7R	C15–C18	4	Murata Electronics	GRM188R71E224KA88D	Digi-Key	490-3290-2	490-3290-1
7	CAP 4.7UFD 6.3V CERM 0603 X5R	C5	1	TDK Corp.	C1608X5R0J475M	Digi-Key	445-1417-2	445-1417-1
8	CAP 1.0UFD 25V CERM 0603 X5R ROHS	C19–C21	3	Taiyo Yuden	TMK107BJ105KA-T	Digi-Key	587-1248-2	587-1248-1
9	CAP 0.68UFD 50V CERM 1206 X7R ROHS	C29–C32	4	Kemet	C1206C684K5RACTU	Digi-Key	399-3500-2	399-3500-1
10	CAP 10UFD 16V ALUM ELEC SMD VSA	C2, C4	2	Panasonic	ECE-V1CS100SR	Digi-Key	PCE3061TR	PCE3061CT
11	CAP 15UFD 50V RAD ALUM ELEC FC	C26	1	Panasonic	EEU-FC1H150	Digi-Key	P10317	No Alt. Part Num
12	CAP 470UFD 35V HE ALUM ELEC ROHS	C33-C36	4	Panasonic	UHE1V471MHD6	Nichicon	493-1583	No Alt. Part Num
13	CAP 100UFD 35V RAD ALUM ELEC M	C24, C25, C27, C28	4	Panasonic	ECA-1VM101	Digi-Key	P5165	P10418TB
RESISTORS								
14	RES 0.0 Ω 1/16W 5% SMD 0603	R1	1	Panasonic	ERJ-3GEY0R00V	Digi-Key	P0.0GTR	P0.0GCT
15	RES 470 Ω 1/10W 5% SMD 0603	R2, R7	2	Panasonic	ERJ-3GEYJ471V	Digi-Key	P470GTR	P470GCT
16	RES 4.7K OHM 1/10W 5% SMD 0603	R9-R12	4	Panasonic	ERJ-3GEYJ472V	Digi-Key	P4.7KGTR	P4.7KGCT
17	RES 10 kΩ 1/16W 5% SMD 0603	R3, R4, R6, R8	4	Panasonic	9C06031A1002JLHFT	Digi-Key	311-10KGTR	311-10KGCT
18	RES 18.2 kΩ 1/10W 1% SMD 0603	R5	1	Yageo	9C06031A1822FKHFT	Digi-Key	311-18.2KHTR	311-18.2KHCT
INDUCTORS								
19	INDUCTOR, SERIES 11RHBP, 22UH	L1–L4	4	Toko America	No Manfact. Part Num	Toko America	A7503AY-220M	No Alt. Part Num
HEADERS								
20	Header, 2 Pin Male, PCB-RA, TIN W/Lock	J2, J3	2	JST	B2PS-VH	Digi-Key	455-1255	No Alt. Part Num
21	Header, 2 Pin Male, PCB Straight Gold ROHS	JP1, JP4	2	Sullins	PBC02SAAN	Digi-Key	S1011E-02	No Alt. Part Num
22	Header, 2X9 Pin Male, PCB Straight Gold ROHS	J1	1	Sullins	BC09DAAN	Digi-Key	S2011E-09	No Alt. Part Num
23	Socket Header, 2x8 Pin Female Gold PCB-RA	J4	1	Samtec	SSW-108-02-G-D-RA	Samtec	SSW-108-02-G-D-RA	No Alt. Part Num
SHUNTS								
24	SHUNT, BLACK AU FLASH 0.100	JP1-JP4	4	Sullins	SPC02SYAN	Digi-Key	S9001	No Alt. Part Num
STANDOFFS AND HARDWARE								
25	Standoff 4–40 Threaded M/F 0.50 in. ALUM-HEX	HW1–HW4	4	Keystone Electronics	8401	Digi-Key	8401K	No Alt. Part Num
26	Hex Nut, 4-40, Zinc/Steel	HW1–HW4	4	Building Fasteners	HNZ440	Digi-Key	H216	No Alt. Part Num

6.3 Schematic

The schematic for TAS5706EVM2 and MC57xxPSIA are located at the end of this document.

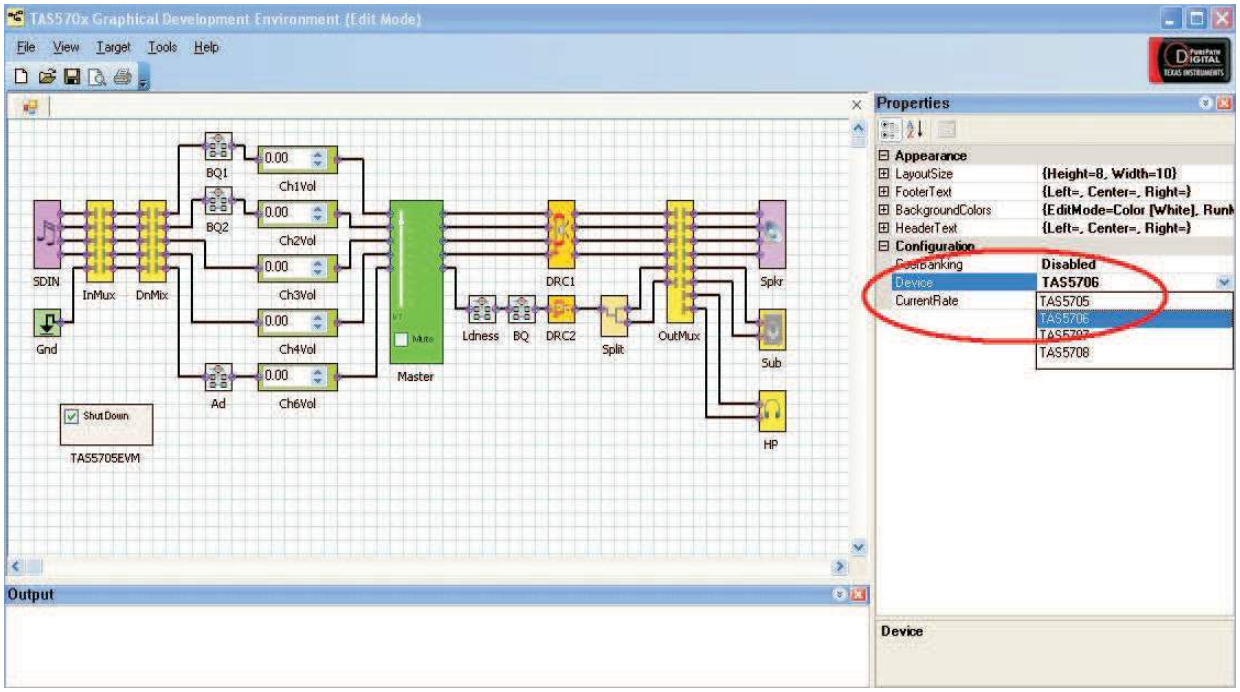
7 Quick-Start Setup Guide

This section discusses the five most common configurations of the TAS5706EVM2, and how to enable the Headphone mode.

Common Configurations:	Corresponding I²C Script
1. 2 × BTL BD	TAS5706_BD_2xBTL.ini
2. 2.1 AD (2 × SE + 1 × BTL via OutC and OutD)	TAS5706_AD_2_1_2xSE_1BTL.ini
3. 2.1 BD (2 × BTL + 1 × BTL via TAS5601)	TAS5706_BD_2_1_BTL_TAS5601.ini
4. 4 × SE AD	TAS5706_AD_4xSE.ini
5. 4.1 AD (4 × SE + 1 × BTL via TAS5601)	TAS5706_AD_4_1_4xSE.ini
6. Headphone mode	HP_mode.ini
7. 2.1 and Line out AD (2xBTL + 1 Subwoofer + 1 Line out)	AD_BTL_subout_Lineout.ini
8. 2.1 and Line out BD (2xBTL + 1 Subwoofer + 1 Line out)	BD_BTL_subout_Lineout.ini

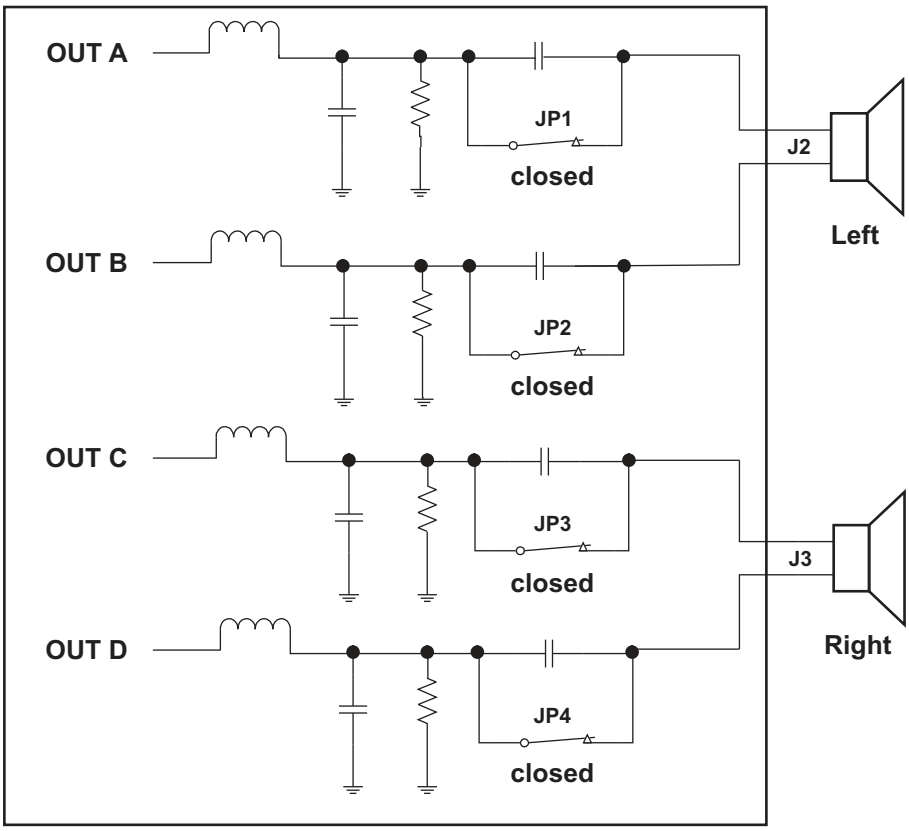
Before you begin:

- Follow all steps in the EVM Installation section (Section 2.1).
- Click on GUI background, and in the Properties sidebar, set Device to TAS5706A:

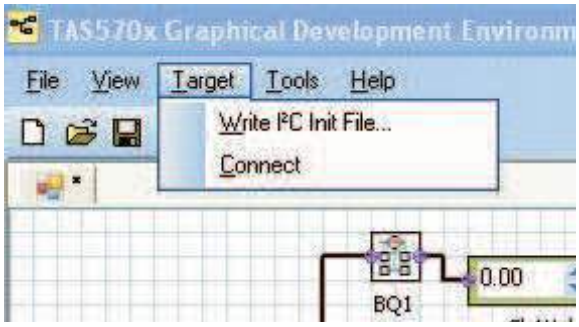


7.1 2 X BTL BD (Default: BD mode)

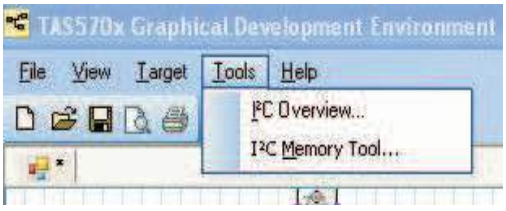
1. Set up the hardware as shown in the following illustration. Ensure that all the four jumpers (JP1-JP4) are plugged in. This provides you with BTL output configurations for both left and right channels.



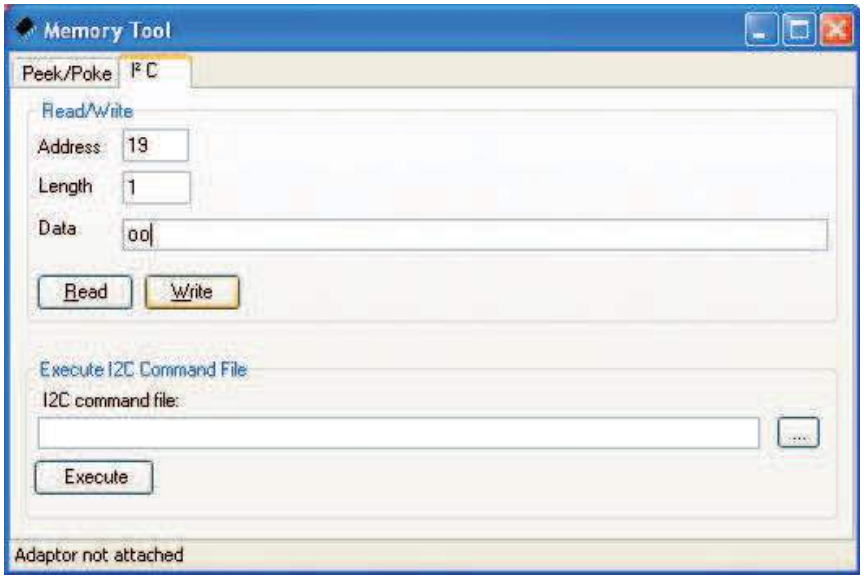
2. Go to Appendix A of this document, and save the script as **NAME.ini**. (**OR use the corresponding script from the CD or TI website)**.The format for the config file can be .ini or .CFG
3. Connect to the device: **Target > Connect**.



4. Go to **Tools > I²C Memory Tools**.



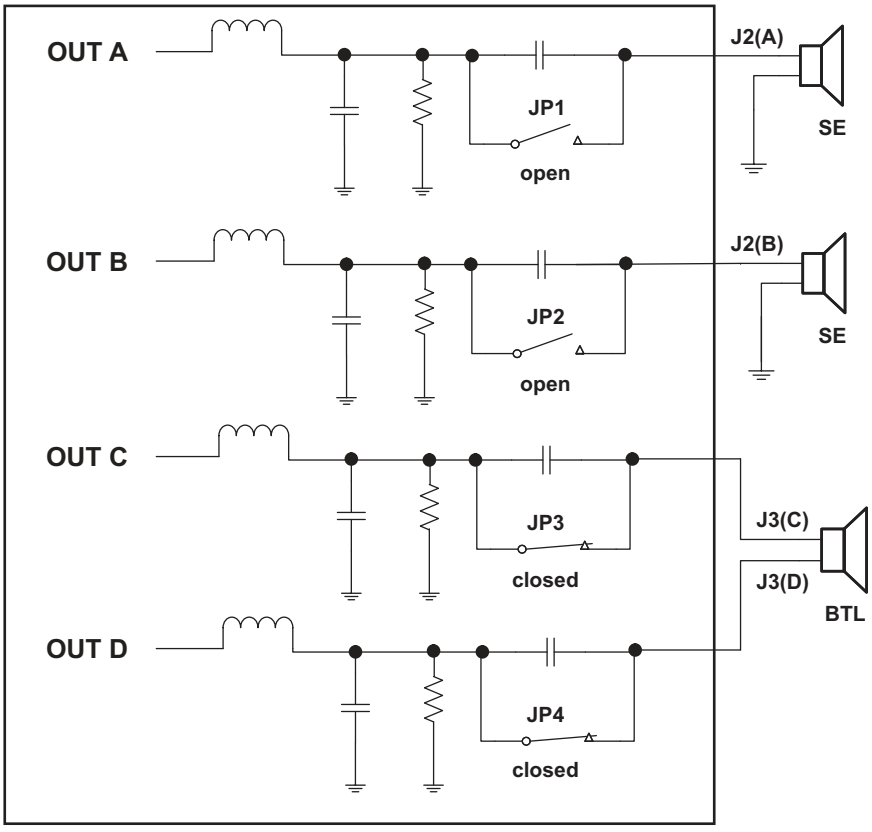
5. Click on the **I²C** tab, and upload the saved configuration script **NAME.ini** into the **I²C command File** window. Click **Execute**.



6. Finally uncheck the **shutdown** box to bring the device out of Shutdown mode, and adjust the **Master Volume** as desired.

7.2 2.1 AD (2 x SE + 1 x BTL via OutC and OutD)

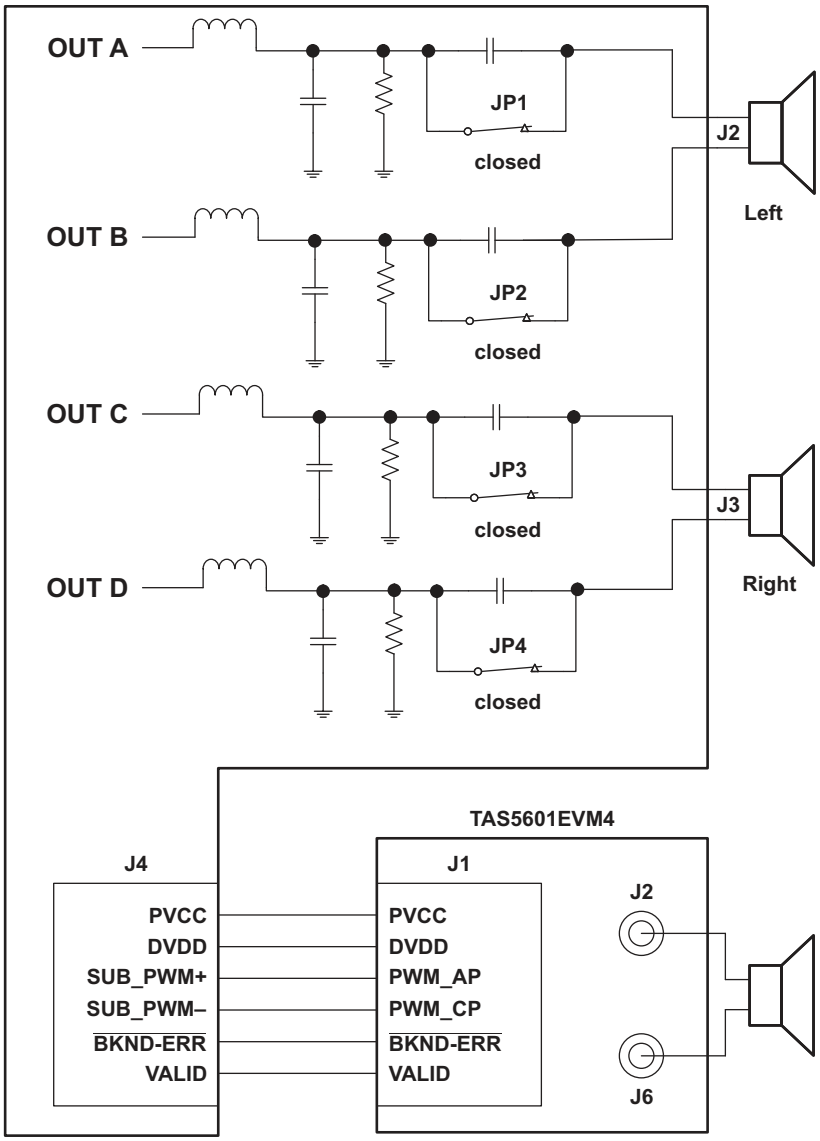
1. Set up the hardware configuration as shown in the following illustration. Ensure that the jumpers (JP1-JP4) for the two SE output channels (Out A and Out B) are removed, and jumpers for BTL output (Out C and Out D) are plugged in.



2. Go to Appendix B of this document, and save the script as **NAME.ini**.
3. Repeat steps 3 to 6 in Section 7.1 to load the I^2C command file.

7.3 2.1 BD (2 x BTL + 1 x BTL via external subwoofer amplifier TAS5601)

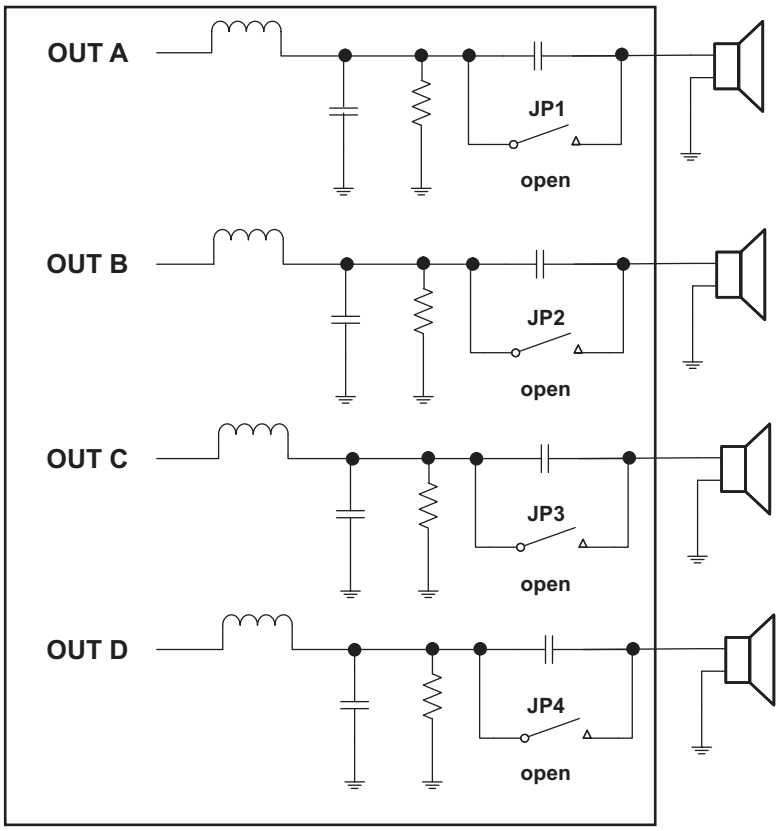
1. Set up the hardware as it is shown in the following illustration. Ensure that the jumpers (JP1-JP4) for OUT A, OUT B, OUT C, and OUTD are all plugged in. Connect the TAS5601EVM to the TAS5706EVM2 as well.



2. Go to Appendix C of this document, and save the script as **NAME.ini**
3. Repeat steps 3 to 6 in Section 7.1 to load I^2C command file.

7.4 4 x SE AD

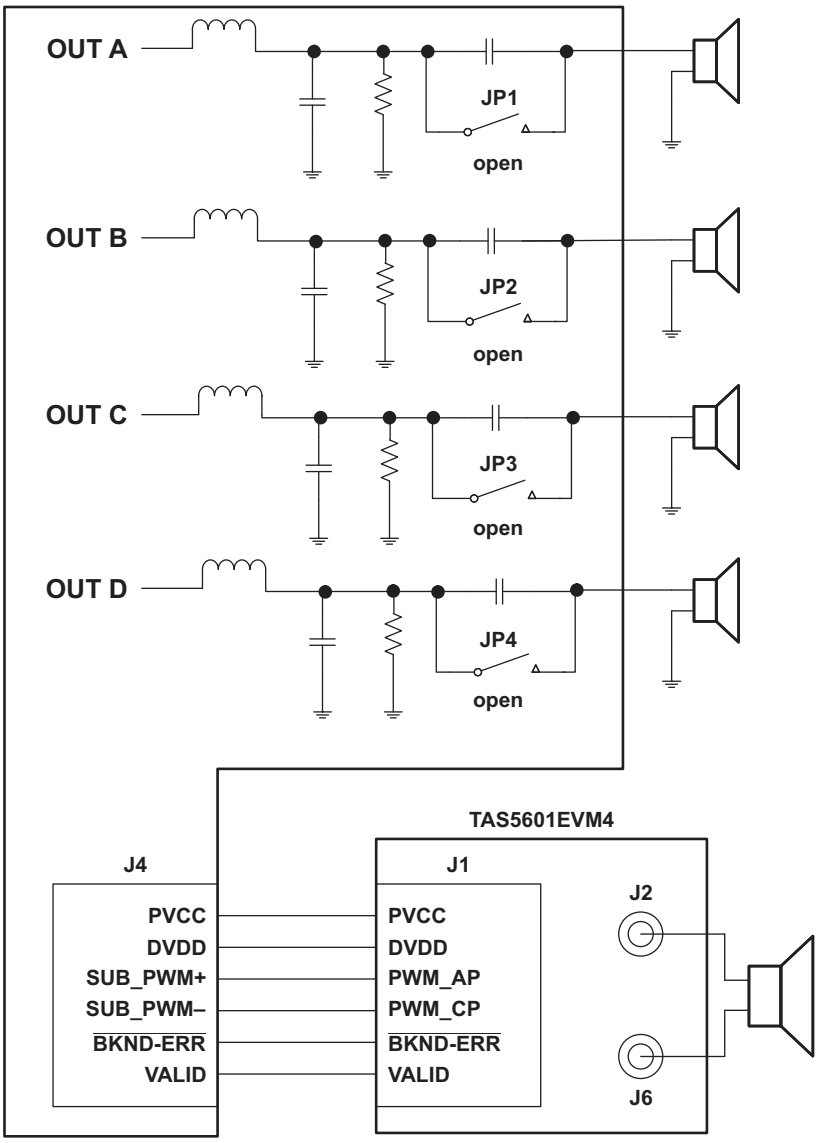
1. Connect the hardware as shown in the following illustration. Remove all four jumpers. This enables the DC blocking capacitors and provides SE output configurations for all four channels.



2. Go to Appendix D of this document, and save the script as **NAME.ini**
3. Repeat steps 3 to 6 in Section 7.1 to load I^2C command file.

7.5 4.1 AD (4 x SE + 1 x BTL via external subwoofer amplifier TAS5601)

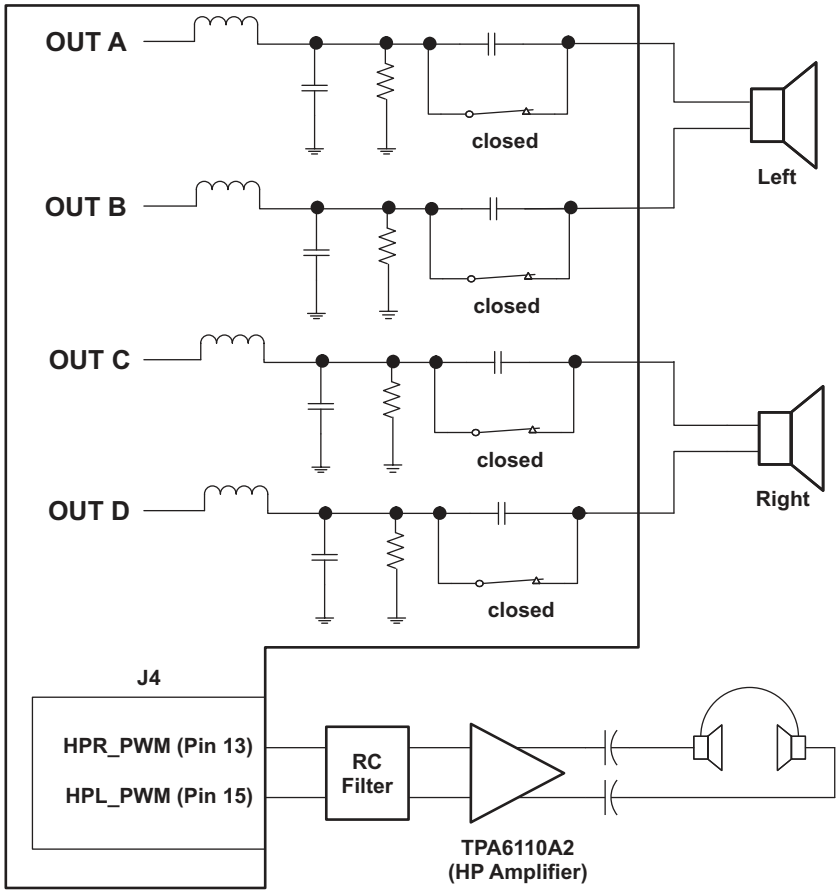
1. Set up the hardware as shown in the following illustration. Remove all the four jumpers for the SE output configurations. Connect the TAS5601EVM to the TAS5706EVM2.



2. Then go to Appendix E of this document, and save the script as **NAME.ini**
3. Repeat steps 3 to 6 in Section 7.1 to load I^2C command file.

7.6 Headphone AD

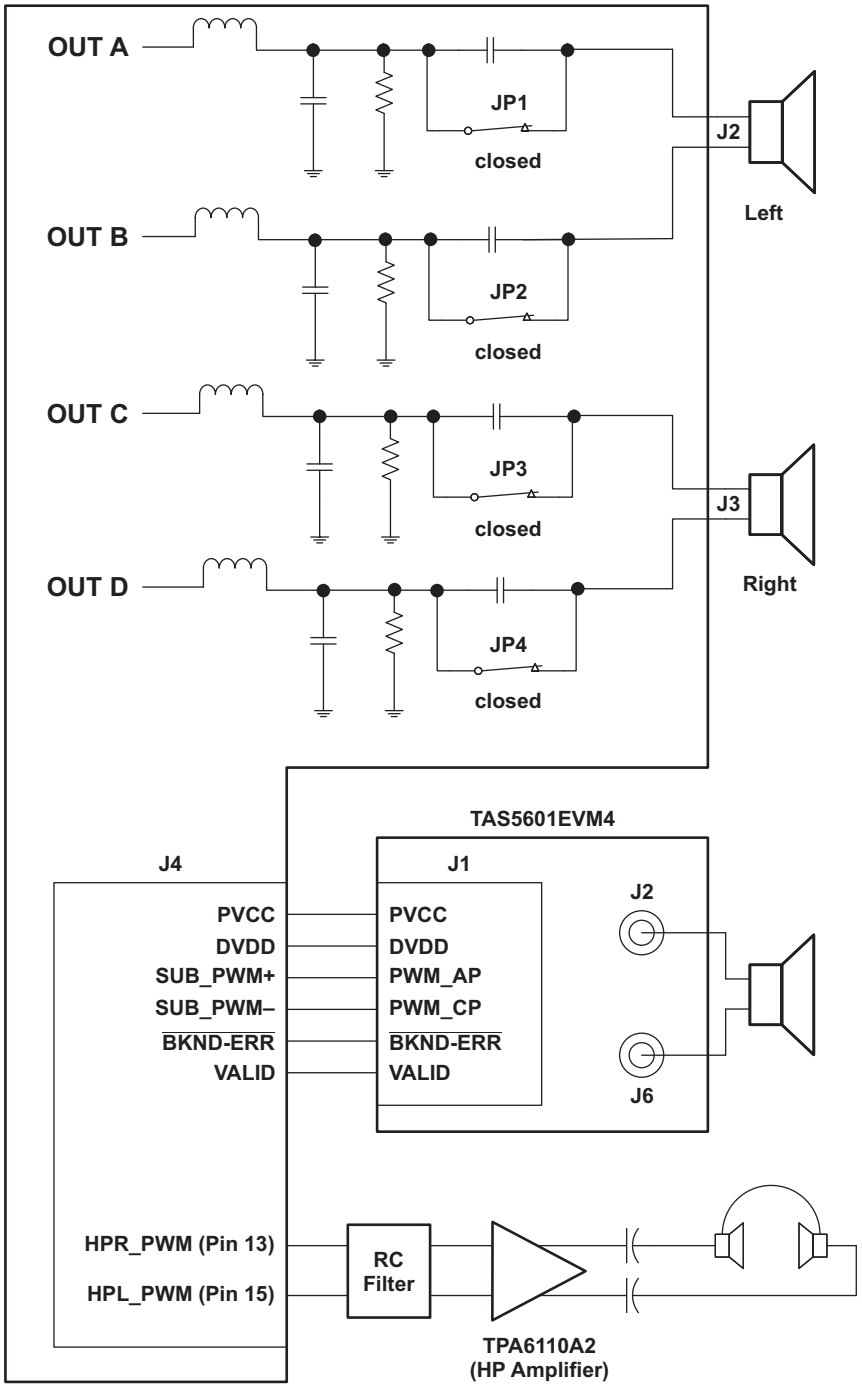
1. Set up the hardware as shown in the following illustration.



2. Go to Appendix F of this document, and save the script as **NAME.ini**
3. Repeat steps 3 to 6 in Section 7.1 to load I^2C command file.

7.7 AD 2.1 Mode and Line Out (2 x BTL Speaker Out + 1 Subwoofer Out + 1 Line Out, AD MODE)

1. Set up the hardware as shown in the following illustration.



2. Go to Appendix G of this document, and save the script as **NAME.ini**
3. Repeat steps 3 to 6 in Section 7.1 to load I^2C command file.

0 BD 2.1 Mode and Line Out (2 x BTL Speaker Out + 1 Subwoofer Out + 1 Line Out, BD MODE)

1. The hardware setup for the BD mode is the same as the setup for AD mode (step 1 of Section 7.7). All the speakers, subwoofer, and the headphone need to be connected to the TAS5706A.

2. Go to Appendix H of this document, and save the script as **NAME.ini**
3. Repeat steps 3 to 6 in Section 7.1 to load I^2C command file.

Appendix A 2 X BTL BD (Default: BD mode)

Following initial scripts may also be found on the installation CD or TI website. **The following scripts use .ini format where the first column is type of write command ("01" means single byte, "02" means multi-byte, "00" means comment), the following column is the I2C address and then followed by data(s).**

```
01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 00 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 30 Shutdown Group Resister
01 1A 0A Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 00 89 77 7A
00 01 (Below) Downmix Register
02 21 00 00 42 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 02 13 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 4C Inter-Channel Delay Channel 1
01 12 34 Inter-Channel Delay Channel 2
01 13 1C Inter-Channel Delay Channel 3
01 14 64 Inter-Channel Delay Channel 4
01 15 D0 Inter-Channel Delay Channel 5
01 16 90 Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)
```

Appendix B 2.1 AD (2 x SE + 1 x BTL via OutC and OutD)

01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 00 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 30 Shutdown Group Resister
01 1A 0A Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 02 01 66 72
00 01 (Below) Downmix Register
02 21 00 00 40 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 01 54 23
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 3C Inter-Channel Delay Channel 1
01 12 C0 Inter-Channel Delay Channel 2
01 13 00 Inter-Channel Delay Channel 3
01 14 00 Inter-Channel Delay Channel 4
01 15 00 Inter-Channel Delay Channel 5
01 16 08 Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)

Appendix C 2.1 BD (2 x BTL + 1 x BTL via External Subwoofer TAS5601)

```
01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 20 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 00 Shutdown Group Resister
01 1A 0A Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 00 89 77 7A
00 01 (Below) Downmix Register
02 21 00 00 40 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 02 13 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 4C Inter-Channel Delay Channel 1
01 12 34 Inter-Channel Delay Channel 2
01 13 1C Inter-Channel Delay Channel 3
01 14 64 Inter-Channel Delay Channel 4
01 15 D0 Inter-Channel Delay Channel 5
01 16 90 Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)
```

Appendix D 4 x SE AD

```
01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 00 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 30 Shutdown Group Resister
01 1A 95 Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 0A 01 23 66
00 01 (Below) Downmix Register
02 21 00 00 40 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 01 23 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 20 Inter-Channel Delay Channel 1
01 12 A0 Inter-Channel Delay Channel 2
01 13 E0 Inter-Channel Delay Channel 3
01 14 60 Inter-Channel Delay Channel 4
01 15 04 Inter-Channel Delay Channel 5
01 16 FC Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)
```

Appendix E 4.1 AD (4 x SE + 1 x BTL via External Subwoofer TAS5601)

01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 20 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 00 Shutdown Group Resister
01 1A 95 Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 0A 01 23 72
00 01 (Below) Downmix Register
02 21 00 00 42 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 01 23 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 20 Inter-Channel Delay Channel 1
01 12 A0 Inter-Channel Delay Channel 2
01 13 E0 Inter-Channel Delay Channel 3
01 14 60 Inter-Channel Delay Channel 4
01 15 04 Inter-Channel Delay Channel 5
01 16 FC Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)

Appendix F Headphone AD

01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 02 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 3C Shutdown Group Resister
01 1A 95 Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 00 01 66 66
00 01 (Below) Downmix Register
02 21 00 00 42 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 02 13 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 5C Inter-Channel Delay Channel 1
01 12 24 Inter-Channel Delay Channel 2
01 13 54 Inter-Channel Delay Channel 3
01 14 2C Inter-Channel Delay Channel 4
01 15 A4 Inter-Channel Delay Channel 5
01 16 AC Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)

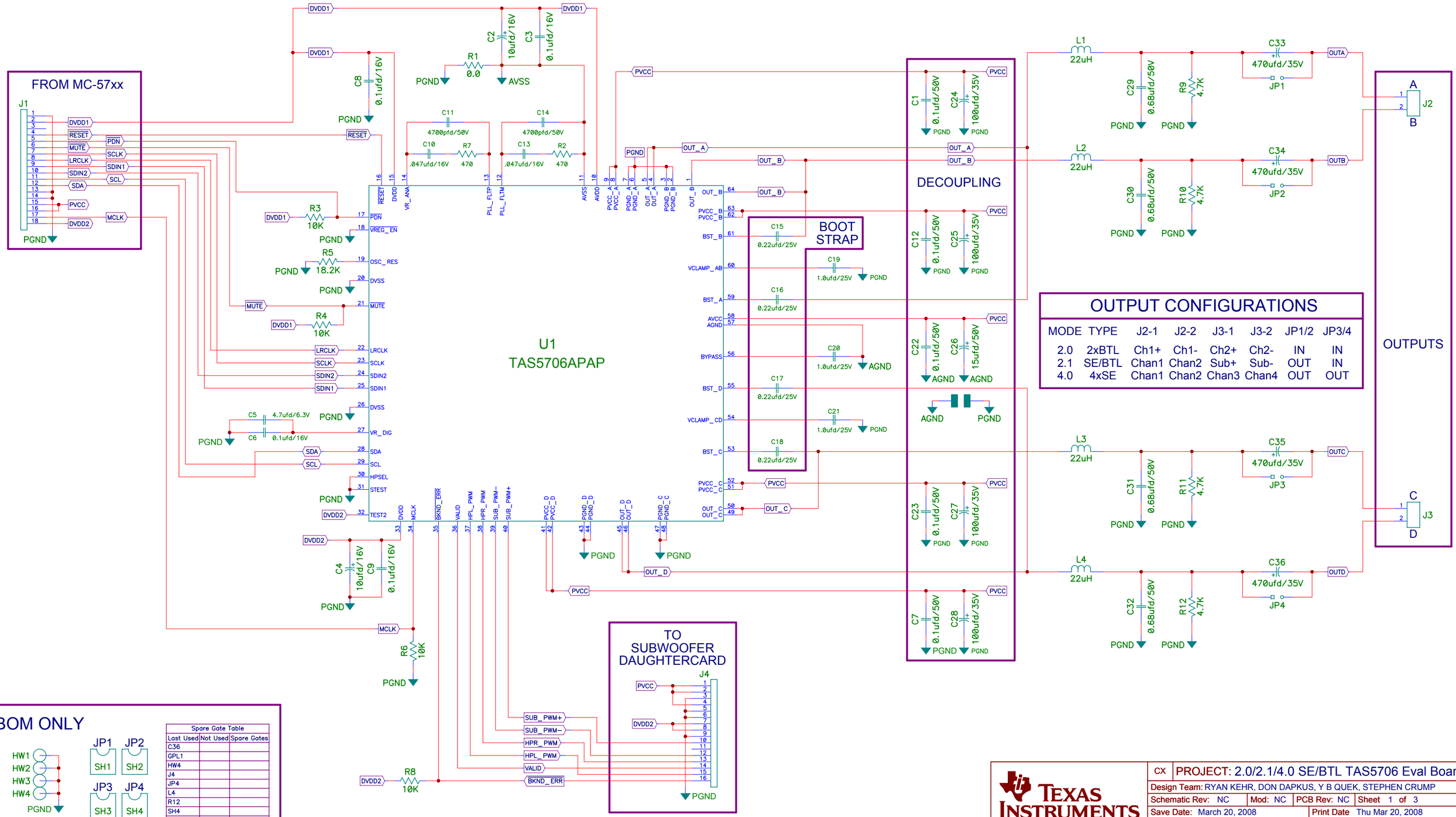
Appendix G 2.1 and Line out AD (2 x BTL Speaker Out + 1 Subwoofer + 1 Line out, AD MODE)

01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 24 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 00 Shutdown Group Resister
01 1A 0F Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 00 01 77 72
00 01 (Below) Downmix Register
02 21 00 00 40 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 02 13 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 5C Inter-Channel Delay Channel 1
01 12 24 Inter-Channel Delay Channel 2
01 13 54 Inter-Channel Delay Channel 3
01 14 2C Inter-Channel Delay Channel 4
01 15 A4 Inter-Channel Delay Channel 5
01 16 AC Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)

Appendix H 2.1 and Line out BD (2 x BTL Speaker + 1 Subwoofer Out + 1 Line out, BD MODE)

01 1B 00 Oscillator Trim
01 03 A0 System Control Register 1
01 04 05 Serial Data Interface Register
01 05 24 System Control Register 2
01 06 00 Soft Mute Register
01 07 FF Master Volume Register (0xFF = Mute)
01 08 30 Channel 1 Volume
01 09 30 Channel 2 Volume
01 0A 30 Channel 3 Volume
01 0B 30 Channel 4 Volume
01 0C 30 Channel 5 Volume
01 0D 1C Channel 6 Volume
01 0E 91 Micro Register
01 10 02 Modulation Limit
01 18 0F PWM Start Register
01 19 00 Shutdown Group Resister
01 1A 0A Split Capacitor Charge Period
01 1C 02 Back-end Error Register
00 01 (Below) Input Mux Register
02 20 00 89 77 7A
00 01 (Below) Downmix Register
02 21 00 00 40 03
00 01 (Below) AM Mode Register
02 22 00 00 00 00
00 01 (Below) Biquad1 Coeff
02 23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) Biquad2 Coeff
02 24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 01 (Below) PWM Output MUX Register (Note: Writes to this register affect Inter-Channel Delay)
02 25 01 02 13 45
00 01 (Below) 1/G
02 26 00 80 00 00
00 01 (Below) Scale = 1/(1-1/G)
02 28 00 80 00 00
01 11 4C Inter-Channel Delay Channel 1
01 12 34 Inter-Channel Delay Channel 2
01 13 1C Inter-Channel Delay Channel 3
01 14 64 Inter-Channel Delay Channel 4
01 15 D0 Inter-Channel Delay Channel 5
01 16 90 Inter-Channel Delay Channel 6
01 17 00 Offset Register (Absolute Delay)

TAS5706A 2.0/2.1/4.0 SE/BTL Evaluation Board



OUTPUT CONFIGURATIONS

MODE	TYPE	J2-1	J2-2	J3-1	J3-2	JP1/2	JP3/4
2.0	2xBTL	Ch1+	Ch1-	Ch2+	Ch2-	IN	IN
2.1	SE/BTL	Chan1	Chan2	Sub+	Sub-	OUT	IN
4.0	4xSE	Chan1	Chan2	Chan3	Chan4	OUT	OUT

BOM ONLY

HW1
HW2
HW3
HW4
PGND

JP1 SH1
JP2 SH2
JP3 SH3
JP4 SH4

Spare Gate Table		
Last Used	Not Used	Spare Gates
C36		
GPL1		
HW4		
J4		
JP4		
L4		
R12		
SH4		
U1		

TEXAS INSTRUMENTS

CX	PROJECT: 2.0/2.1/4.0 SE/BTL TAS5706 Eval Board		
Design Team: RYAN KEHR, DON DAPKUS, Y B QUEK, STEPHEN CRUMP			
Schematic Rev: NC	Mod: NC	PCB Rev: NC	Sheet 1 of 3
Save Date: March 20, 2008		Print Date	Thu Mar 20, 2008
Filename: TAS5706EVM2.SCH			Drawn By: LDN

USB INTERFACE

ENGINEERING EVALUATION ONLY

USB BOOT EPROM

3.3V-USB, R1 4.7K, A0, GND

U1 24LC64: A0, A1, A2, GND, Vcc, WP, SCL, SDA; 3.3V-USB, SCL, SDA

(A0 IN DEFAULT)

R8 4.7K 3.3V-USB

R9 4.7K

SCL, SDA

TO EVM BOARD

SCL, SDA

USB I/O

J1: Vcc, Data+, Gnd Shield, Data-

R4 1.50K PUR

R2 27.4 DP

R3 27.4 DM

C2 47pfd/50V, C3 47pfd/50V

FB1 GND_USBIN

GND

USB RESET

S1 GND

MRESET

U3 TAS1020BPFB

C10 27pfd/50V, C11 27pfd/50V, Y1 6.000MHz, XTALO, XTALI

R10 0.0

C12 100pfd/50V, C13 1000pfd/50V

R11 3.09K

AVSS-USB

3.3V-USB

SCL, SDA, PUR, DP, DM, MRESET

TEST, EXTEN, RSTO, RESET, VREN

PLLFILO, AVDD, AVSS, PLLFIL, XTAL, XTALO, MCLKI

MCLKO2, MCLKO1, CDATO, CSCLK, CDATI, CSYNC, CRESET, CSCHNE

P1.7, P1.6, P1.5, P1.4, P1.3, P1.2, P1.1, P1.0, NC, NC, P3.5, P3.4, P3.3, P3.2/XINT, P3.1, P3.0

DVDD x3, DVSS x3

GND

U2

U2: GND, EN, IN, IN, RESET, NC, OUT, OUT; TPS77533D

VCC-USB, FB2, 5V-USB

C1 10ufd/16V

R5 249K

C4 68ufd/6.3V

DECOUPLING

U1-8, U3-8, U3-21, U3-33, U3-2

C5 0.1ufd/50V, C6 0.1ufd/50V, C7 0.1ufd/50V, C8 0.1ufd/50V, C9 0.1ufd/50V

R7 0.0

3.3V-USB, AVSS-USB

LED1

3.3V-USB, LED1 Green, R6 392, GND

CX	PROJECT: EVM CONTROLLER BOARD
Design Team:	YONG GWAN KIM
Schematic Rev: NC	Mod: NC | PCB Rev: NC | Sheet 1 of 5
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SPDIF RECEIVER

ENGINEERING EVALUATION ONLY

SPDIF INPUT

RCA, GND

OPTO — TORX147LFT (+3.3V, Vcc, GND, Shield, Shield, OUT) → OPTO-IN

R13 75.0 Ω

C15 0.047ufd/16V

R15 100

R17 1.00M

INV1 — 74AHC1GU04 (NC, GND, Vcc)

C18 0.047ufd/16V

R20 2.00K

R21 7.50K

INV2 — 74AHC1GU04 (NC, GND, Vcc)

SPDIF INPUT SELECT

1-2: OPTO INPUT
2-3: RCA INPUT

+3.3V, R14 1.0K, S3, GND

RCA INPUT (LOW)

+3.3V, 4.7K, Q1, LED3 Green, R18 357, GND

OPTO INPUT (HIGH)

LED4 Green, R19 357, +3.3V, Q2, 4.7K, GND

MUX

SN74LVC2G157DCT (A, B, Y, Ȳ, A/B, G, GND, Vcc, +3.3V)

RXIN

U5

DIR9001PW

AUDIO, FSOUT0, FSOUT1, SCKO, Vdd, DGND, XTO, XTI, CLKST, LRCKO, BCKO, DOUT, PSCK0, PSCK1, CKSEL, ERROR, FMT1, FMT0, Vcc, AGND, FILT, RST, RXIN, RSV, BFRAME, EMPH, UOUT, COUT

SCKO, R28 47, MCLK

R32 100

R23 0.0, C23 33pfd/50V, R26 470, Y2 12.288MHz, C24 33pfd/50V

C26 4700pfd/50V, R33 680, C27 0.068ufd/16V, AGND-SPDIF

DATA FORMAT

	FMT1	FMT0
24Bit/MSB/I2S	H	H

FMT1, FMT0, R34 0.0, R35 0.0, +3.3V

3.3V-SPDIF, AGND-SPDIF

JP1

+3.3V, R24 4.99K, JP1, R25 4.99K, GND, PSCK0, PSCK1

JP1 IN: SCKO = 512 Fs
JP1 OUT: SCKO = 256 Fs (DEFAULT)

DOUT, BCKO, LRCKO, R29 47, R30 47, R31 47

DOUT-SPDIF, SCLK, LRCLK

SPDIF LOCK

+3.3V, 4.7K, Q3, LED5 Blue, R38 392, GND

TO ADC

MCLK, DOUT-SPDIF, SCLK, LRCLK

TO EVM BOARD

MCLK, DOUT-SPDIF, SCLK, LRCLK, RST

MASTER RESET

+3.3V, R12 4.99K, S2, GND, U4 TPS3825-33DBVT (Vdd, MR, Gnd, Reset, Reset), RST

RST

TO EVM BOARD

+3.3V

TO SPDIF

+3.3V

TO ADC

+3.3V

SPDIF DECOUPLING

+3.3V, U5-5, OPTO-3, R36 0.0, U5-24, U5-24, 3.3V-SPDIF

C28 10ufd/16V, C29 0.1ufd/16V, C30 0.1ufd/16V, R37 0.0, C31 10ufd/16V, C32 0.1ufd/16V, AGND-SPDIF, GND

5V POWER INPUT

VIN, Red, 5V, Black, GND, GND

TO ADC: 5V

C14 47ufd/16V, C16 0.1ufd/16V, C17 22ufd/10V, C19 0.1ufd/16V, GND

VR1 — TPS76733QD (IN, IN, OUT, OUT, NC, EN, Gnd, Reset)

3.3V@1A

R22 249K

C20 22ufd/10V, C21 10ufd/16V, C22 10ufd/16V, C48 10ufd/16V, C25 0.1ufd/16V, C45 0.1ufd/16V, C46 0.1ufd/16V, C47 0.1ufd/16V

U4-5, INV1-5, INV2-5, MUX-5

LED2 Green, R16 332, GND

Design Team:	YONG GWAN KIM		
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CX | PROJECT: EVM CONTROLLER BOARD | Sheet 2 of 5 | Drawn By: LDN

TEXAS INSTRUMENTS

ADC / CONNECTOR I/O

ENGINEERING EVALUATION ONLY

NOTES ON JUMPERS
IN: LIN/RIN = 1Vrms MAX.
OUT: LIN/RIN = 2Vrms MAX.

ANALOG INPUTS
LIN — LEFT–IN — AGND–ADC
RIN — RIGHT–IN — AGND–ADC

JP2 R39 4.99K C35 1ufd/50V
JP3 R40 4.99K C36 1ufd/50V
C33 470pfd/100V
C34 470pfd/100V
R41 4.99K
R42 4.99K
R44 100
R45 100
C41 0.01ufd/16V
C42 0.01ufd/16V
VINL
VINR

ADC
PCM1808PW
VREF AGND Vcc Vdd DGND SCKI LRCK
VINR VINL FMT MD1 MD0 DOUT BCK
C38 10ufd/16V
C40 0.1ufd/16V
AGND–ADC
5VA–ADC
3.3VD–ADC
MCLK
LRCLK
R47 47
SCLK
GND

FROM SPDIF
MCLK LRCLK SCLK DOUT–SPDIF

FROM USB
SCL SDA

FROM MASETER RESET
RST

FROM VR1
+3.3V

HIGH POWER INPUT
PVCC
Red — PVCC–IN
Black — GND

FAULT
+3.3V — R48 392 — GND
LED6 Green
Q4 4.7K
R52 100K +3.3V
FAULT

PDN
+3.3V — R49 392 — GND
LED7 Green
Q5 4.7K
S4
R51 10K +3.3V
PDN

MUTE
+3.3V — R50 392 — GND
LED8 Green
Q6 4.7K
S5
R27 10K +3.3V
MUTE1

DOUT–ADC
DOUT–SPDIF
JP4 (SDIN1)
JP5 (SDIN2)

JP6 SDIN1EVM
JP7 SDIN2EVM
JP8 MCLKEVM
JP9 LRCLKEVM
JP10 SCLKEVM
MC012 (1-2)
PSIA (2-3)
GND

TO EVM BOARDS
J2
+3.3V RST MUTE1 LRCLKEVM SDIN2EVM SDA PVCC–IN +3.3V
FAULT PDN SCLKEVM SDIN1EVM SCL MCLKEVM GND

3.3V DECOUPLING
+3.3V — R43 3.3 — ADC–4 ADC–4 — 3.3VD–ADC
C37 10ufd/16V
C39 0.1ufd/16V
GND

5V DECOUPLING
5V — R46 4.7 — ADC–3 ADC–3 — 5VA–ADC
C43 10ufd/16V
C44 0.1ufd/16V
GND — AGND–ADC

TEXAS INSTRUMENTS

CX	PROJECT: EVM CONTROLLER BOARD			
Design Team: YONG GWAN KIM				
Schematic Rev: NC	Mod: NC	PCB Rev: NC	Sheet 3 of 5	
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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -0.5 V to 4.1 V and the output voltage range of 1 Vrms.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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