



STL23NM50N

N-channel 500 V, 0.170 Ω typ., 14 A MDmesh™ II Power MOSFET
in a PowerFLAT™ 8x8 HV package

Datasheet — production data

Features

Type	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STL23NM50N	550 V	< 0.210 Ω	14 A ⁽¹⁾

1. The value is rated according to R_{thj-case}

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

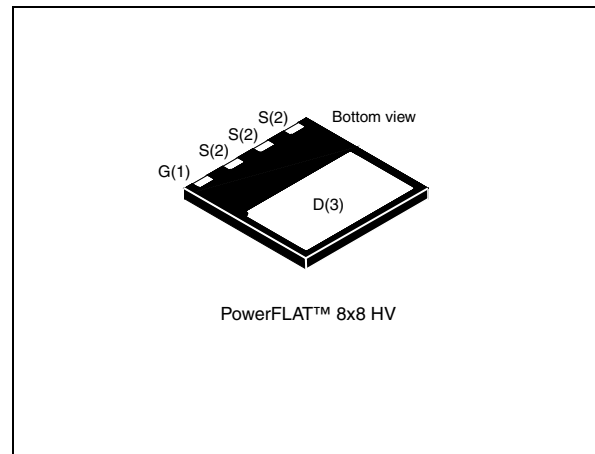


Figure 1. Internal schematic diagram

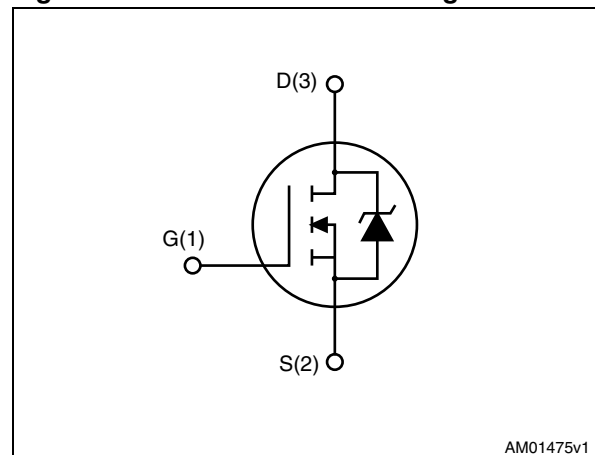


Table 1. Device summary

Order code	Marking	Package	Packaging
STL23NM50N	23NM50N	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	14	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.1	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	56	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	3	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	300	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board of 1 inch^2 , 2oz Cu
4. $I_{SD} \leq 14\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	45	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch^2 FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ °C}$ $V_{GS} = 0$			1 100	μA μA
I_{GSS}	Gate-body leakage current	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$		0.170	0.210	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1330	-	pF
C_{oss}	Output capacitance			84		pF
C_{rss}	Reverse transfer capacitance			4.8		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }400\text{ V}$	-	210	-	pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 17\text{ A}$, $V_{GS} = 10\text{ V}$, <i>(see Figure 14)</i>	-	45	-	nC
Q_{gs}	Gate-source charge			7		nC
Q_{gd}	Gate-drain charge			24		nC
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias=0 Test signal level=20 mV open drain	-	4.6	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 17\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ <i>(see Figure 13)</i>	-	6.6	-	ns
t_r	Rise time			19		ns
$t_{d(off)}$	Turn-off-delay time			71		ns
t_f	Fall time			29		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	286		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	3700		nC
I_{RRM}	Reverse recovery current	(see Figure 18)	-	26		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	350		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	4800		nC
I_{RRM}	Reverse recovery current	(see Figure 18)	-	27		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

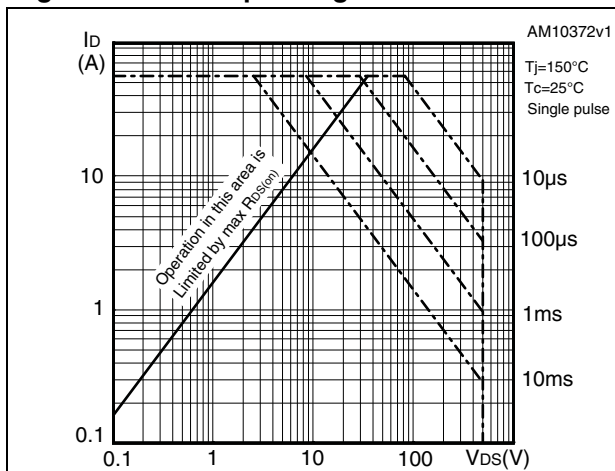


Figure 3. Thermal impedance

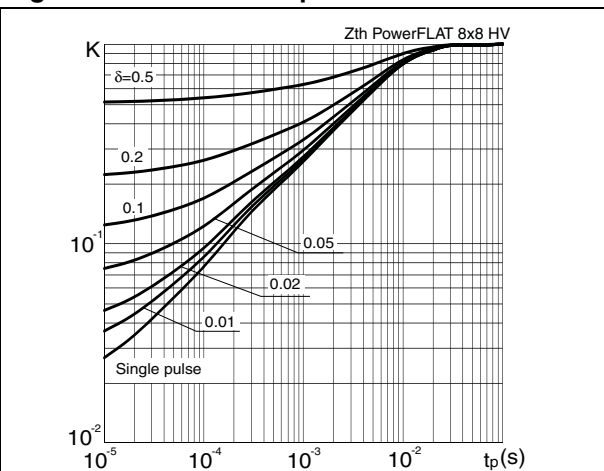


Figure 4. Output characteristics

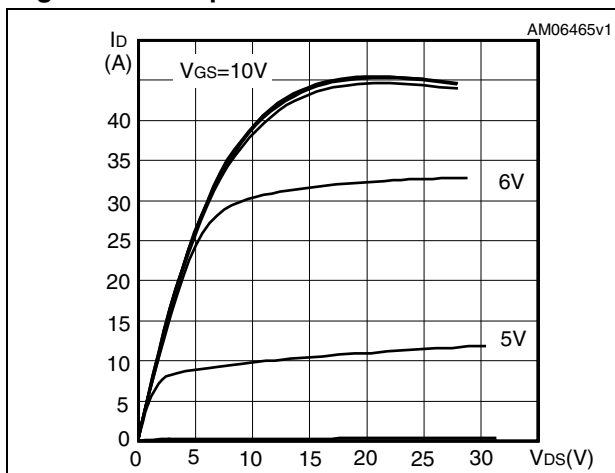


Figure 5. Transfer characteristics

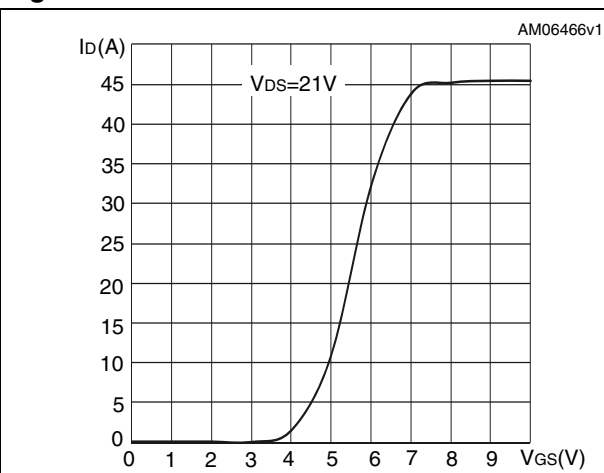


Figure 6. Normalized B_{VDS} vs temperature

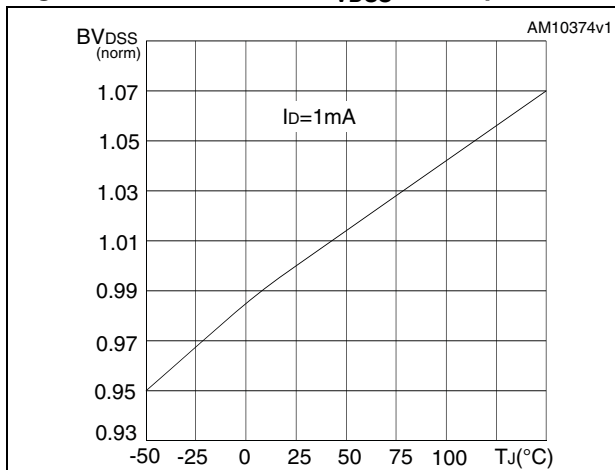


Figure 7. Static drain-source on-resistance

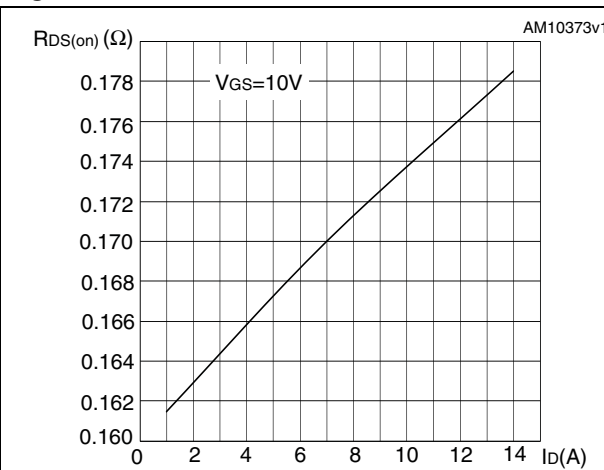


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

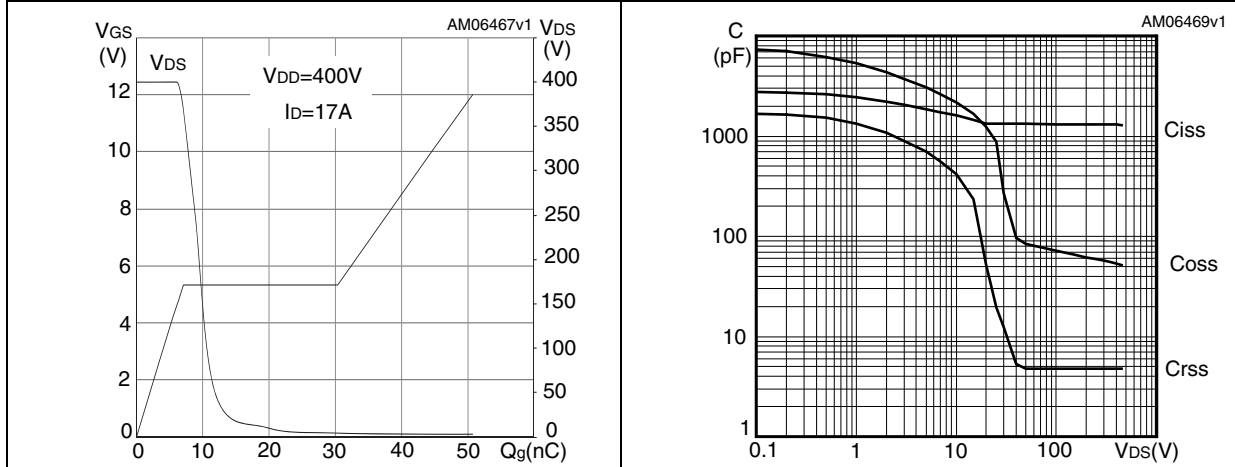


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

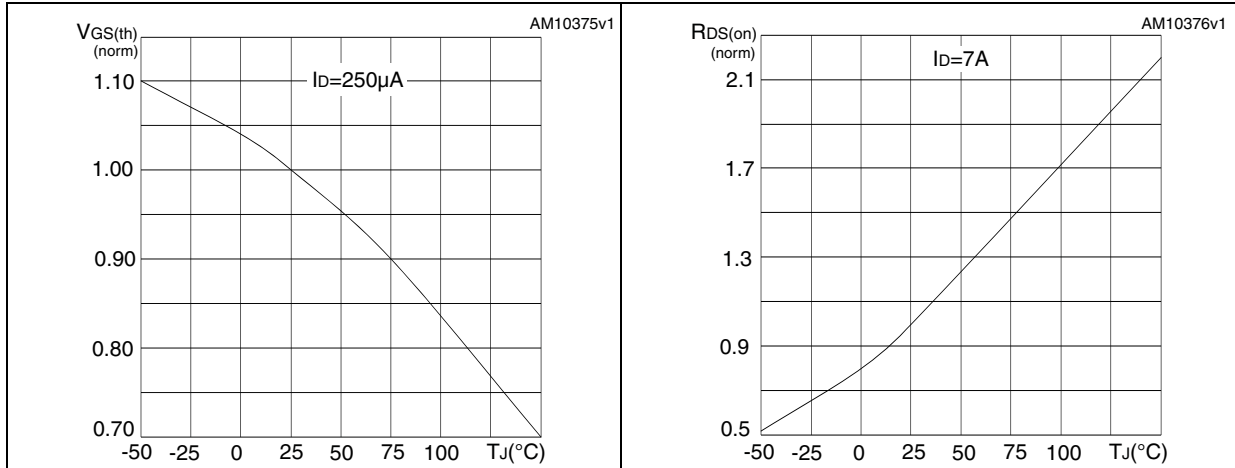
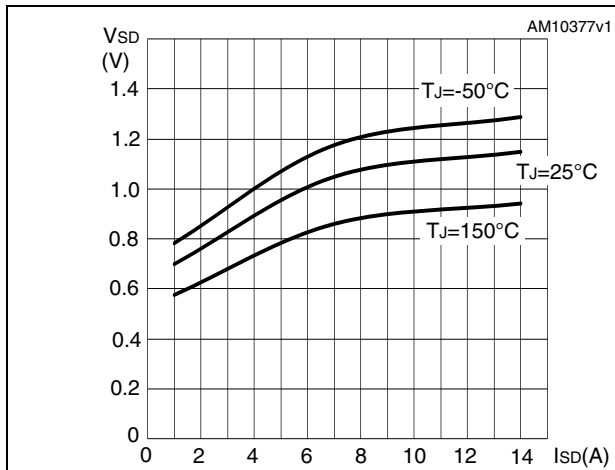


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

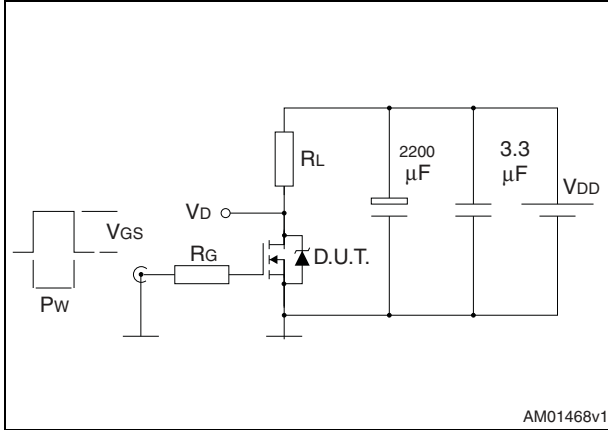


Figure 14. Gate charge test circuit

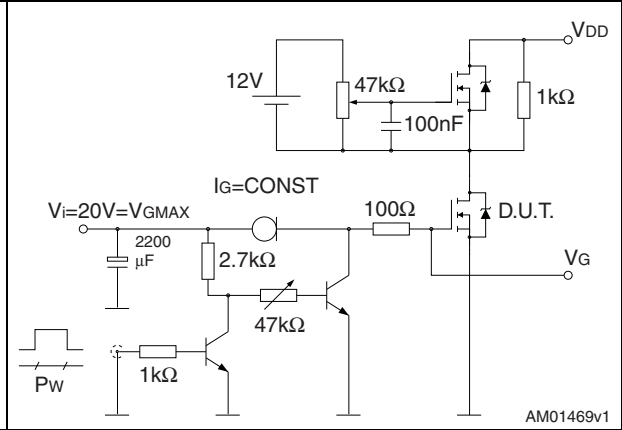


Figure 15. Test circuit for inductive load switching and diode recovery times

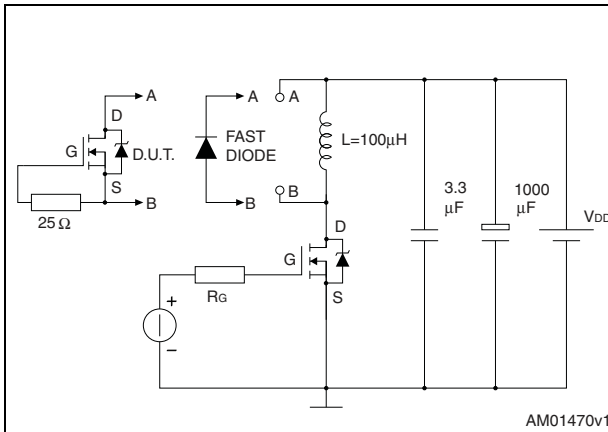


Figure 16. Unclamped inductive load test circuit

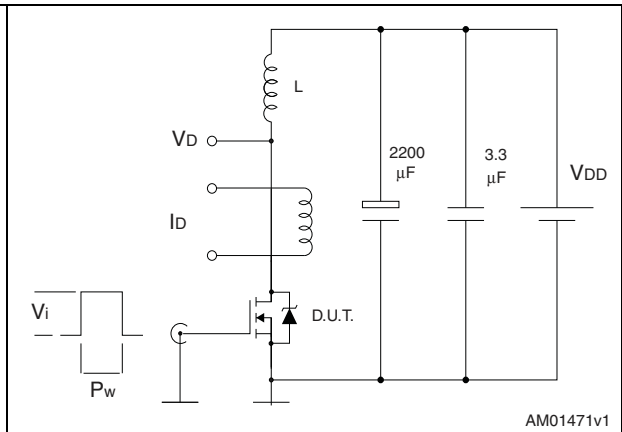


Figure 17. Unclamped inductive waveform

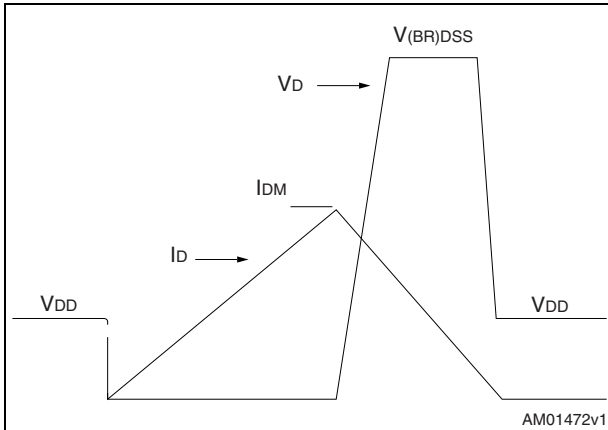
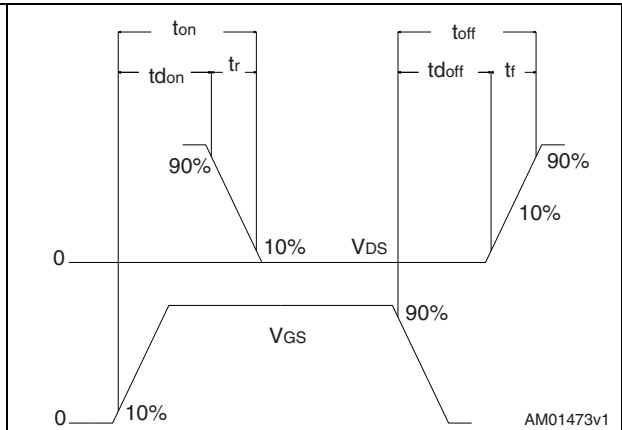


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 19. PowerFLAT™ 8x8 HV drawing mechanical data

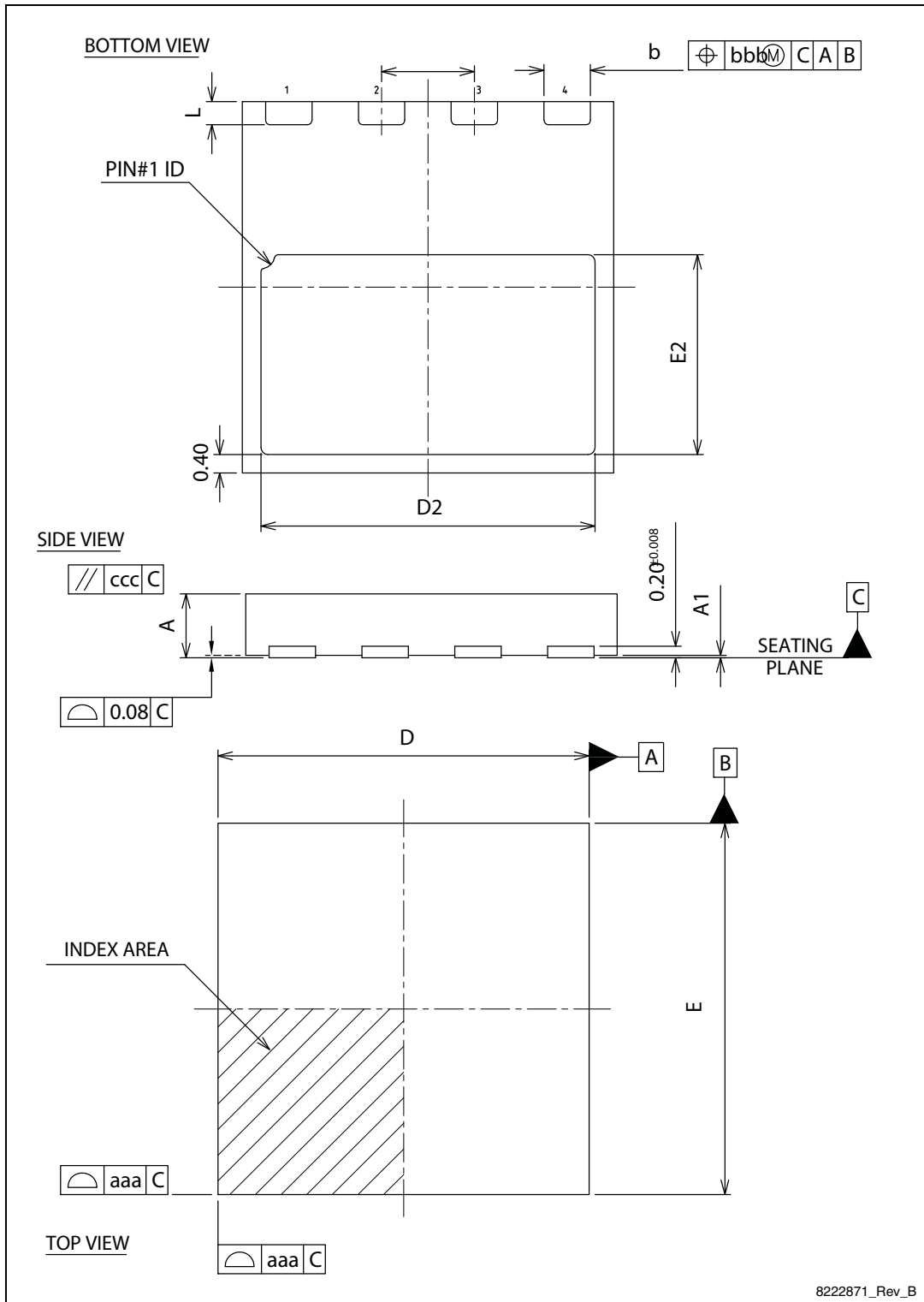
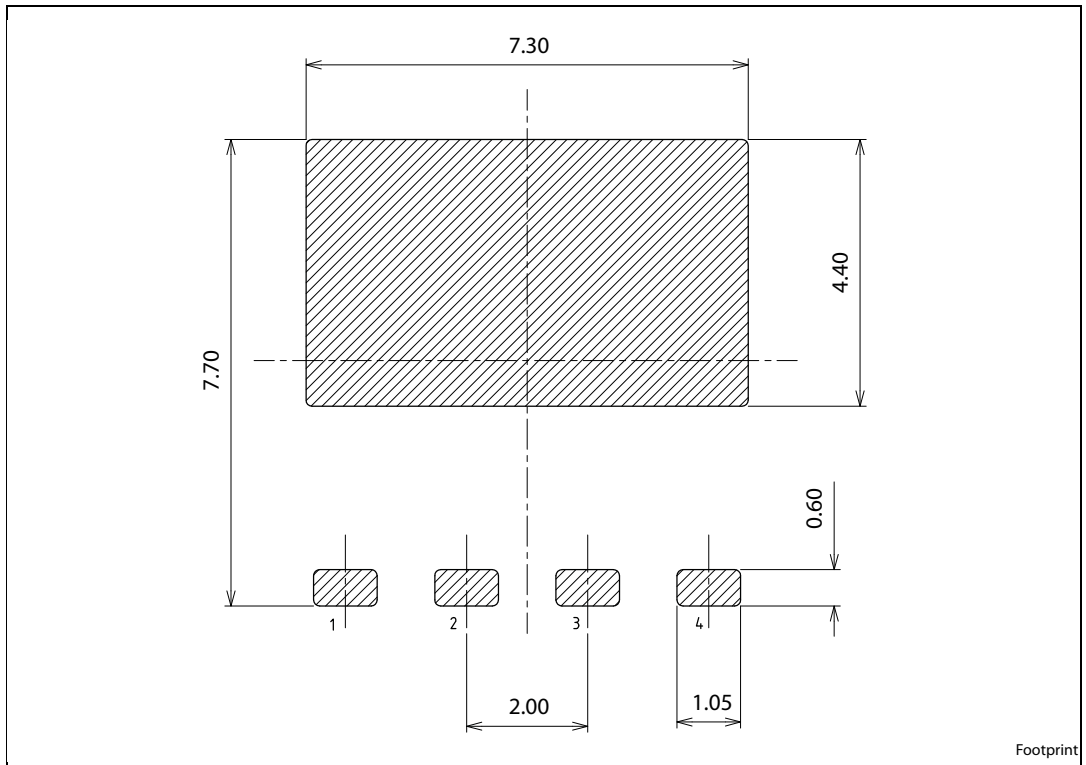


Figure 20. PowerFLAT™ 8x8 HV recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Oct-2011	1	First release.
08-Oct-2012	2	Updated title on the cover page. Updated value for dv/dt on Table 2: Absolute maximum ratings . Document status promoted from preliminary to production data.

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