ST6G3244ME

Level translator for SD, SDIO, mini SD, and micro SD Cards with internal I/O supply and ±15 kV ESD protection

Features

- Supports 60 MHz clock rate
- Supports DDR mode for SD Card™
- Compliant with
  - SD Specification Part 1 Physical Layer Specification 3.00 (SDR12, SDR25, DDR50)
  - SD Specification Part 1 Physical Layer Specification 2.00
- Bi-directional with direction control pin
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- LDO power-down support. When the LDO is powered down, V_{CCB} is pulled to GND via the 130 Ω resistor. When V_{CCB} = 0 V, there is no additional leakage seen on V_{CCA}.
- EMI filtering and signal conditioning
- Supports both 1.8 V and 2.9 V data translation on card side
- Integrated LDO to supply 1.8 V or 2.9 V power for B-side I/Os (pin-selectable); can be used also externally
- Integrated pull-up and pull-down resistors on B-side
- Operating voltage range
  - V_{CCA} = 1.62 V to 1.98 V
  - V_{BAT} = 3.0 V to 5.0 V
- Latch-up performance exceeds 100 mA (JEDEC Standard 78)
- ESD protection for card side (B-port, CD and WP pins)
  - ±8 kV contact discharge (IEC61000-4-2)
  - ±15 kV air-gap discharge (IEC61000-4-2)
- ESD protection for host side (A-side)
  - ±2 kV HBM (JEDEC 22-A114)
  - ±200 V MM (JEDEC 22-A115)

Flip Chip 25

- Operating temperature range –40 °C to +85 °C
- Space-saving Flip Chip 25 package (2 x 2 x 0.605 mm, 0.4 mm bump pitch)
- RoHS compliant, lead-free soldering capable

Applications

- Mobile phones, smartphones
- PDAs
- Cameras
- SD Card readers
- Any device with SD memory card

Table 1. Device summary

Order code	Package	Packing	Package topmark
ST6G3244MEBJR	Flip Chip 25 2 x 2 x 0.605 mm, 0.4 mm bump pitch	Tape and reel (5000 parts per reel)	VKH, VKV

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1 Description

The ST6G3244ME is a dual supply, low voltage 6-bit bi-directional CMOS level translator for SD, mini SD and micro SD Cards. Designed for use as an interface between baseband and memory cards, it achieves high speed operation while maintaining CMOS low-power dissipation.

The A-port is designed to track V_{CCA}. The internal LDO is powered by V_{BAT} and provides a power supply of either 1.8 V or 2.9 V to the B-side I/Os (programmed by the SEL pin). The B-port is designed to track V_{CCB}. The V_{CCB} voltage can be also used externally. When V_{CCB} = 0 V, there is no additional leakage seen on V_{CCA}. All outputs are push-pull type.

This device is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by CMD.dir, DAT0.dir and DAT123.dir inputs.

All inputs are equipped with protection circuits against electrostatic discharge, giving them ±2 kV (on A-side) and ±15 kV (on B-side, CD and WP) ESD and transient excess voltage immunity.

2 Functional description

Figure 1. Pin connections

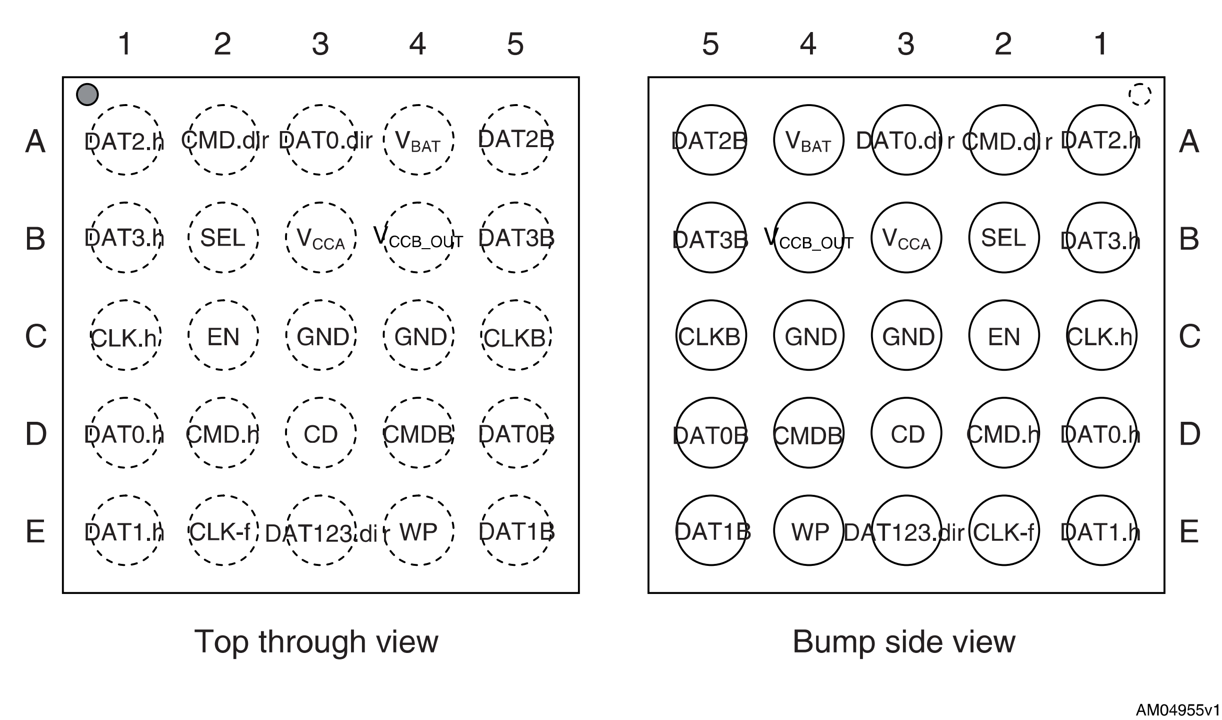


Table 2. Signal names (1)

Pin name	Bump	Type	Side	Description
V_{CCA}	B3	Input	A	Host side positive power supply (1.8 V)
V_{CCB_OUT}	B4	Output	B	Internal supply voltage decoupling, V_{CCB} LDO output
V_{BAT}	A4	Input	A	Battery power supply (3.0 - 5.0 V)
GND	C4	Ground	-	Ground
GND	C3	Ground	-	Ground
EN	C2	Input	A	Enable, active-high
SEL	B2	Input	A	V_{CCB} selection (B-side supply voltage, 1.8 V/2.9 V)
CMD.dir	A2	Input	A	Command direction control
CMD.h	D2	I/O	A	Host side command
CLK.h	C1	Input	A	Host side clock input
CLK-f	E2	Output	A	Clock feedback to host
DAT0.dir	A3	Input	A	DAT0 direction control
DAT0.h	D1	I/O	A	Host side data input/output
DAT123.dir	E3	Input	A	DAT1, DAT2, DAT3 direction control
DAT1.h	E1	I/O	A	Host side data input/output

Table 2. Signal names (continued)[1]

Pin name	Bump	Type	Side	Description
DAT2.h	A1	I/O	A	Host side data input/output
DAT3.h	B1	I/O	A	Host side data input/output
WP	E4	Input to CPU	A	Write protect
CD	D3	Input to CPU	A	Card detect
CMDB	D4	I/O	B	Card side command
CLKB	C5	Output	B	Card side clock output
DAT0B	D5	I/O	B	Card side data input/output
DAT1B	E5	I/O	B	Card side data input/output
DAT2B	A5	I/O	B	Card side data input/output
DAT3B	B5	I/O	B	Card side data input/output

1. Collective names are used for groups of pins in the datasheet:
   *.dir = CMD.dir, DAT0.dir, DAT123.dir
   *.h = CMD.h, CLK.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h
   *B = CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B
   V_{IA} = all A-side input pins.

Table 3. Direction control

Command signals				Direction of A-side signals[1]					Direction of B-side signals[1]			
EN	CMD.dir	DAT0.dir	DAT123.dir	CMD.h	CLK.h	CLK-f	DAT0.h	DAT1.h DAT2.h DAT3.h	CMDB	CLKB	DAT0B	DAT1.B DAT2.B DAT3.B
H	H	X	X	IN	IN	OUT	X	X	OUT	OUT	X	X
H	L	X	X	OUT	IN	OUT	X	X	IN	OUT	X	X
H	X	H	X	X	IN	OUT	IN	X	X	OUT	OUT	X
H	X	L	X	X	IN	OUT	OUT	X	X	OUT	IN	X
H	X	X	H	X	IN	OUT	X	IN	X	OUT	X	OUT
H	X	X	L	X	IN	OUT	X	OUT	X	OUT	X	IN
L	X	X	X	X	X	Z	X	X	(2)	Z	(2)	(2)

1. When the direction of the A-side signal is INPUT, the host CPU WRITES to the SD Card (i.e. the direction of the B-side signal is OUTPUT).
   When the direction of the A-side signal is OUTPUT, the host CPU READS the SD Card (i.e. the direction of the B-side signal is INPUT).
2. Level of the B-side signals when EN = L is defined by the internal resistors as listed in *Table 7*.

Note: During application design it has to be considered that the level shifter device needs some time to change the direction after a change of the .dir signal level. Valid data on the input of the corresponding channel can then start after a turn-around time, see the t_{TA} *specification in Table 12.*

Figure 2. Block diagram

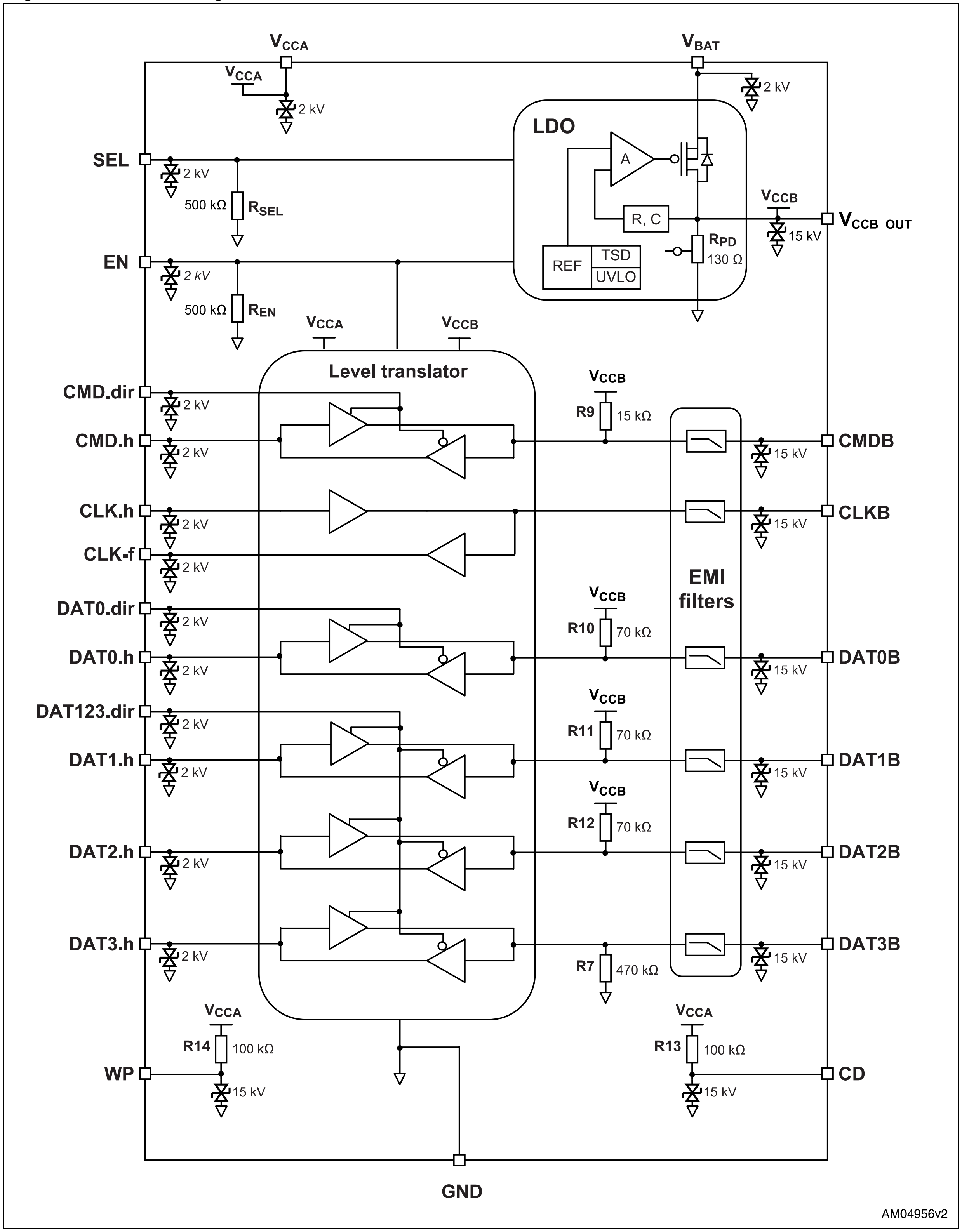
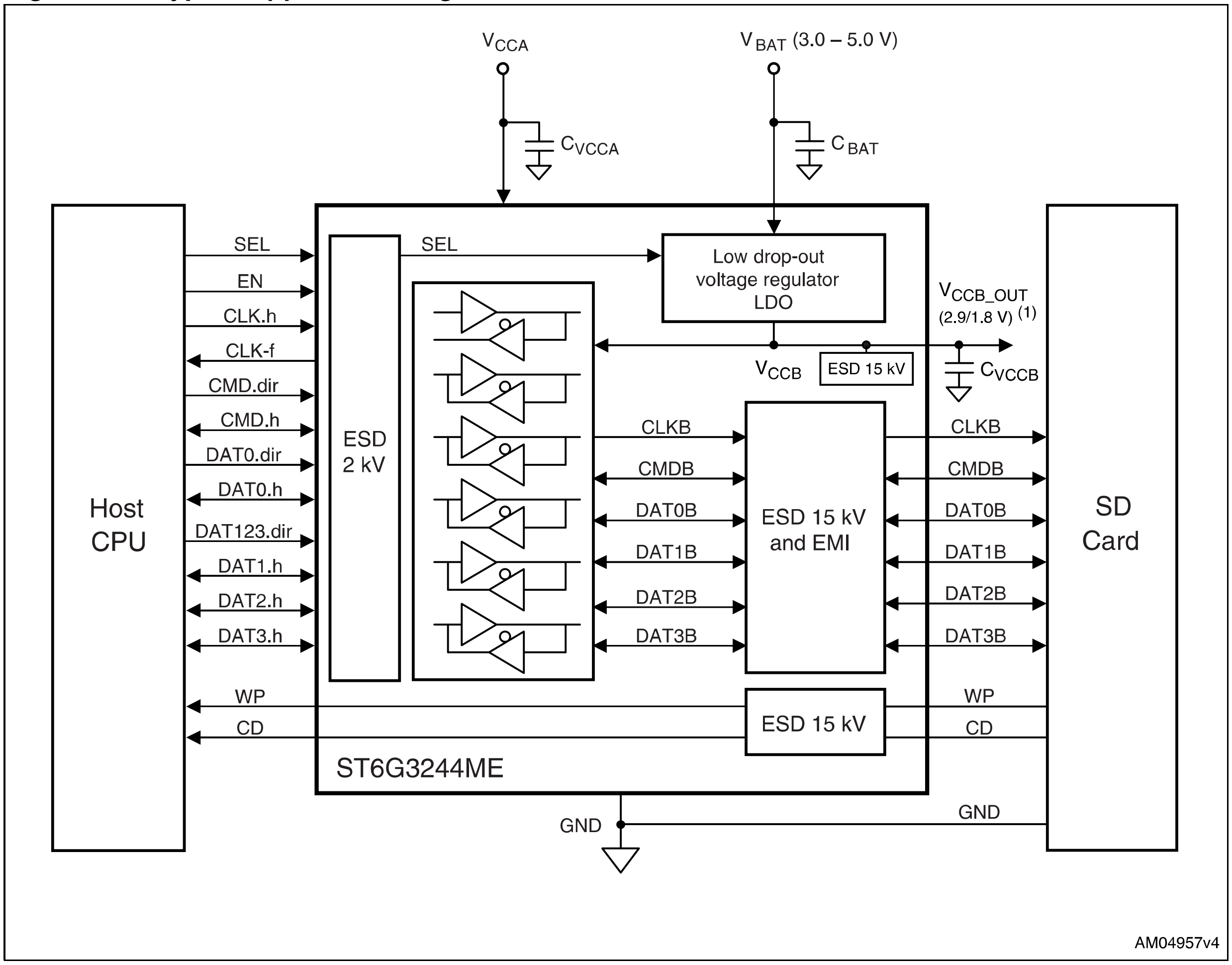


Figure 3. Typical application diagram



1. Can be used externally, however, note that it follows V_{CCB} value that is switched between 2.9 and 1.8 V by the SEL pin.

3 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

<table>
<tr><th>Symbol</th><th colspan="3">Parameter</th><th>Value</th><th>Unit</th></tr>
<tr><td>T_{JMAX}</td><td colspan="3">Maximum junction temperature</td><td>150</td><td>°C</td></tr>
<tr><td>$R_{TH(J-A)}$ (1)</td><td colspan="3">Thermal resistance from junction to ambient
(board: epoxy FR4, $e_{(CU)}$ = 40 µm, 4 layers)</td><td>64</td><td>°C/W</td></tr>
<tr><td>P_{DMAX}</td><td colspan="3">Maximum power dissipation:
$P_{DMAX} = (T_{JMAX} - T_{AMAX})/R_{TH(J-A)}$</td><td>1</td><td>W</td></tr>
<tr><td>T_{STG}</td><td colspan="3">Storage temperature range</td><td>–55 to 150</td><td>°C</td></tr>
<tr><td>V_{CCA}</td><td colspan="3">Power supply</td><td>–0.3 to 4.6</td><td>V</td></tr>
<tr><td>V_{BAT}</td><td colspan="3">Battery power supply</td><td>–0.3 to 5.5</td><td>V</td></tr>
<tr><td rowspan="3">V_{IO}</td><td colspan="3">CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B</td><td>–0.3 to V_{CCB} + 0.3</td><td rowspan="3">V</td></tr>
<tr><td colspan="3">V_{CCA}, SEL, EN</td><td>–0.3 to 4.6</td></tr>
<tr><td colspan="3">CMD.dir, CMD.h, CLK.h, CLK-f, DAT0.dir, DAT0.h, DAT123.dir, DAT1.h, DAT2.h, DAT3.h, WP, CD</td><td>–0.3 to V_{CCA} + 0.3</td></tr>
<tr><td rowspan="4">ESD</td><td rowspan="2">A-side (host CPU), all pins:
V_{CCA}, EN, SEL, DAT123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, DAT0.dir, DAT0.h, DAT1.h, DAT2.h, DAT3.h, V_{BAT}</td><td>HBM</td><td>JEDEC 22-A114</td><td>±2</td><td>kV</td></tr>
<tr><td>MM</td><td>JEDEC 22-A115</td><td>±200</td><td>V</td></tr>
<tr><td rowspan="2">B-side (SD Card), external pins:
CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B, WP, CD, V_{CCB_OUT}</td><td>Air discharge</td><td>IEC61000-4-2</td><td>±15</td><td>kV</td></tr>
<tr><td>Contact discharge</td><td>IEC61000-4-2</td><td>±8</td><td>kV</td></tr>
</table>

1. The thermal resistance depends on the printed circuit board layout. To dissipate the heat efficiently away from the Flip-Chip bumps, it is recommended to make the copper planes as large as possible and consider using thermal vias.

4 DC and AC parameters

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CCA}	Power supply		1.62	1.8	1.98	V
V_{BAT}	Battery power supply		3.0		5.0	V
C_{BAT}	External battery capacitance	Ceramic capacitor	1.0	2.2	2.8	µF
C_{VCCA}	V_{CCA} decoupling capacitor	Ceramic capacitor	0.1			µF
C_{VCCB}	Internal supply voltage (V_{CCB}) decoupling capacitor	Ceramic capacitor	1.0	2.2	2.8	µF
T_A	Ambient operating temperature		–40	25	85	°C
T_J	Junction operating temperature		–40	25	125	°C
P_D	Maximum power dissipation	$P_D = (T_J - T_A)/R_{TH(J-A)}$			625	mW
V_{IO_B}	I/O voltage on external pins (without WP and CD) - B-side	CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B	0		V_{CCB}	V
V_{IO_A}	I/O voltage on internal pins (includes WP and CD) - A-side	EN, SEL, WP, CD, DAT123.dir, CMD.dir, CMD.h, CLK.h, CLK-f, DAT0.dir, DAT0.h, DAT1.h, DAT2.h, DAT3.h	0		V_{CCA}	V

Table 6. Current levels under recommended operating conditions (T_A = –40 °C to 85 °C)

Symbol	Parameter	Test conditions(1)		Min.	Typ.	Max.	Unit
I_{Q_OFF}	Quiescent current consumption I_{CCA_OFF}	V_{EN} = 0.4 V, V_{BAT} = 3.4 V, V_{CCA} = 1.98 V *.dir, *B = 0 V, WP = CD = V_{CCA} All other pins floating				1	µA
	Quiescent current consumption I_{BAT_OFF}					1	µA
I_{Q_ON}	Quiescent current consumption (Ground pin current) $I_{BAT} + I_{CCA}$	*.dir = 0 V, V_{BAT} = 3.4 V $V_{EN} = V_{CCA} = V_{CLK.h}$ = 1.98 V All other pins floating	I_{OUT} = 100 µA			150(2)	µA
			I_{OUT} = 50 mA			250(2)	
I_{CCA_ON}	Quiescent current on V_{CCA}	$V_{EN} = V_{CCA}$ = 1.92 V, V_{BAT} = 3.4 V, *.dir = V_{CCA}, V_{IA} = *.h = V_{CCA}			3	10	µA

1. Collective names for groups of pins:
   *.dir = CMD.dir, DAT0.dir, DAT123.dir
   *.h = CMD.h, CLK.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h
   *B = CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B
   V_{IA} = all A-side input pins.
2. Guaranteed by design.

5 Passive integration and low-pass EMI filter

Figure 4. Circuit diagram of ST6G3244ME (without LDO)

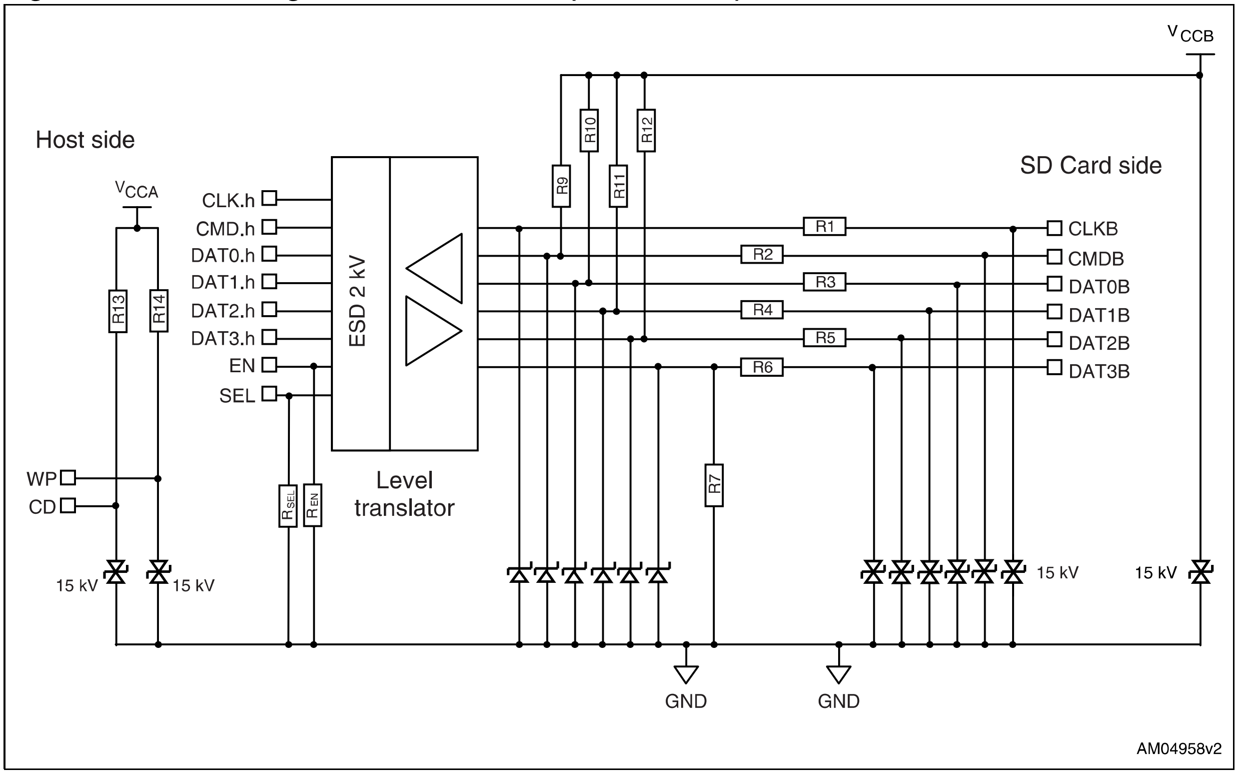


Table 7. Components

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
C_{IN-A}	Input capacitance for A-side	V_{BAT} = 3.4 V, *.dir = V_{EN} = V_{CCA} f = 1 MHz, V_{DC} = 0 V ± 30 mV, V_{AC} = 30 mV		5	10	pF
C_{IN-B}	Input capacitance for B-side	V_{BAT} = 3.4 V, *.dir = 0 V, V_{EN} = V_{CCA} f = 1 MHz, V_{DC} = 0 V ± 30 mV, V_{AC} = 30 mV		24	28	pF
R1, R2, R3, R4, R5, R6[2]	EMIF resistors	T_J = 25 °C	32	40	48	Ω
R10, R11, R12	DAT0B, DAT1B, DAT2B pull-up resistors	T_J = 25 °C	49	70	91	kΩ
R9	CMDB pull-up resistor	T_J = 25 °C	10.5	15	19.5	kΩ
R7	DAT3B pull-down resistor	T_J = 25 °C	329	470	611	kΩ
R13	CD pull-up resistor	T_J = 25 °C	70	100	130	kΩ
R14	WP pull-up resistor	T_J = 25 °C	70	100	130	kΩ
R_{PD}	LDO resistor	T_J = 25 °C	90	130	170	Ω
R_{EN}	EN pull-down resistor	T_J = 25 °C		500		kΩ
R_{SEL}	SEL pull-down resistor	T_J = 25 °C		500		kΩ

1. See Note 1 on page 7 for definition of collective names of pins, for example *.dir.
2. These values are guaranteed by design and statistical process control.

Table 8. EMI filter attenuation

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IL_{0-200M}	Filter attenuation[1]	Frequency range: 0 Hz to 200 MHz	6	-	-	dB
$IL_{401-800M}$		Frequency range: 401 MHz to 800 MHz	10	-	-	
$IL_{801-2500M}$		Frequency range: 801 MHz to 2.5 GHz	20	-	-	
$IL_{2600-6000M}$		Frequency range: 2.6 GHz to 6 GHz	30	-	-	

1. Guaranteed by design.

6 Data transmission

All values in the tables below are guaranteed across the operating temperature and voltage range unless otherwise specified.

Table 9. DC voltage levels on host CPU side (T_A = –40 °C to 85 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IHA}	High level input voltage		0.65 V_{CCA}	V_{CCA}		V
V_{ILA}	Low level input voltage			0	0.35 V_{CCA}	V
V_{OHA}	High level output voltage	I_{OH} = –6 mA, V_{CCA} = 1.62 V	V_{CCA} – 0.45	V_{CCA}		V
V_{OLA}	Low level output voltage	I_{OL} = 7 mA, V_{CCA} = 1.62 V		0	0.45	V

Table 10. DC voltage levels on SD Card side (T_A = –40 °C to 85 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IHB}	High level input voltage		0.7 V_{CCB}	V_{CCB}		V
V_{ILB}	Low level input voltage			0	0.3 V_{CCB}	V
V_{OHB}	High level output voltage	I_{OH} = –4 mA	0.8 V_{CCB}	V_{CCB}		V
V_{OLB}	Low level output voltage	I_{OL} = 4 mA		0	0.2 V_{CCB}	V

Table 11. Leakage and short-circuit currents

Symbol	Parameter	Test condition[1]	Min.	Typ.	Max.	Unit
I_{LH}	Leakage current on host side pins	V_{SEL} = 0 V, V_{EN} = *.dir = V_{CCA} = 1.98 V V_{IA} = V_{CCA} or 0 V, V_{BAT} = 3.4 V			5	µA
I_{LSD}	Leakage current on SD Card side pins	V_{SEL} = 0 V, V_{BAT} = 3.4 V, $V_{CLK.h}$ = V_{CCA} V_{CMD} = V_{DAT0} = V_{DAT1} = V_{DAT2} = V_{CCB} V_{DAT3} = *.dir = 0 V			5	µA
I_{SCH}	Short-circuit current on host side pins	SD Card input = H, host = 0 V SD Card input = 0 V, host = V_{CCA} = 1.8 V *.dir = 0 V, V_{BAT} = 3.4 V, T_J = 25 °C		25		mA
I_{SCSD}	Short-circuit current on SD Card side pins	Host input = H, SD Card = 0 V Host input = L, SD Card = V_{CCB} = 2.9 V, T_J = 25 °C, *.dir = V_{CCA} = 1.8 V, V_{BAT} = 3.4 V	25		70	mA
		Host input = H, SD Card = 0 V Host input = L, SD Card = V_{CCB} = 1.8 V, T_J = 25 °C, *.dir = V_{CCA} = 1.8 V, V_{BAT} = 3.4 V	25		70	

1. Collective names for groups of pins:
*.dir = CMD.dir, DAT0.dir, DAT123.dir
*.h = CMD.h, CLK.h, DAT0.h, DAT1.h, DAT2.h, DAT3.h
*B = CMDB, CLKB, DAT0B, DAT1B, DAT2B, DAT3B
V_{IA} = all A-side input pins.

Figure 5. Symbol definitions of t_{PLH}, t_{PHL}, t_r and t_f for AC characteristics

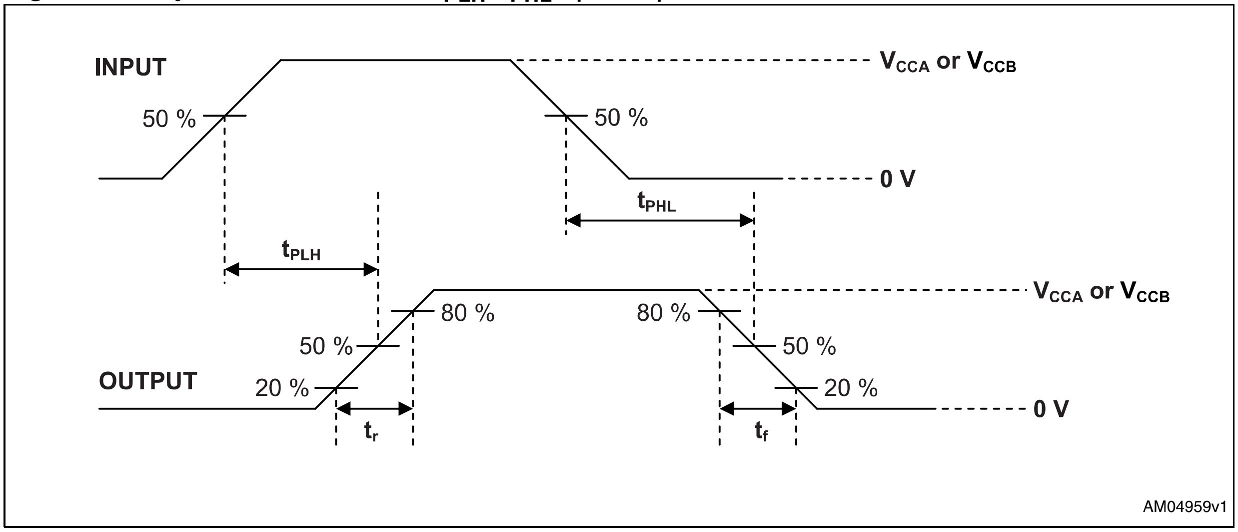


Table 12. AC characteristics (T_A = –40 °C to 85 °C)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
t_{PHL}	Propagation delay HL from host to SD	See *Section 6.1*	V_{CCB} = 1.8 V		3.2	7	ns
			V_{CCB} = 2.9 V		3.2	5	
t_{PLH}	Propagation delay LH from host to SD	See *Section 6.1*	V_{CCB} = 1.8 V		3.2	7	ns
			V_{CCB} = 2.9 V		3.2	5	
t_{PHL}	Propagation delay HL from SD to host	See *Section 6.2*	V_{CCB} = 1.8 V		3.0	7	ns
			V_{CCB} = 2.9 V		2.8	5	
t_{PLH}	Propagation delay LH from SD to host	See *Section 6.2*	V_{CCB} = 1.8 V		3.0	7	ns
			V_{CCB} = 2.9 V		2.8	5	
t_r	Rise time from host to SD	See *Section 6.1*	V_{CCB} = 1.8 V		2.0	4	ns
			V_{CCB} = 2.9 V		2.0	4	
	Rise time from SD to host	See *Section 6.2*	V_{CCB} = 1.8 V		2.0	4	
			V_{CCB} = 2.9 V		2.0	4	
t_f	Fall time from host to SD	See *Section 6.1*	V_{CCB} = 1.8 V		2.0	4	ns
			V_{CCB} = 2.9 V		2.0	4	
	Fall time from SD to host	See *Section 6.2*	V_{CCB} = 1.8 V		2.0	4	
			V_{CCB} = 2.9 V		2.0	4	
t_{TA}	Turn-around time (direction switch response, for all channels)(1)		V_{CCB} = 1.8 V or 2.9 V, C_L = 15 pF		7.5	12	ns
t_{SKEW}	Delay differences from host to SD	See *Section 6.1*	See *Section 6.3*	–0.5	0	0.5	ns
$t_{CH2CH\text{-}SKEW}$	Channel-to-channel skew			–0.5	0	0.5	ns
$t_{SKEW.f}$	CLK-f to CMD, DAT delay (valid for PCB trace lengths from 20 mm to 100 mm)	See *Section 6.2*	See *Section 6.4*	0.3		1.2	ns
t_{P_CLKF}	Propagation delay from CLK feedback	See *Section 6.2*	V_{CCB} = 1.8 V		5.7	13.5	ns
			V_{CCB} = 2.9 V		5.5	9.5	

Table 12. AC characteristics (T_A = –40 °C to 85 °C) (continued)

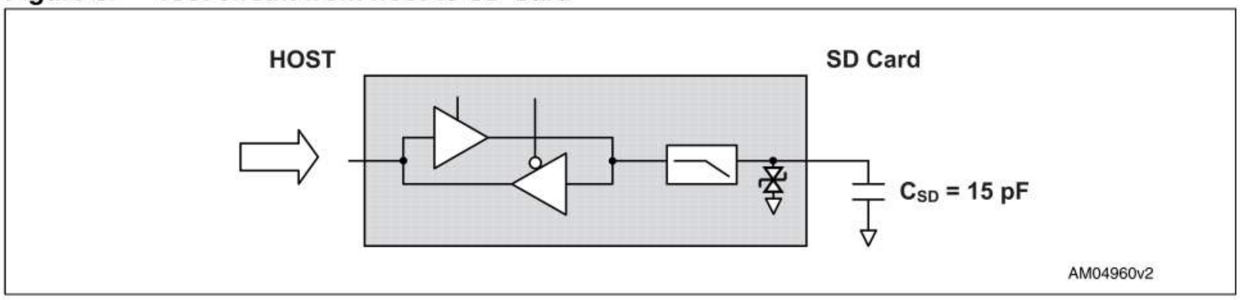
Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
t_{r_CLKF}	Rise time for CLK feedback	See Section 6.2	V_{CCB} = 1.8 V		1.0	3	ns
			V_{CCB} = 2.9 V		1.0	3	
t_{f_CLKF}	Fall time for CLK feedback	See Section 6.2	V_{CCB} = 1.8 V		1.0	3	ns
			V_{CCB} = 2.9 V		1.0	3	
f_{MAX}	Clock rate					60	MHz
	Data rate					120	Mbps

1. The time after the .dir signal transition that the device needs to switch direction, after that it is ready to accept valid data on the switched input.

6.1 Test circuit from host to SD Card

The test circuit from the host to the SD Card is shown in *Figure 6*. Timings are measured for the whole line cell (translator + EMI + ESD) on an external load C_{SD} = 15 pF (board capacitance 5 pF + SD Card capacitance 10 pF).

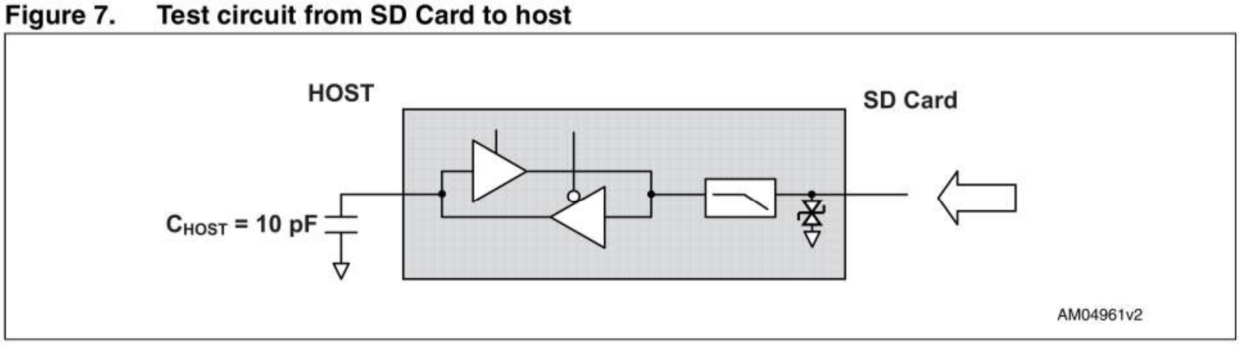
Figure 6. Test circuit from host to SD Card



6.2 Test circuit from SD Card to host

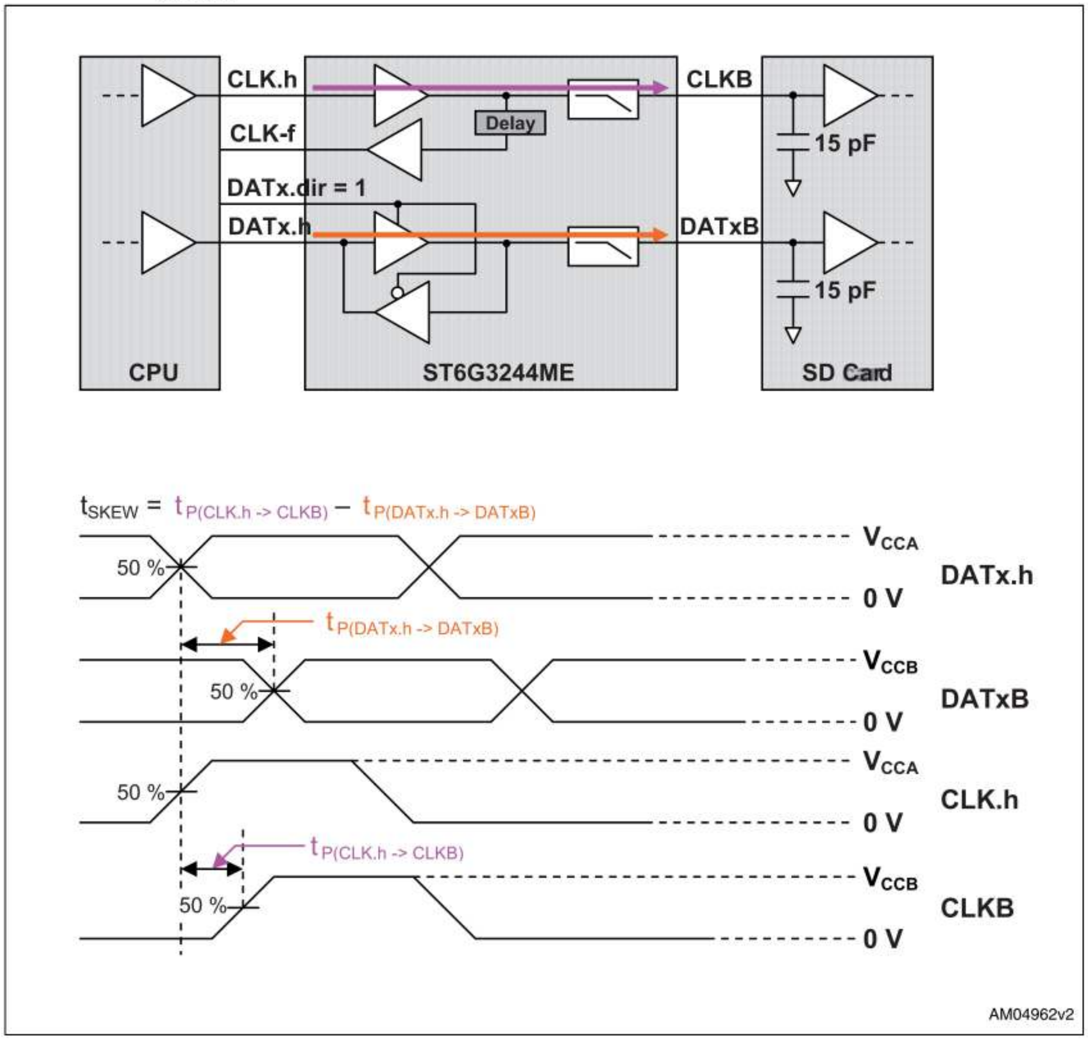
The test circuit from the SD Card to the host is shown in *Figure 7*. Timings are measured for the whole line cell (translator + EMI + ESD) on an external load C_{HOST} = 10 pF (board capacitance + host capacitance).

Figure 7. Test circuit from SD Card to host



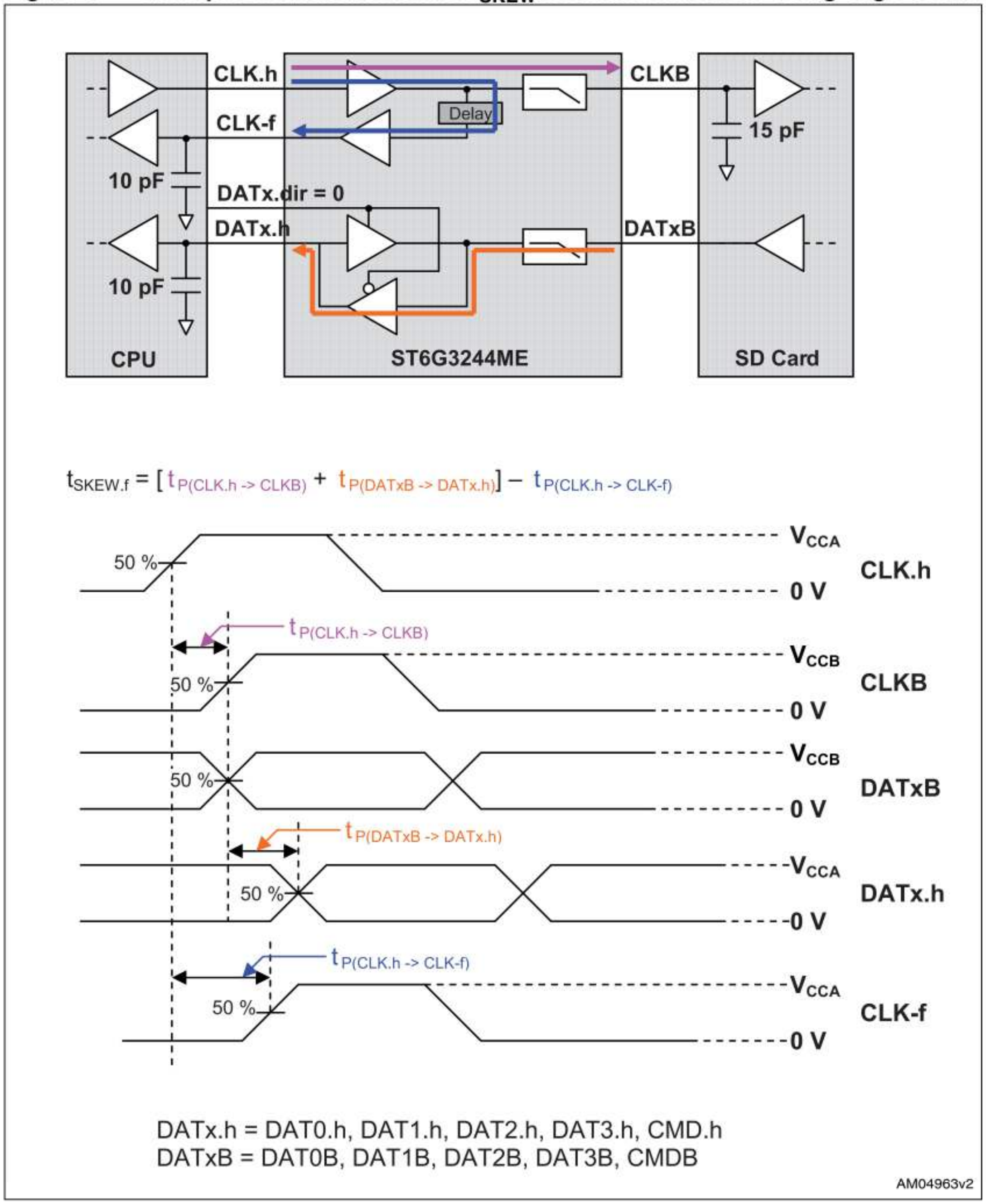
6.3 Measurement of t_{SKEW} (SD Card to host) from rising edge CLK.h

Figure 8. Example of measurement of t_{SKEW} (SD Card to host) from rising edge CLK.h



6.4 Measurement of $t_{SKEW.f}$ (read mode) from rising edge CLK.h

Figure 9. Example of measurement of t_{SKEW} for read mode from rising edge CLK.h



7 Low drop-out voltage regulator

Figure 10. Low drop-out voltage regulator

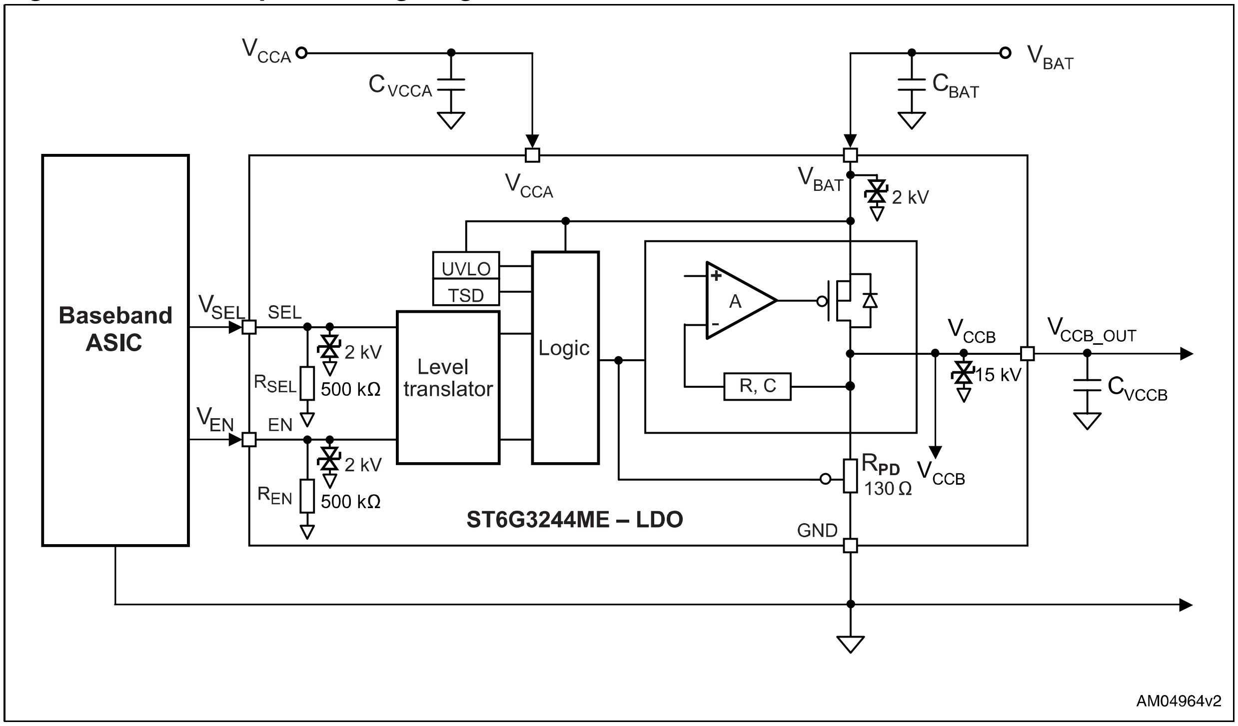


Table 13. V_{CCB} selection (B-side power supply voltage), EN pin control

EN	SEL	V_{CCB}(1) (V)
0	x	0(2)
1	0	2.9
1	1	1.8

1. V_{CCB} is an internal B-side I/O power supply, tied to the V_{CCB_OUT} pin for external decoupling capacitor. V_{CCB} supply voltage can also be used externally.
2. Pulled down to GND by R_{PD}. When V_{CCB} = 0 V, no additional leakage is seen on V_{CCA}.

Table 14. LDO static parameters (V_{EN} = V_{CCA} unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{CCB_OUT}	Regulated output voltage (V_{CCB})	V_{BAT} = 3 to 5 V, SEL = 0 I_{OUT} = 0.1 to 50 mA, T_J = –40 to 125 °C		2.75	2.90	3.05	V
		V_{BAT} = 3 to 5 V, SEL = 1 I_{OUT} = 0.1 to 50 mA, T_J = –40 to 125 °C		1.71	1.8	1.89	
V_{DO}	Drop-out voltage	V_{CCB_OUT} (nom) – 100 mV T_J = –40 to 85 °C SEL = 0	I_{OUT} = 50 mA		25	40	mV
I_{OUT}	V_{CCB_OUT} output current					50	mA
TSD	Thermal shutdown temperature	V_{BAT} = 3.4 V	Shutdown (temp. ↑)		150		°C
			Reset (temp. ↓)		130		
			Hysteresis		20		
UVLO	Undervoltage lockout	T_J = –40 to 125 °C	Shutdown (V_{BAT} ↓)	2.3	2.5	2.7	V
			Reset (V_{BAT} ↑)	2.35	2.55	2.75	V
			Hysteresis		50		mV

*Note: Level translator deactivated, *.dir = 0, CLK.h = V_{CCA}, all other pins floating.*

Table 15. LDO dynamic parameters (V_{EN} = V_{CCA} unless otherwise specified)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
PSRR	Power supply rejection ratio	V_{BAT} = 3.4 V I_{OUT} = 50 mA T_J = 25 °C C_{VCCB} = 2.2 µF, ESR = 5 mΩ	f = 1 kHz		40		dB
			f = 10 kHz		30		
t_{START}	Settling time	V_{CCB_OUT} ↑ 95% nom., V_{BAT} = 5 V, I_{OUT} = 50 mA, T_J = –40 °C to 125 °C, C_{VCCB} = 1 µF, enable L →H, SEL = 0			30	100	µs
		V_{CCB_OUT} ↑ 95% nom., V_{BAT} = 5 V, I_{OUT} = 50 mA, T_J = –40 °C to 125 °C, C_{VCCB} = 1 µF, enable L →H, SEL = 1			30	100	
t_{STOP}	Discharge time	V_{CCB_OUT} ↓ 10% nom., V_{BAT} = 3.4 V, I_{OUT} = 1 mA, T_J = 25 °C, C_{VCCB} = 1 µF, enable H →L, SEL = 0			0.6	1	ms
		V_{CCB_OUT} ↓ 10% nom., V_{BAT} = 3.4 V, I_{OUT} = 1 mA, T_J = 25 °C, C_{VCCB} = 1 µF, enable H →L, SEL = 1			0.6	1	

8 SD Card specification compliance

The ST6G3244ME is designed to be compliant with SD Card specifications. The reference standards used include:

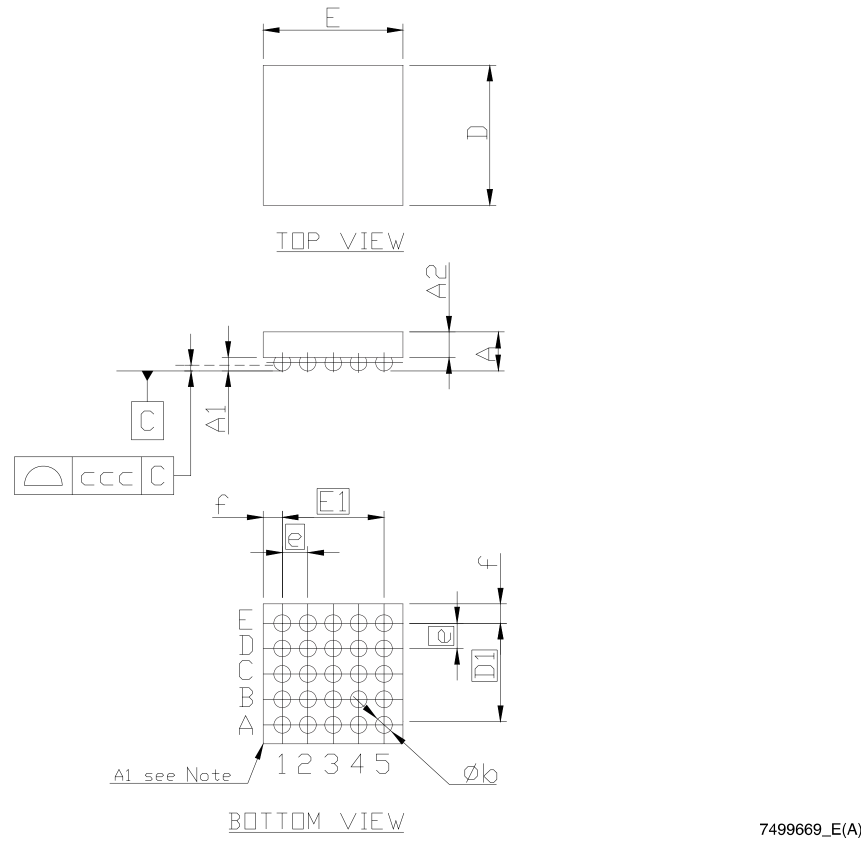
- SD Card Specification v3.00 (SDR12, SDR25, DDR50)
- SD Card Specification v2.00

The clock and data channels are designed to meet a 60 MHz clock rate and 120 Mbps data rate respectively to support both SDR and DDR modes.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 11. Package outline for Flip Chip 25 (2 mm x 2 mm x 0.605 mm, 0.4 mm pitch)

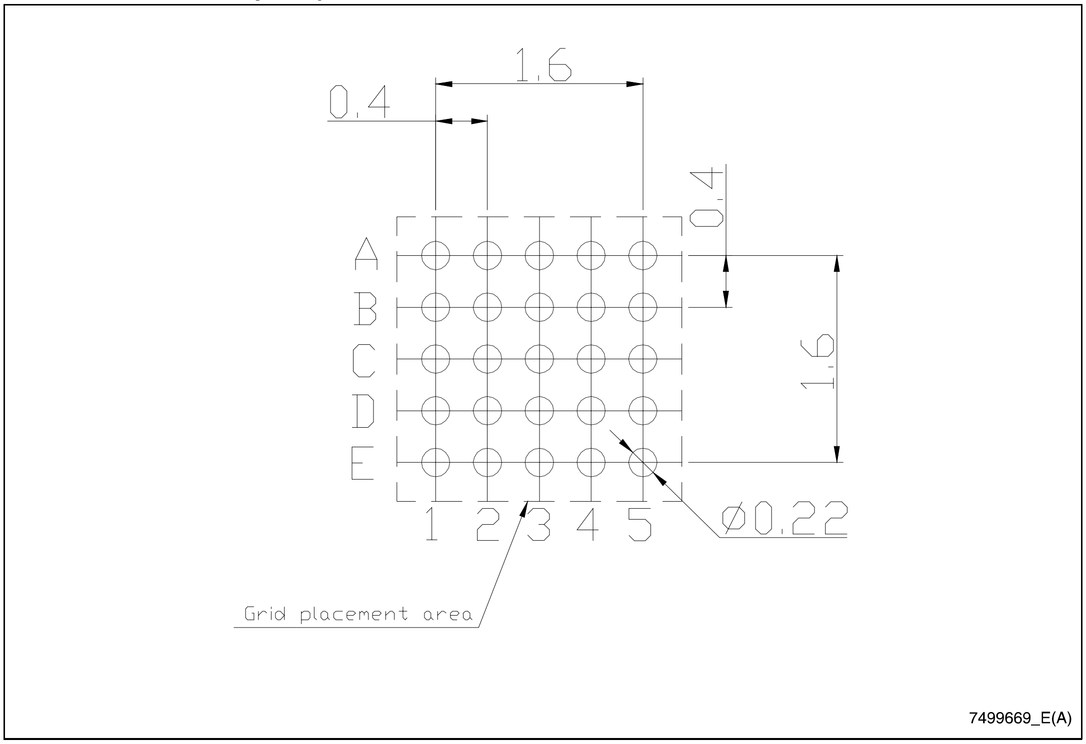


Note: The terminal A1 is on the top side of the package identified by a circular dot - typically 0.5 mm in diameter.

Table 16. Package mechanical data for Flip Chip 25 (2 mm x 2 mm x 0.605 mm, 0.4 mm pitch)

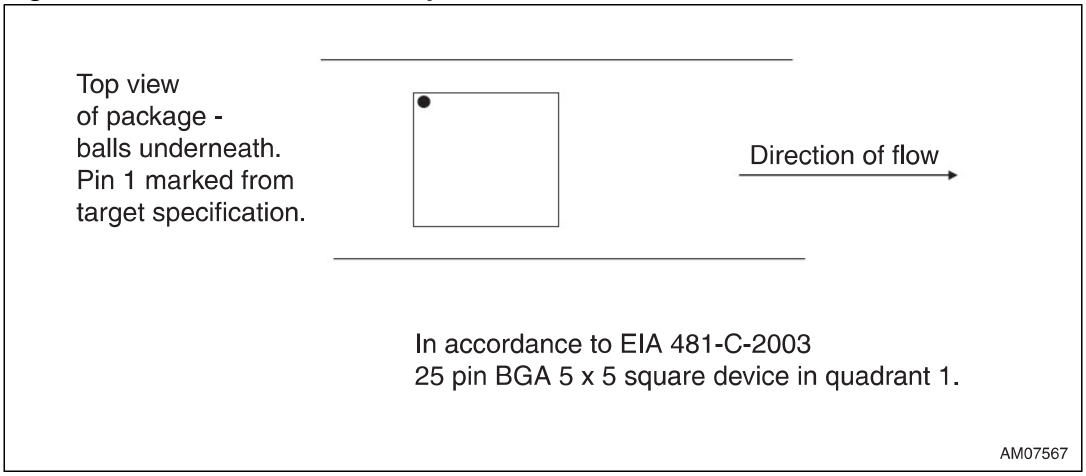
Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.560	0.605	0.650
A1	0.180	0.205	0.230
A2	0.380	0.400	0.420
b	0.230	0.255	0.280
D	1.985	2.00	2.015
D1	1.59	1.60	1.61
E	1.985	2.00	2.015
E1	1.59	1.60	1.61
e	0.36	0.40	0.44
f	0.190	0.200	0.210
ccc			0.05

Figure 12. Footprint recommendation for Flip Chip 25 (2 mm x 2 mm x 0.605 mm, 0.4 mm pitch)



10 Tape and reel information

Figure 13. Pin 1 orientation in tape



11 Revision history

Table 17. Document revision history

Date	Revision	Changes
25-Aug-2011	1	Initial release.
08-Nov-2011	2	Removed label “custom data”, updated *Features*, *Applications*, *Table 1* updated and moved from *Section 11 Package marking* on page 26 to page 1, updated *Section 1: Description*, *Section 2: Functional description*, *Table 2*, *Table 3* to *Table 7*, *Table 10* to *Table 12*, *Table 14*, *Figure 8*, *Figure 9*, *Figure 13*, removed *Section 11 Package marking*, minor text corrections throughout document.

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