

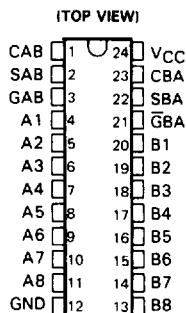
SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1983 - REVISED JANUARY 1990

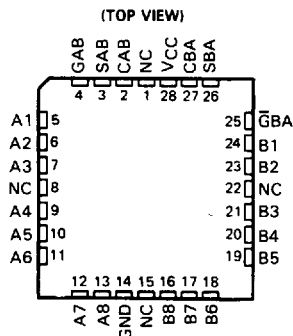
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE



SN54ALS', SN54AS' . . . FK PACKAGE



NC - No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{GBA}}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{GBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The -1 versions of the SN74ALS651 through SN74ALS653 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54' series.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

**SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652
 SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
 OCTAL BUS TRANSCEIVERS AND REGISTERS**

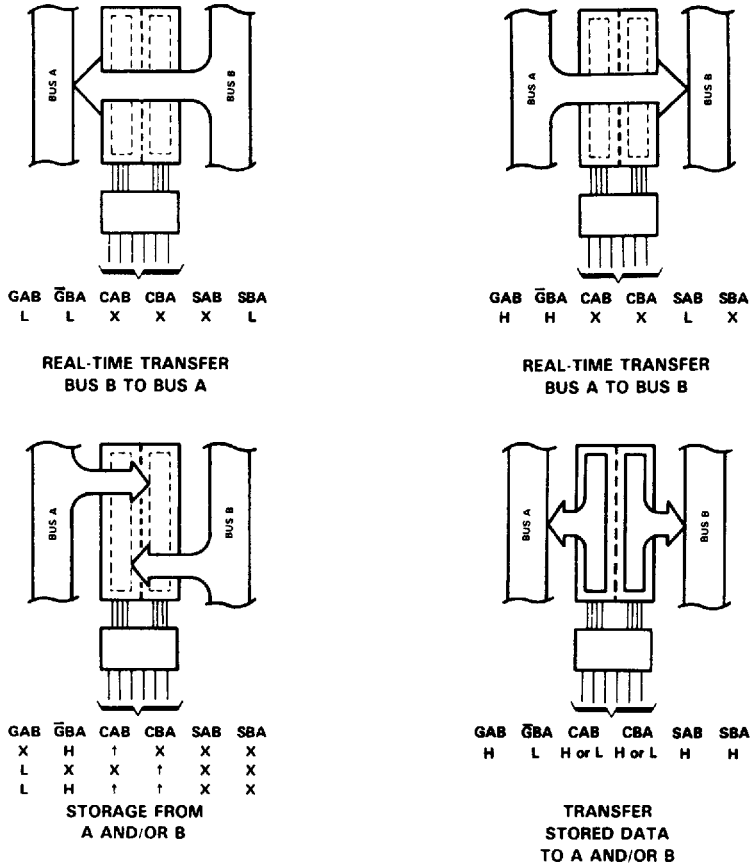


Figure 1. Bus Transfer Diagram

SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

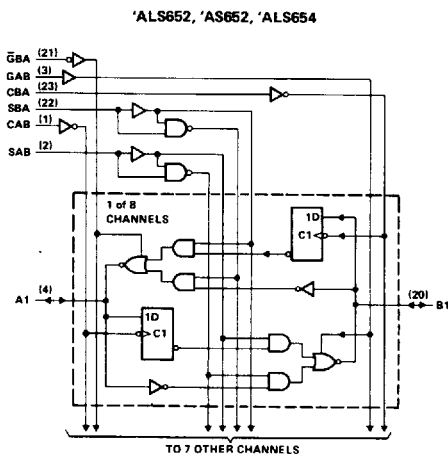
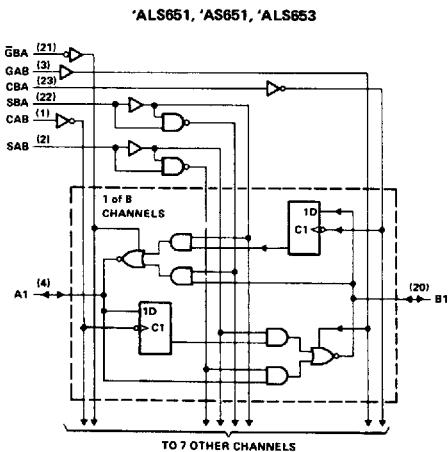
INPUTS				DATA I/O				OPERATION OR FUNCTION	
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	-	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	+	↑	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B	Hold A, Store B
L	L	*	↑	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time \bar{B} Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored \bar{B} Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time \bar{A} Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored \bar{A} Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored \bar{A} Data to B Bus and Stored \bar{B} Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

†The data output functions may be enabled or disabled by various signals at the GAB or $\bar{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.

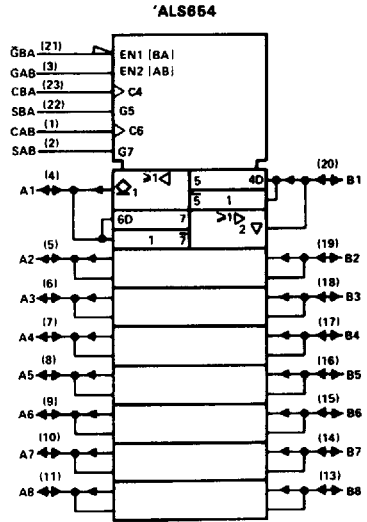
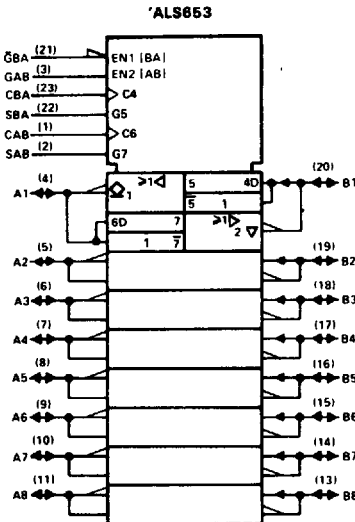
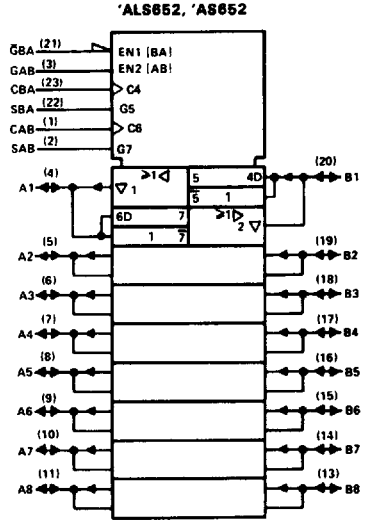
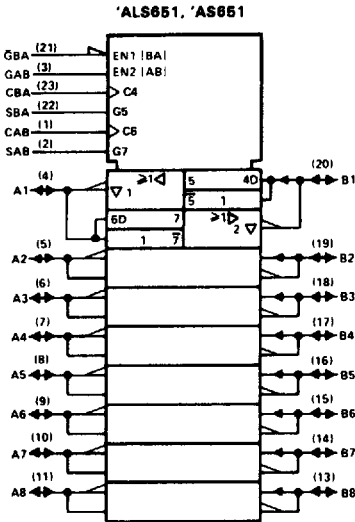
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages

**SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652
SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12
Pin numbers shown are for DW, JT, and NT packages



SN74ALS651, SN74ALS652, SN54ALS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS652	-55°C to 125°C
SN74ALS651, SN74ALS652	0°C to 70°C
Storage temperature range	-65°C to 150°C

'ALS651 recommended operating conditions

		SN74ALS651			UNIT	
		MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5	5.5	V	
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage	0.8			V	
I_{OH}	High-level output current	-15			mA	
I_{OL}	Low-level output current	24			mA	
		48 [†]				
f_{clock}	Clock frequency	0	40		MHz	
t_w	Pulse duration	CBA or CAB high			ns	
		12.5				
t_{su}	Setup time before $CAB\uparrow$ or $CBA\uparrow$	CBA or CAB low			ns	
		12.5				
t_{th}	Hold time after $CAB\uparrow$ or $CBA\uparrow$	A or B			ns	
T_A	Operating free-air temperature	0			70	°C

'ALS652 recommended operating conditions

		SN54ALS652			SN74ALS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.8			0.8			V
I_{OH}	High-level output current	-12			-15			mA
I_{OL}	Low-level output current	12			24			mA
		48 [†]			40			
f_{clock}	Clock frequency	0	35		0	40		MHz
t_w	Pulse duration	CBA or CAB high			12.5			ns
		14.5			12.5			
t_{su}	Setup time before $CAB\uparrow$ or $CBA\uparrow$	CBA or CAB low			10			ns
		15			0			
t_{th}	Hold time after $CAB\uparrow$ or $CBA\uparrow$	A or B			0			ns
T_A	Operating free-air temperature	-55			125		70	°C

[†]The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 and if V_{CC} is maintained between 4.75 V and 5.25 V

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN74ALS651, SN74ALS652, SN54ALS652

OCTAL BUS TRANSCEIVERS AND REGISTERS

ALS651 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS651			UNIT
		MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$	2.4	3.2		
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$				
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15 \text{ mA}$	2			
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$		0.25	0.4	V
	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 24 \text{ mA}$		0.35	0.5	
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 48 \text{ mA}$ (-1 versions)				
I_I	Control inputs A or B ports	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.1	mA
		$V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$	20		μA
	A or B ports‡		20		
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$	-0.2		mA
	A or B ports‡		-0.2		
I_O^{\S}	B ports	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	mA
I_{CC}	'ALS651	$V_{CC} = 5.5 \text{ V}$	Outputs high		mA
			Outputs low		
			Outputs disabled		
			42	68	
			52	82	
			52	82	

ALS652 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS652			SN74ALS652			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V	
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V	
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2			
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2							
	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -15 \text{ mA}$				2				
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4		V	
	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 24 \text{ mA}$				0.35	0.5			
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 48 \text{ mA}$ (-1 versions)								
I_I	Control inputs A or B ports	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$		0.1		0.1		mA	
		$V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$		0.1		0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$	20		20		μA		
	A or B ports‡		20		20				
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$	-0.2		-0.2		mA		
	A or B ports‡		-0.2		-0.2				
I_O^{\S}	B ports	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112	mA		
I_{CC}	'ALS652	$V_{CC} = 5.5 \text{ V}$	Outputs high		47	76	47	76	mA
			Outputs low		55	88	55	88	
			Outputs disabled		55	88	55	88	

†All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN74ALS651, SN74ALS652, SN54ALS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

'ALS651 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX		UNIT
			SN74ALS651		
			MIN	MAX	
f _{max}			40		MHz
t _{PLH}	CBA or CAB	A or B	10	32	ns
t _{PHL}			5	17	
t _{PLH}	A or B	B or A	4	18	ns
t _{PHL}			2	10	
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	13	38	ns
t _{PHL}			7	21	
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	8	25	ns
t _{PHL}			7	21	
t _{PZH}	G \bar{B} A	A	5	20	ns
t _{PZL}			5	18	
t _{PHZ}	B \bar{B} A	A	2	9	ns
t _{PLZ}			3	12	
t _{PZH}	GAB	B	7	22	ns
t _{PZL}			7	21	
t _{PHZ}	GAB	B	2	12	ns
t _{PLZ}			2	14	

'ALS652 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX				UNIT
			SN54ALS652		SN74ALS652		
			MIN	MAX	MIN	MAX	
f _{max}			35		40		MHz
t _{PLH}	CBA or CAB	A or B	10	35	10	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A or B	B or A	5	20	5	18	ns
t _{PHL}			3	15	3	12	
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	15	40	15	35	ns
t _{PHL}			6	23	6	20	
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	8	30	8	25	ns
t _{PHL}			5	24	5	20	
t _{PZH}	G \bar{B} A	A	3	20	3	17	ns
t _{PZL}			5	22	5	18	
t _{PHZ}	G \bar{B} A	A	1	12	1	10	ns
t _{PLZ}			2	20	2	16	
t _{PZH}	GAB	B	8	25	8	22	ns
t _{PZL}			6	21	6	18	
t _{PHZ}	GAB	B	1	12	1	10	ns
t _{PLZ}			2	21	2	16	

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN74ALS653, SN74ALS654, SN54ALS653 OCTAL BUS TRANSCEIVERS AND REGISTERS

ALS653 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS653			SN74ALS653			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}	B ports	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
		V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4	3.2		2.4	3.2		
		V _{CC} = 4.5 V, I _{OH} = -12 mA	2						
		V _{CC} = 4.5 V, I _{OH} = -15 mA				2			
I _{OH}	A ports	V _{CC} = 4.5 V, V _{OH} = 5.5 V					0.1	mA	
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA	0.25	0.4		0.25	0.4	V	
		V _{CC} = 4.75 V, I _{OL} = 24 mA				0.35	0.5		
		V _{CC} = 4.75 V, I _{OL} = 48 mA (-1 versions)							
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V					0.1	mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V					0.1		
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V					20	μA	
	A or B ports‡						20		
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V					-0.2	mA	
	A or B ports‡						-0.2		
I _O [§]	B ports	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112		-30	-112	mA	
I _{CC}	'ALS653	V _{CC} = 5.5 V	Outputs high	47	76		47	76	mA
			Outputs low	55	88		55	88	
			Outputs disabled	55	88		55	88	

ALS654 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS654			UNIT			
		MIN	TYP†	MAX				
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2	V			
V _{OH}	B ports	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V		
		V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4	3.2				
		V _{CC} = 4.5 V, I _{OH} = -12 mA						
		V _{CC} = 4.5 V, I _{OH} = -15 mA			2			
I _{OH}	A ports	V _{CC} = 4.5 V, V _{OH} = 5.5 V			0.1	mA		
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 12 mA			0.25	0.4	V	
		V _{CC} = 4.75 V, I _{OL} = 24 mA						
		V _{CC} = 4.75 V, I _{OL} = 48 mA (-1 versions)			0.35	0.5		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V				0.1	mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V				0.1		
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V				20	μA	
	A or B ports‡					20		
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V				-0.2	mA	
	A or B ports‡					-0.2		
I _O [§]	B ports	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112		-112	mA	
I _{CC}	'ALS654	V _{CC} = 5.5 V	Outputs high	47	76		76	mA
			Outputs low	55	88		88	
			Outputs disabled	55	88		88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_OS

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

 **TEXAS
INSTRUMENTS**

SN74ALS653, SN54ALS653
OCTAL BUS TRANSCEIVERS AND REGISTERS

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R ₁ = R ₂ = 500 Ω (B outputs), T _A = MIN to MAX				UNIT
			SN54ALS653		SN74ALS653		
			MIN	MAX	MIN	MAX	
f _{max}		A	12.5				MHz
		B	25				
t _{PLH}	CBA	A	16	71	16	64	ns
t _{PHL}			6	2 [†]	6	22	
t _{PLH}	CAB	B	10	35	10	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A	B	5	20	5	18	ns
t _{PHL}			15	18	2	15	
t _{PLH}	B	A	8	63	12	56	ns
t _{PHL}			2	18	2	15	
t _{PLH}	SBA [†] (with B high)	A	19	68	19	62	ns
t _{PHL}			5	27	5	25	
t _{PLH}	SBA [†] (with B low)	A	19	68	19	62	ns
t _{PHL}			5	27	5	25	
t _{PLH}	SAB [†] (with A high)	B	8	30	15	35	ns
t _{PHL}			6	25	6	22	
t _{PLH}	SAB [†] (with A low)	B	12	40	8	25	ns
t _{PHL}			6	25	6	22	
t _{PLH}	G̅BA	A	6	35	6	30	ns
t _{PHL}			6	27	6	24	
t _{PZH}	GAB	B	7	25	8	22	ns
t _{PZL}			6	25	6	22	
t _{PHZ}	GAB	B	1	16	1	14	ns
t _{PLZ}			2	21	2	16	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input

SN74ALS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R ₁ = R ₂ = 500 Ω (B outputs), T _A = MIN to MAX		UNIT
			SN74ALS654		
			MIN	MAX	
f _{max}		A B	35		MHz
t _{PLH}	CBA	A	16	64	ns
t _{PHL}			6	22	
t _{PLH}	CAB	B	10	30	ns
t _{PHL}			5	17	
t _{PLH}	A	B	5	18	ns
t _{PHL}			2	15	
t _{PLH}	B	A	12	56	ns
t _{PHL}			2	15	
t _{PLH}	SBA [†] (with B high)	A	19	62	ns
t _{PHL}			5	25	
t _{PLH}	SBA [†] (with B low)	A	19	62	ns
t _{PHL}			5	25	
t _{PLH}	SAB [†] (with A high)	B	15	35	ns
t _{PHL}			6	22	
t _{PLH}	SAB [†] (with A low)	B	8	25	ns
t _{PHL}			6	22	
t _{PLH}	$\overline{\text{G}}\text{BA}$	A	6	30	ns
t _{PHL}			6	24	
t _{PZH}	GAB	B	8	22	ns
t _{PZL}			6	22	
t _{PHZ}	GAB	B	1	14	ns
t _{PLZ}			2	16	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the input.

SN74AS651, SN74AS652, SN54AS651, SN54AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

AS651 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB [†]	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\bar{C}BA$	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\bar{C}BA$	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

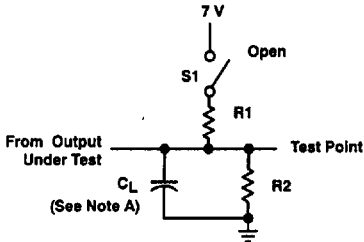
AS652 switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB [†]	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\bar{C}BA$	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\bar{C}BA$	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input

**SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652
SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS**

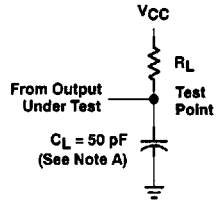
PARAMETER MEASUREMENT INFORMATION



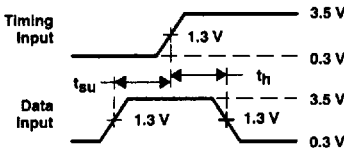
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

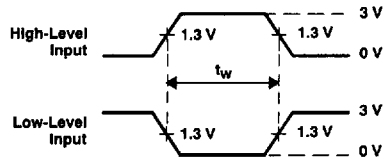
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



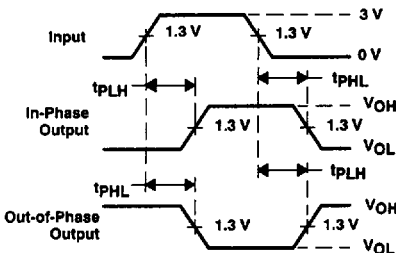
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



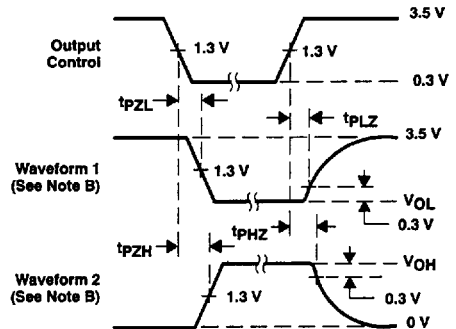
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES. A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%

D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms