XMC1100 / XMC1200 / XMC1300

Fixed Flash Wait States

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet Addendum

V1.0 2016-02

Microcontrollers

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1 Fixed Flash Wait States

The parameter limits defined in this addendum extend the electrical parameters defined in the XMC1100 / XMC1200 / XMC1300 Data Sheet stated below.

- Data Sheet AA-Step, V1.4, 2014-05
- Data Sheet AB-Step, V1.6, 2015-04

1.1 Flash read access with fixed wait states

Per default the XMC1100 / XMC1200 / XMC1300 devices use a configuration with adaptive wait states for read accesses to the flash memory, dynamically adapting to the system frequency and flash access timing without user software interaction.

Alternatively, it is possible to configure the XMC1100 / XMC1200 / XMC1300 devices to apply fixed wait states to each flash read access, improving determinism of program execution from flash. The required number of wait states depends on the system frequency f_{MCLK}, as defined in the parameter $N_{FWSFLASH}$. The number of wait states can be configured with the bit **NVM_NVMCONF**.WS, the selection of adaptive or fixed wait states is done with the bit **NVM_CONFIG1**.WS.

Attention: Any write operation to the register NVM_CONFIG1 to switch between adaptive and fixed wait states configuration must only modify the bit NVM_CONFIG1.FIXWS. Changing other bits in NVM_CONFIG1 can lead to unpredictable results.

Attention: Before and after the fixed wait states configuration or the system frequency f_{MCLK} is changed, the number of selected wait states must always comply to the parameter $N_{FWSFLASH}$.

Below is a code snippet defining the register addresses, configuring one wait state and then switching to operation with fixed wait states.

Example

```
// Headers and variables to fix number of wait states to "1"
#define ADDR1 0x40050008   //Address of NVM_NVMCONF
uint32_t * NVM_NVMCONF  = (uint32_t *) ADDR1;
#define ADDR2 0x40050048   //Address of NVM_CONFIG1
uint32_t * NVM_CONFIG1  = (uint32_t *) ADDR2;

// init sequence to fix number of wait states to "1"
*NVM_NVMCONF = *NVM_NVMCONF | 0x1000; //Set .WS bit => 1WS
*NVM_CONFIG1 = *NVM_CONFIG1 | 0x0800; //Set .FIXWS bit => fixed
WS scheme
```

1.2 NVM Registers

NVM Configuration Register

The definition of bit NVMCONF.12 changes to NVMCONF.WS.

NVM_NVMCONF
NVM Configuration Register (4005 0008$_H$) Reset Value: 9000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM_ON	INT_ON	0	WS	SECPROT								0	HRLEV		0
rw	rw	rw	rw	rw								r	rw		rw

Field	Bits	Type	Description
NVM_ON	15	rw	**NVM On** When cleared, no software code can be executed anymore from the NVM, until it is set again. I.e., already the software code that initiates the change in NVM_ON itself may not reside in the NVM, otherwise the software is stalled forever. 0_B **SLEEP**, NVM is switched to or stays in sleep mode. 1_B **NORM**, NVM is switched to or stays in normal mode.
INT_ON	14	rw	**Interrupt On** When enabled the completion of a sequence started by setting NVMPROG.ACTION (write or erase sequence) will be indicated by NVM interrupt. The same is true for the wake-up sequence. 0_B **INTOFF**, No NVM ready interrupts are generated. 1_B **INTON**, NVM ready interrupts are generated.
0	13	rw	**Reserved for Future Use** Must be written with 0 to allow correct operation.
WS	12	rw	**Number of fixed Wait States** Defines the number of fixed wait states when NVM_CONFIG1.FIXWS = 1_B. 0_B 0 fixed wait states. 1_B 1 fixed wait state.
SECPROT	11:4	rw	**Sector Protection**[1)] This field defines the number of write, erase, verify protected sectors, starting with physical sector 0.

Field	Bits	Type	Description
0	3	r	**Reserved** Read as 0; should be written with 0.
HRLEV	2:1	rw	**Hardread Level**[2)] Defines single hardread level for verification with NVMPROG.ACTION.VERIFY = 11_B: 00_B **NR**, Normal read 01_B **HRW**, Hardread written 10_B **HRE**, Hardread erased 11_B **RFU**, Reserved for Future Use
0	0	rw	**Reserved for Future Use** Must be written with 0 to allow correct operation.

1) For SECPROT > 0, SECPROT defines the number of protected sectors. The sectors 0 to SECPROT-1 cannot be written, erased, or verified. All writes that target the protected sectors are accepted, but are internally ignored.

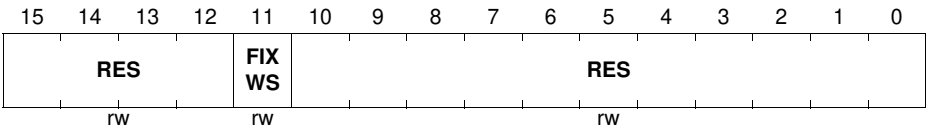
2) HRLEV defines the hardread level for a stand-alone verification sequence started with NVMPROG.ACTION.VERIFY = 11_B. This hardread level is used until the end of the verification sequence. HRLEV may not be changed in between.

Configuration 1 Register

The bit NVM_CONFIG1.FIXWS allows to switch between adaptive and fixed wait state configuration.

Attention: Any write operation to the register NVM_CONFIG1 to switch between adaptive and fixed wait states configuration must only modify the bit NVM_CONFIG1.FIXWS. Changing other bits in NVM_CONFIG1 can lead to unpredictable results.

NVM_CONFIG1
Configuration 1 Register **(4005 0048$_H$)** **Reset Value: XXXX$_H$**



Field	Bits	Type	Description
RES	15:12	rw	**Reserved** Must not be changed when programming the NVM_CONFIG1 register.

Field	Bits	Type	Description
FIXWS	11	rw	**Wait States Scheme** Defines the scheme by which flash wait states are generated. Withfixed wait states NVM_NVMCONF.WS defines the number of wait states. 0_B adaptive wait states. 1_B fixed wait states.
RES	10:0	rw	**Reserved** Must not be changed when programming the NVM_CONFIG1 register.

1.3 Electrical Parameters

1.3.1 Flash Memory Parameters

This definition expands the flash wait states definition by parameters for the configuration with fixed wait states.

Table 1 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{FWSFLASH}$ SR	0	0	1		NVM_CONFIG1.FIXWS = 1_B, $f_{MCLK} \leq$ 16 MHz
		1	1	1		NVM_CONFIG1.FIXWS = 1_B, 16 MHz < $f_{MCLK} \leq$ 32 MHz

w w w . i n f i n e o n . c o m

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