Texas Instruments

User's Guide

SNOA485A–March 2007–Revised May 2013

AN-1602 LMH7322 Dual Comparator Evaluation Board

1 General Description

This board is designed to demonstrate the LMH7322 dual comparator with RSPECL outputs. It will facilitate the evaluation of the LMH7322 in most of the possible configurations. There is one part containing two comparators mounted onto this board. The intention of this board is to demonstrate the conversion of an analog signal to a digital presentation at LVDS levels and to translate this LVDS signal to RSECL levels. The LATCH function can be evaluated using the two switches mounted on the edge of the board. Two test points located between the comparators allows checking the LVDS levels while the output signals are fed to two SMA connectors that feed the signals on a 50 Ω basis to any scope or analyzer. To demonstrate the hysteresis functionality both hysteresis resistors are mounted on header pins, which makes them changeable in a convenient manner. Only two supply voltages are needed to make this setup work. The positive supply is +2.5 V and the negative supply is −5.2 V.

2 Basic Operation

The complete schematic consists of two comparators that show the conversion of analog to LVDS and LVDS to RSECL levels.

2.1 Input Conditions

The input signal is connected to an SMA connector and feed to the non-inverting input of the first comparator. This is a DC path and referenced to ground by a 50 Ω (R3) resistor. The inverting input is also referenced to ground via a 50 Ω (R4) resistor. If no signal is present and both inputs are referenced to the same voltage, the comparator may oscillate if no precautions are taken. Adding a hysteresis resistor introduces a small voltage around the trip point, which prevents the input stage from continuously switching due to noise or other uncontrolled events. The hysteresis voltage can be varied by changing the resistor value connected to J3 (input stage) or J4 (output stage). The resistor can be varied between its extremes of being shorted or being open. Both situations are allowed. The short means that the highest hysteresis voltage is set and an open connection means that there is no hysteresis voltage set. This last situation means that there is the highest risk for oscillations if no signal or a very small signal is applied. It is desirable to use some hysteresis while working with very small and/ or low frequency signals.

2.2 The Latch Function

Both comparators of the LMH7322 have a separate LATCH function, which means that every comparator can be activated or deactivated by a separate LATCH signal. Both latch functions use complementary signals and are connected to the two mini-switches (S1 and S2) situated on the border of the printed circuit board (PCB). If these switches are placed in the 'ON' state, the latch function is active and the outputs are frozen.

2.3 Output Configuration

The outputs of every comparator need to be biased with some current drawn from the Q or $\overline{Q}$. pin. To activate these ECL configured outputs every output has a resistor connected to the most negative supply voltage. This assures that there is always a current flowing out of the pin. The higher the resistor value, the less current is drawn from the pin. Optimizing for high speed means the resistor should have a relatively low value causing a current of 10 to 20 mA to flow out of every pin. A standard termination of 50 Ω to the termination voltage of 2 V below the V_{CCO}, means that the output current for ‘1’ is 18 mA and for ‘0’ is 10 mA. The maximum output current per the output pin is about 40 mA or even more without damaging the device. This means that a system designer has a wide range to vary the bias resistor. Be aware that high resistor values result in slower response times of the comparator, but using values that are too low will also make the response times slower while raising the power consumption. The output signals are connected to SMA connectors via a coupling capacitor of 100 nF (C5 and C6) directly soldered onto the board. In parallel with this capacitor are two header sockets (J1 and J2) that can be used for a larger capacitor. This will lower the 3 dB point of the coupling capacitor and the 50 Ω output termination resistor present on any scope or analyzer. The 3 dB point using only the 100 nF capacitor is about 30 kHz. When placing a capacitor of 10 µF in parallel with the 100 nF, the 3 dB point will be lowered to about 300 Hz. This AC connection is done for testing purposes only, because in this manner no external termination voltage is needed. The test board can now be tested by a direct connection to a scope or analyzer with a 50 Ω termination. If a DC connection is needed to analyze the board the two header sockets can be easily connected using a bended lead.

2.4 Layout Considerations

The setup of the PCB is simple and consists of a double sided PCB with a ground plane on the bottom side and the components and transmission lines on the top side.

2.5 Analog to LVDS Converter

The input transmission line is 50 Ω and is as short as possible. The LVDS output line from the analog to LVDS converter (the first comparator) is designed as a 100 Ω co-planar transmission line terminated with a 100 Ω termination resistor positioned as close as possible to the input of the LVDS to RSECL converter. Close to this termination resistor are two test points and two ground connections. This makes it possible to test the LVDS signals with a standard probe with a ground lead or with a special differential probe, which will give the best results. The power connections, V_{CCI} and V_{CCO}, are connected together and need a supply voltage of +2.5 V. The V_{EE} supply is −5.2 V and is not critical but is used because this is a standard ECL supply value.

2.6 LVDS TO RSECL Converter

The setup of the LVDS to RSECL converter (the second comparator) is roughly the same but has two different supplies for the V_{CCI} and V_{CCO}. This comparator has to produce (RS)ECL levels and therefore the V_{CCO} is connected to the ground, while the V_{EE} is connected to −5.2 V. Decoupling capacitors are always placed as close as possible to the appropriate pins. Every comparator has a resistor for setting the hysteresis voltage and this resistor is a standard resistor placed into two header sockets, which makes it easy to change its value.

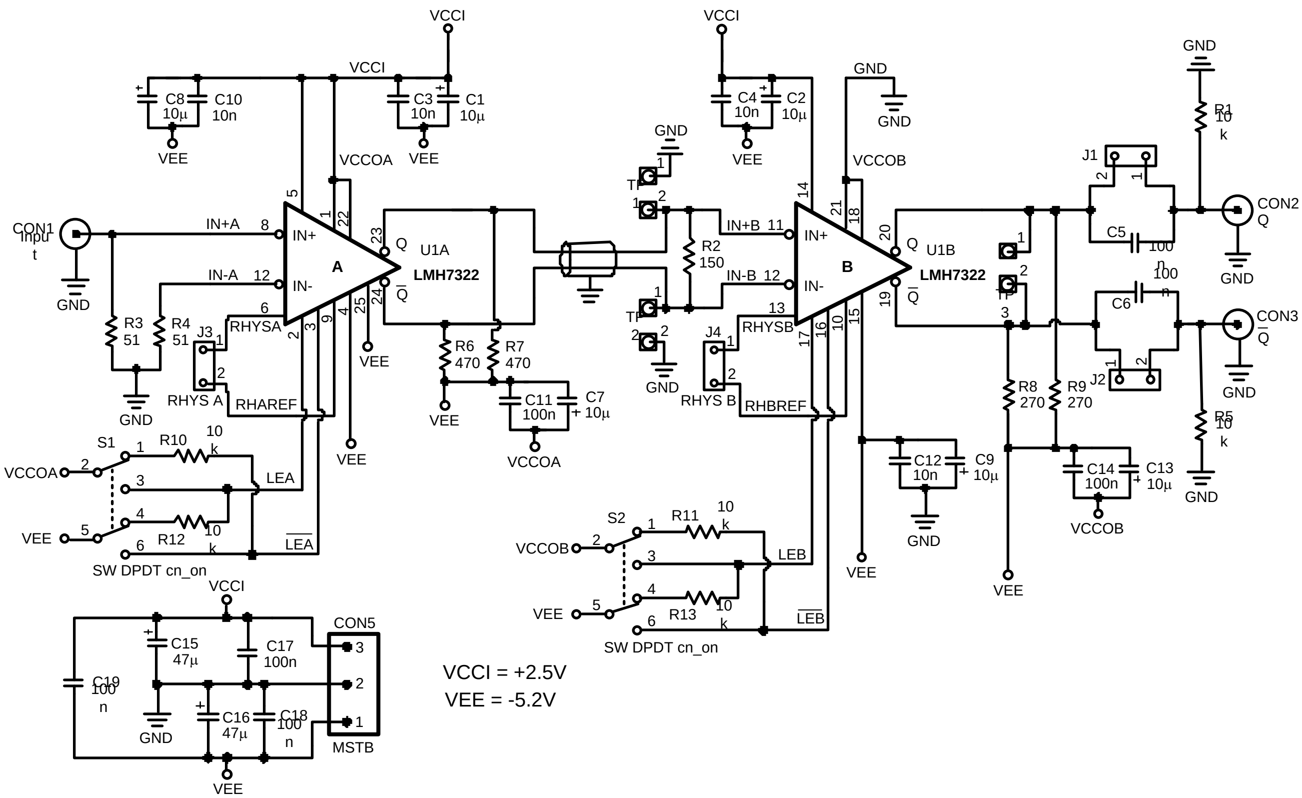
2.7 External Connections

The connections for input and output signals are SMA connectors. The supply voltages are connected via a 3 pole MSTB connector.

3 Measurement Hints

For good high speed results, it is recommended that measurements are done via the SMA output connections. To obtain best results it is necessary to have terminated both outputs, otherwise reflections from one output will disturb the signal integrity on the other. If a probe is needed, be sure to connect via short leads and do not use the standard ground leads with alligator clips that are several inches long. These cause ringing while measuring pulsed signals and lead to the unwanted pick-up of spurious signals. The use of a differential probe is strongly recommended to view the real LVDS output signal, because of the probe's low parasitic capacitance and ease of use. Alternatively, it is possible to use two single probes and construct the LVDS signal by combining both signals.

4 Board Schematic



5 Board Layout

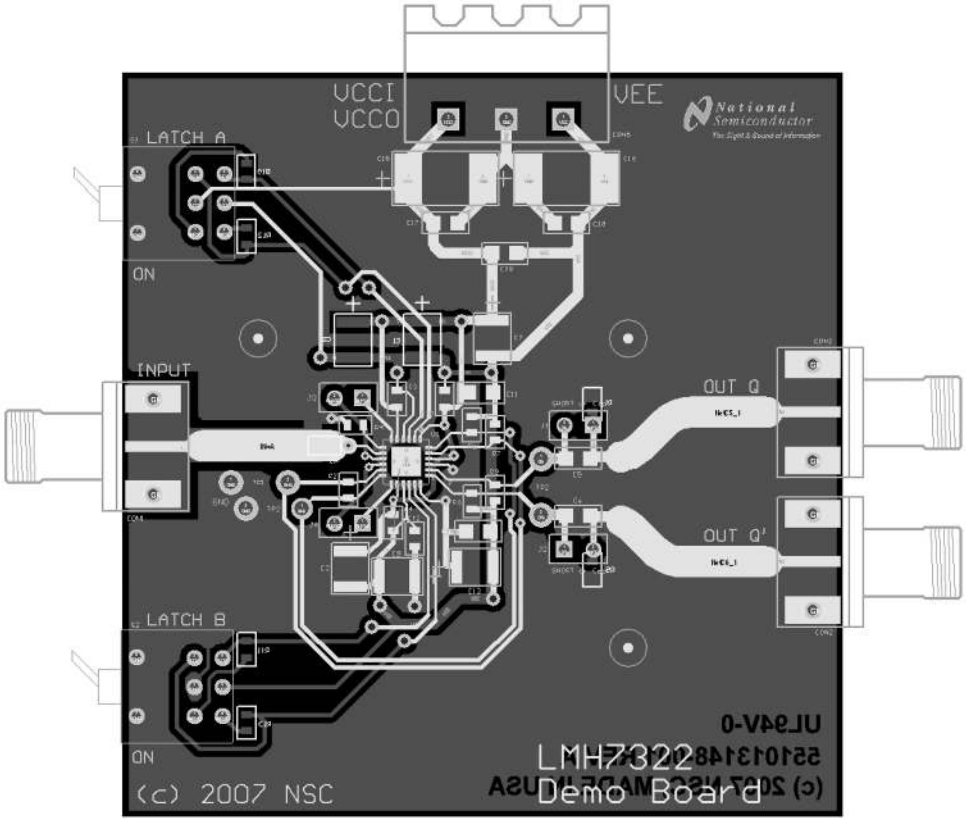


Figure 1. PCB View

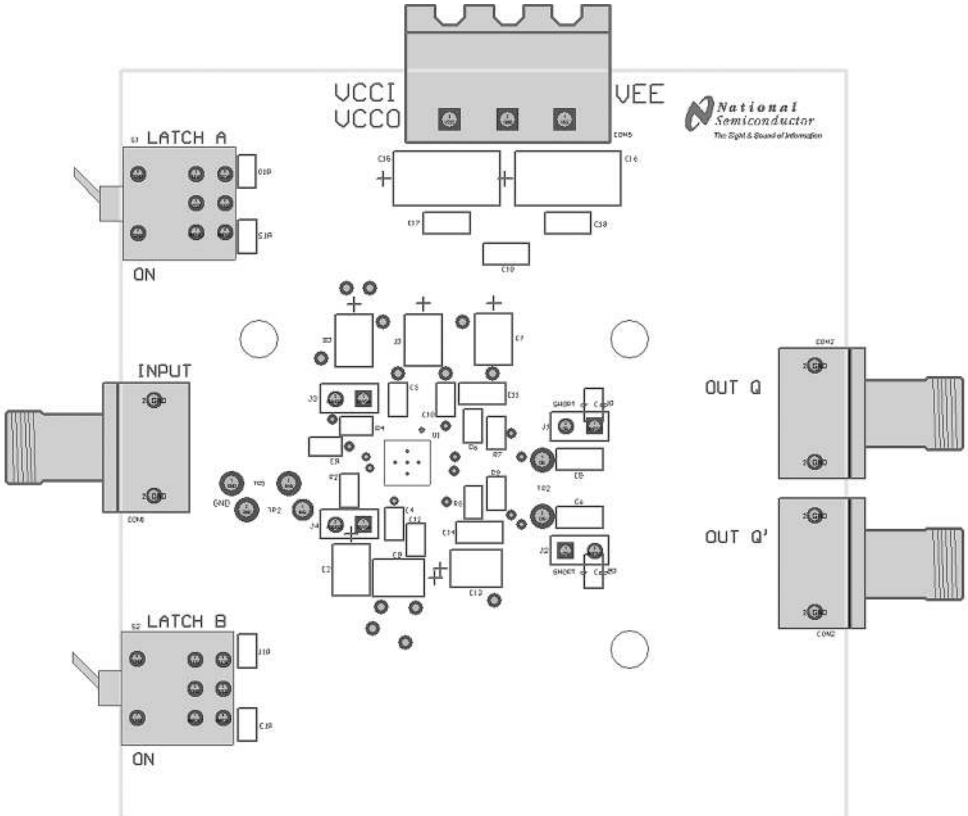


Figure 2. Component View

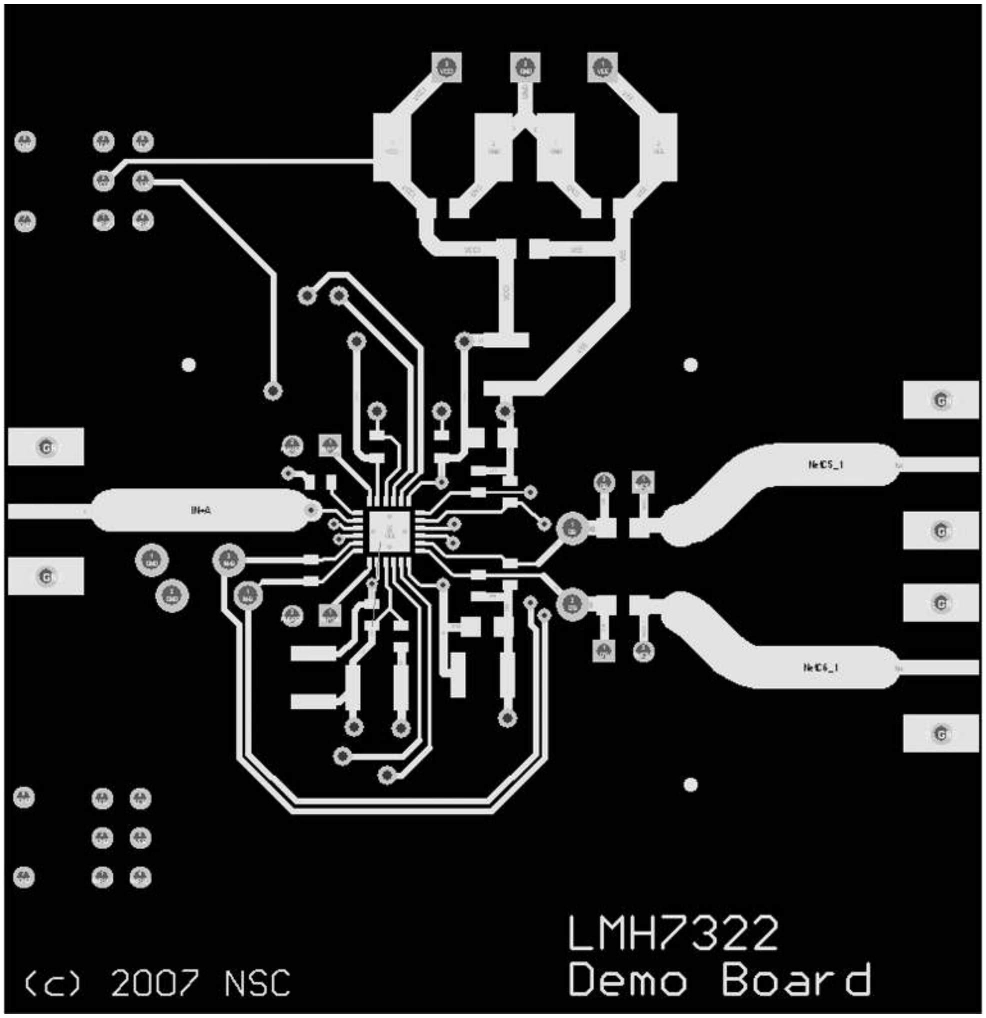


Figure 3. Component View

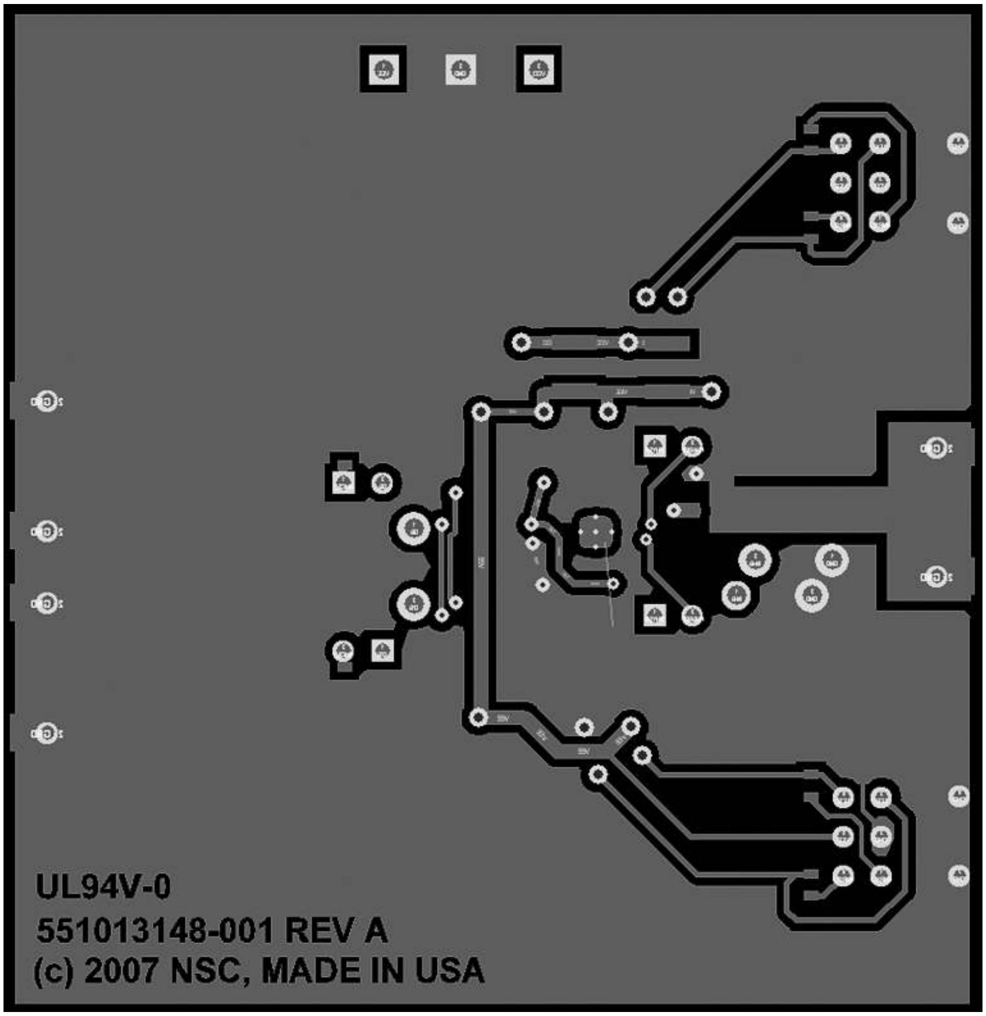


Figure 4. Tracks Bottom Side