LMH2190 Quad Channel 27 MHz Clock Tree Driver with I²C Interface

Check for Samples: LMH2190

FEATURES

- **1 Input Clock, 4 Output Clocks**
- **Supports both Square or Sine Wave Input**
- **1.8V Square Wave Clock Outputs**
- **Skewed Clock Outputs**
- **Independent Clock Request**
- **High Isolation of Supply Noise to Clock Input**
- **High Output to Output Isolation**
- **Output Drive up to 50 pF**
- **EMI Controlled Output Edges and EMI Filtering**
- **Integrated 1.8V Low-Dropout Regulator**
  - **Low Output Noise Voltage**
  - **10 mA load Current**
- **I²C Configurable up to 400 kHz (Fast Mode)**
- **Ultra Low Standby Current**
- **V_{BAT} Range = 2.5V to 5.5V**

APPLICATIONS

- **Mobile Handsets**
- **PDAs**
- **Portable Equipment**

DESCRIPTION

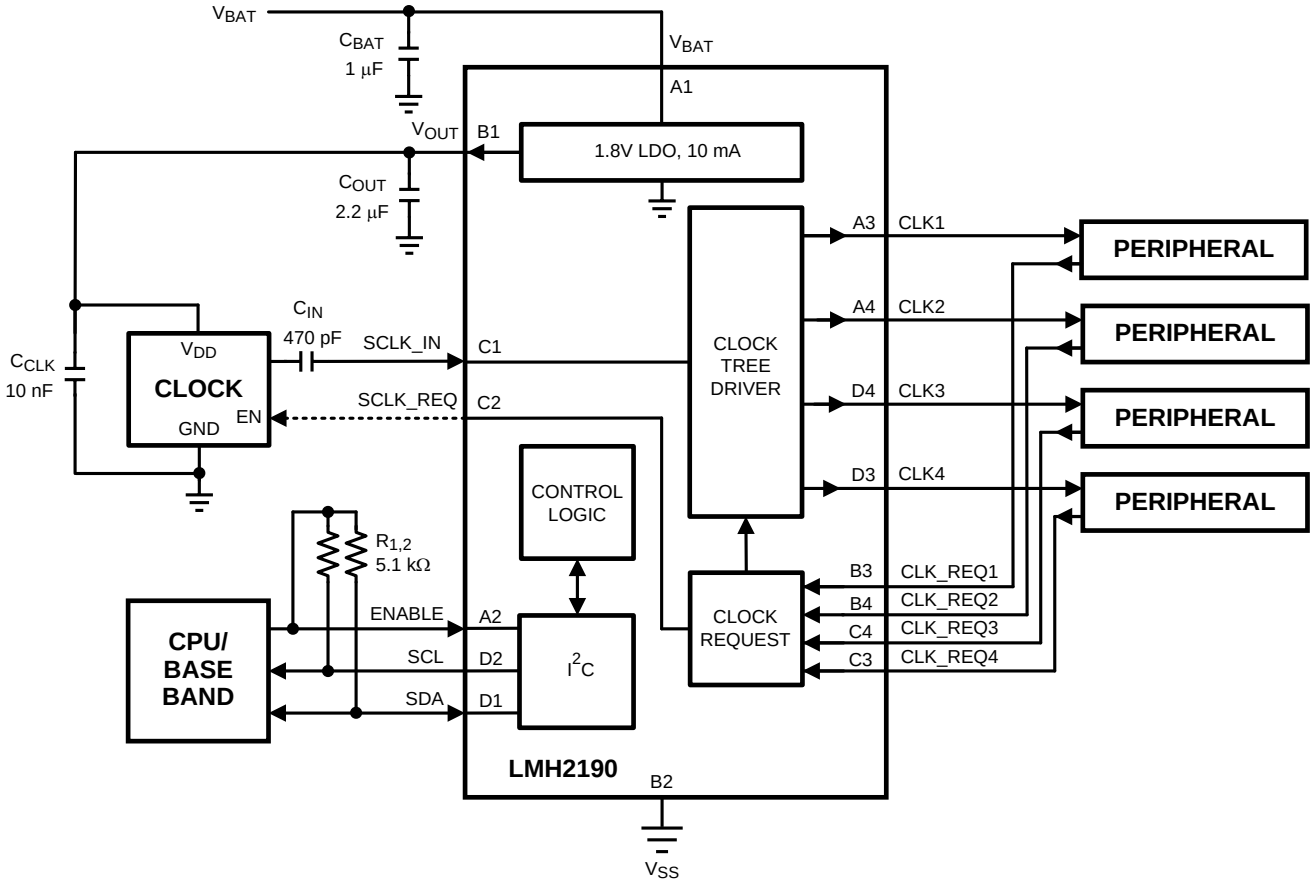
The LMH2190 is a quad channel configurable clock tree driver which supplies a digital system clock to peripherals in mobile handsets or other applications. It provides a solution to clocking issues such as limited drive capability for fanout or longer traces, protection of the master clock from varying loads and frequency pulling effects, isolation buffering from noisy modules, and crosstalk isolation. It has very low phase noise which enables it to drive sensitive modules such as Wireless LAN and Bluetooth.

The LMH2190 can be clocked up to 27 MHz, and has an independent clock request pin for each clock output which allows the peripheral to control the clock. It features an integrated LDO which provides an ultra low noise voltage supply with 10 mA external load current which can be used to supply the TCXO or other clock source.

The I²C serial interface can be used to override the default configuration of the device to optimize the LMH2190 for the application. Some of these programmable features include setting the polarity of both the clock and the clock request inputs. In addition, the clock outputs have programmable output drive current to optimize for the connected load. EMI switching noise can be controlled by configuring output drive and skew settings.

The LMH2190 quad clock distributor is offered in a tiny 1.61mm x 1.61mm 16 bump DSBGA package. Its small size and low supply current make it ideal for portable applications.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage	
V_{BAT} - V_{SS}	-0.3V to 6V
LVCMOS port IO voltage	-0.3V to (V_{OUT} + 0.3V)
Current on CLKx pins	+/- 65 mA
ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C
Maximum Lead Temperature	
(Soldering,10 sec)	230°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but performance is not specified. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, applicable std. MIL-STD-883, Method 3015.7. Machine model, applicable std. JESD22–A115–A (ESD MM std of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std. of JEDEC)
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

OPERATING RATINGS (1)

Supply Voltage (V_{BAT} - V_{SS})	2.5V to 5.5V
V_{ENABLE}	0 to 2V
Input Clock, SCLK_IN	
DC Mode	32 kHz to 27 MHz
AC Mode	13 MHz to 27 MHz
Duty Cycle	45% to 55%
Temperature Range	-40°C to +85°C
Package Thermal Resistance θ_{JA} (2)	113.6°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but performance is not specified. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3.5 V DC AND AC ELECTRICAL CHARACTERISTICS (1)(2)

Unless otherwise specified, all limits are specified at T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See Figure 6) (3), I_{OUT} = 1 mA, Registers are in default setting. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (4)	Typ (5)	Max (4)	Units
Supply Current (6)							
I_{DD}	Active Supply Current	Clock outputs toggling at 26 MHz without external capacitors on CLK1/2/3/4, LDO is ON, I_{OUT} = 0 mA			3		mA
	Shutdown Supply Current	In Shutdown. No clocks toggling. LDO is OFF			0.1	**1**	µA
		In Shutdown. Input CLK toggling, no Clock outputs toggling. LDO is OFF			0.1	**1**	
I_{DDQ}	Quiescent Supply Current	No Clock outputs toggling. LDO is ON, I_{OUT} = 0 mA			36	**60**	µA
		No Clock outputs toggling, LDO is ON, I_{OUT} = 10 mA			50	**80**	
I_{DDEN}	Current to Enable pin	I^2C port is operational				**300**	µA
		I^2C port is idle				**0.1**	
C_{PD}	Power Dissipation Capacitance per CLK output, (7)	Defined with respect to V_{OUT} = 1.8V			15.7	**17.5**	pF
Clock Outputs (CLK1/2/3/4)							
tp_{LH}	Propagation Delay SCLK_IN to CLK1 - Low to High, Figure 1 (7)	50% to 50%			6.5	**10**	ns
tp_{HL}	Propagation Delay SCLK_IN to CLK1 - High to Low, Figure 1 (7)	50% to 50%			7.5	**11**	ns
t_{SKEW}	Skew Between Outputs (Either Edge), Figure 1, (7)	CLK1 to CLK2, 50% to 50%		**3**	6	**8.5**	ns
		CLK2 to CLK3 and CLK3 to CLK4, 50% to 50%		**1**	3.5	**7.3**	
t_{RISE}	Rise Time, Figure 3, (7)(8)	C_L = 10 pF to 50 pF, 20% to 80%			3	**6**	ns
t_{FALL}	Fall Time, Figure 3 (7)(8)	C_L = 10 pF to 50 pF, 80% to 20%			2.5	**5**	
CLK_DC	Output Clock Duty Cycle, Figure 3, (7)	C_L = 10 pF to 50 pF		**42**	50	**58**	%
$Jitter_{RMS}$	Additive RMS period Jitter	BW = 100 Hz to 1 MHz	CLK1		100		fs
			CLK2		240		
			CLK3		330		
			CLK4		400		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(3) V_{DD_IO} is equal to V_{OUT} when the LDO is enabled and it is equal to V_{ENABLE} when it is disabled.
(4) Limits are 100% production tested at 25°C. Limits over temperature range are specified through correlations using statistical quality control (SQC) method.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(6) I_{DD} current depends on switching frequency and load.
(7) This parameter is specified by design and/or characterization and is not tested in production.
(8) Appropriate output load register must be set.

3.5 V DC AND AC ELECTRICAL CHARACTERISTICS [1][2] (continued)

Unless otherwise specified, all limits are specified at T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See Figure 6) [3], I_{OUT} = 1 mA, Registers are in default setting. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min [4]	Typ [5]	Max [4]	Units
Phase Noise	CLK1 Additive Phase Noise with all Outputs toggling	f = 100 Hz		-130		dBc/Hz
		f = 1 kHz		-144		
		f = 10 kHz		-152		
		f = 100 kHz		-158		
		f = 1 MHz		-165		
	CLK2 Additive Phase Noise with all Outputs toggling	f = 100 Hz		-128		
		f = 1 kHz		-139		
		f = 10 kHz		-146		
		f = 100 kHz		-151		
		f = 1 MHz		-153		
	CLK3 Additive Phase Noise with all Outputs toggling	f = 100 Hz		-127		
		f = 1 kHz		-138		
		f = 10 kHz		-144		
		f = 100 kHz		-148		
		f = 1 MHz		-150		
	CLK4 Additive Phase Noise with all Outputs toggling	f = 100 Hz		-125		
		f = 1 kHz		-135		
		f = 10 kHz		-142		
		f = 100 kHz		-147		
		f = 1 MHz		-148		
V_{OH}	CLK1/2/3/4 Output Voltage High Level	CLK1/2/3/4 = -2 mA	**1.6**			V
V_{OL}	CLK1/2/3/4 Output Voltage Low Level	CLK1/2/3/4 = 2 mA			**0.2**	V
R_{OFF}	Output Impedance when disabled	LDO enabled	grounded			
		LDO disabled	diode to ground			
System Clock Input (SCLK_IN)						
V_{IH}	SCLK_IN Input Voltage High Level	DC Mode	**0.65 x V_{OUT}**		**2.0**	V
		AC Mode	**1.2**		**1.8**	
V_{IL}	SCLK_IN Input Voltage Low Level	DC Mode	**0**		**0.35 x V_{OUT}**	V
		AC Mode	**0**		**0.6**	
I_{IH}	SCLK_IN Input Current High Level	SCLK_IN = 1.8V, Clock path disabled		0	**0.1**	µA
I_{IL}	SCLK_IN Input Current Low Level	SCLK_IN = V_{SS}, Clock path disabled	**-0.1**	0		µA
C_{IN}	Input Capacitance [9]			7.5	**10**	pF
V_{BIAS}	DC Bias Voltage	AC Mode		0.805		V
R_{IN}	Input Resistance	AC Mode, Clock path enabled.	**21**	30		kΩ

(9) This parameter is specified by design and/or characterization and is not tested in production.

3.5 V DC AND AC ELECTRICAL CHARACTERISTICS [1][2] (continued)

Unless otherwise specified, all limits are specified at T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See Figure 6) [3], I_{OUT} = 1 mA, Registers are in default setting. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min [4]	Typ [5]	Max [4]	Units
Clock Request Output (SCLK_REQ)						
tp_{LH}	Propagation Delay, Push-Pull and Open Source, Figure 2, [10]	50% to 50%		21	**32**	ns
tp_{HL}	Propagation Delay, Push-Pull and Open Drain, Figure 2, [10]	50% to 50%		15	**21**	ns
V_{OH}	SCLK_REQ Output Voltage High Level	SCLK_REQ = -500 µA, Push-Pull Output	**1.52**			V
		SCLK_REQ = -500 µA, Open Source Output	**1.52**			V
V_{OL}	SCLK_REQ Output Voltage Low Level	SCLK_REQ = 500 µA, Push-Pull Output			**0.2**	V
		SCLK_REQ = 500 µA, Open Drain Output			**0.2**	V
Clock Request Inputs (CLK_REQ1/2/3/4)						
t_{SET}	Setup Time from CLK_REQx to SCLK_IN, to enable CLKx, Figure 4, [10]		**16**			ns
V_{IH}	CLK_REQ1/2/3/4 Input Voltage High Level		**0.8 x V_{DD_IO}**			V
V_{IL}	CLK_REQ1/2/3/4 Input Voltage Low Level				**0.2 x V_{DD_IO}**	V
I_{IH}	CLK_REQ1/2/3/4 Input Current High Level	200 kΩ internal pull down resistor. CLK_REQ1/2/3/4 = 1.8V		8.3	**12.7**	µA
		Without internal / external pull down resistor. CLK_REQ1/2/3/4 = 1.8V		0	**0.1**	µA
I_{IL}	CLK_REQ1/2/3/4 Input Current Low Level	V_{IL} = V_{SS}	**-0.1**	0		µA
SCL and SDA Inputs, V_{ENABLE} = 1.8V [11]						
V_{IH}	SCL and SDA Input Voltage High Level		**0.8 x V_{ENABLE}**			V
V_{IL}	SCL and SDA Input Voltage Low Level				**0.2 x V_{ENABLE}**	V
I_{IH}	SCL and SDA Input Current High Level	SCL/SDA = V_{ENABLE}		0	**0.1**	µA
I_{IL}	SCL and SDA Input Current Low Level	100 kΩ internal Pull-up resistor, SCL/SDA = V_{SS}	**-28**	-18		µA
V_{OL}	SDA Output Voltage Low Level	SDA = 3 mA			**0.2**	V
ENABLE Input						
V_{IH}	ENABLE Input Voltage High Level		**1.65**		**2**	V
V_{IL}	ENABLE Input Voltage Low Level				**0.5**	V
I_{IH}	ENABLE Input Current High Level	ENABLE = V_{OUT}			**0.1**	µA
I_{IL}	ENABLE Input Current Low Level	ENABLE = V_{SS}	**-0.1**			µA

(10) This parameter is specified by design and/or characterization and is not tested in production.
(11) I^2C interface uses IO cells specified at 1.8V typical supply (1.6V Min - 2.0V Max).

3.5 V DC AND AC ELECTRICAL CHARACTERISTICS [1][2] (continued)

Unless otherwise specified, all limits are specified at T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See Figure 6) [3], I_{OUT} = 1 mA, Registers are in default setting. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min [4]	Typ [5]	Max [4]	Units
LDO							
V_{OUT}	Output Voltage	I_{OUT} = 1 mA		**1.78**	1.805	**1.82**	V
I_{LOAD}	Load Current [12]	V_{OUT} > 1.74V		0		10	mA
V_{DO}	Dropout Voltage [13]	V_{OUT} = 1.7V, I_{OUT} = 10 mA			100	150	mV
I_{SC}	Short Circuit Current Limit				300		mA
PSRR	Power Supply Rejection Ratio	V_{BAT} ripple = 200 mV_{PP}, I_{OUT} = 10 mA	f = 100 Hz		93		dB
			f = 217.5 Hz		90		
			f = 1 kHz		78		
			f = 10 kHz		62		
			f = 50 kHz		54		
			f = 100 kHz		50		
			f = 1 MHz		42		
			f = 3.25 MHz		35		
E_N	Output Noise Voltage	BW = 10Hz to 100 kHz, V_{BAT} = 4.2V, C_{OUT} = 2.2 µF, All Outputs are Off			10		$µV_{RMS}$
T_{SHTDWN}	Thermal Shutdown	Temperature			160		°C
		Hysteresis			20		
ΔV_{OUT}	Line Transient [14]	V_{BAT} = ($V_{OUT\ (NOM)}$ + 1.0V) to ($V_{OUT\ (NOM)}$ + 1.6V) in 30 µs		**-1**			mV
		V_{BAT} = ($V_{OUT\ (NOM)}$ + 1.6V) to ($V_{OUT\ (NOM)}$ + 1.0V) in 30 µs				**1**	
	Load Transient [14]	I_{OUT} = 0 mA to 10 mA in 10 µs		**-70**			mV
		I_{OUT} = 10 mA to 0 mA in 10 µs				**30**	
	Overshoot on Startup [14]					**100**	mV
R_{OUT}	DC Output Resistance				5		Ω
T_{ON}	Turn on Time [14]	to 95% of $V_{OUT\ (NOM)}$			185	270	µs

(12) The device maintains stable, regulated output voltage without a load.
(13) Dropout voltage is the voltage difference between the supply voltage and the output voltage at which the output voltage drops to 100 mV below its nominal value.
(14) This parameter is specified by design and/or characterization and is not tested in production.

TIMING WAVEFORMS

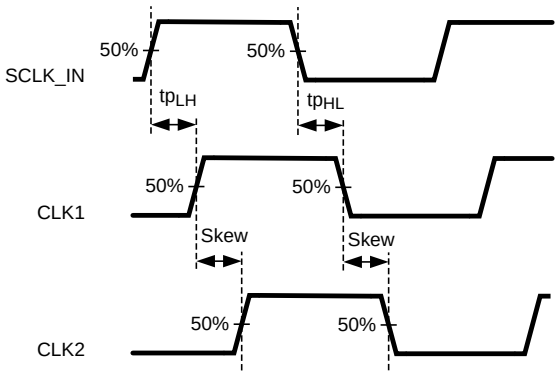


Figure 1. Clock Output Timing Waveforms

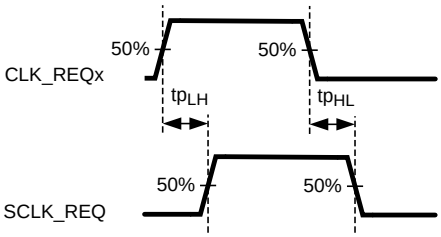


Figure 2. Clock Request Timing Waveforms

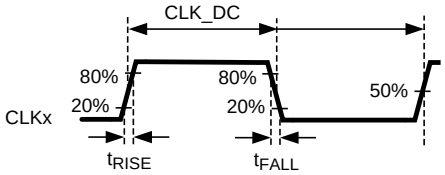


Figure 3. Rise / Fall Time and Duty Cycle Waveform for Clock Outputs

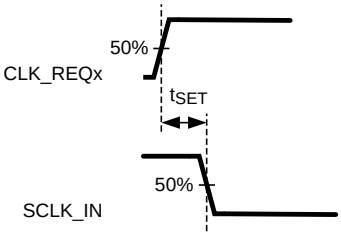


Figure 4. Setup Time from SCLK_IN to CLK_REQ

Connection Diagram

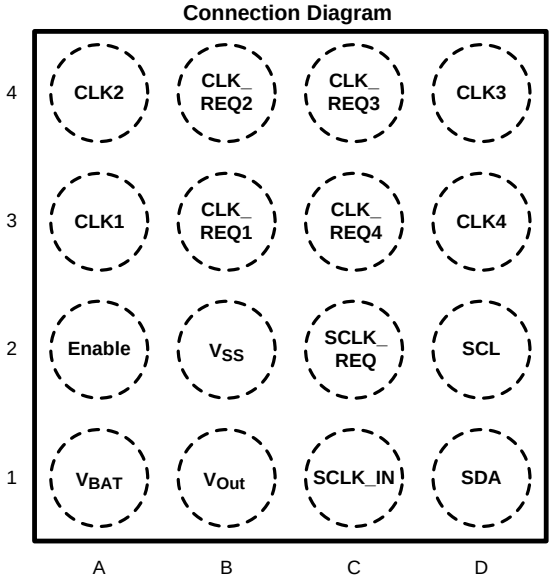


Figure 5. 16-Bump DSBGA
See YFQ0016 Package

PIN DESCRIPTIONS(1)

Pin	Pin Name	Port/Direction	Type	DESCRIPTION
C1	SCLK_IN	Host	I	Source Clock Input
C2	SCLK_RQ	Host	O	Source Clock Request
A3	CLK1	Peripheral	O	Clock Output 1
B3	CLK_REQ1	Peripheral	I	Clock Request Input 1
A4	CLK2	Peripheral	O	Clock Output 2
B4	CLK_REQ2	Peripheral	I	Clock Request Input2
D4	CLK3	Peripheral	O	Clock Output 3
C4	CLK_REQ3	Peripheral	I	Clock Request Input 3
D3	CLK4	Peripheral	O	Clock Output 4
C3	CLK_REQ4	Peripheral	I	Clock Request Input 4
A2	ENABLE	Host	I	Enable Device, Active High
D2	SCL	Host	I	I^2C Clock Input, 100 kΩ Pull-up to ENABLE
D1	SDA	Host/Bidirectional	I/O	I^2C Data I/O, 100 kΩ Pull-up to ENABLE
A1	V_{BAT}	Battery/Input	Power	Power Supply
B1	V_{OUT}	LDO/Output	Power	Power Supply to Clock Source and Clock Outputs
B2	V_{SS}	Ground	Ground	Ground Pin

(1) I = Input, O = Output, I/O = Input / Output

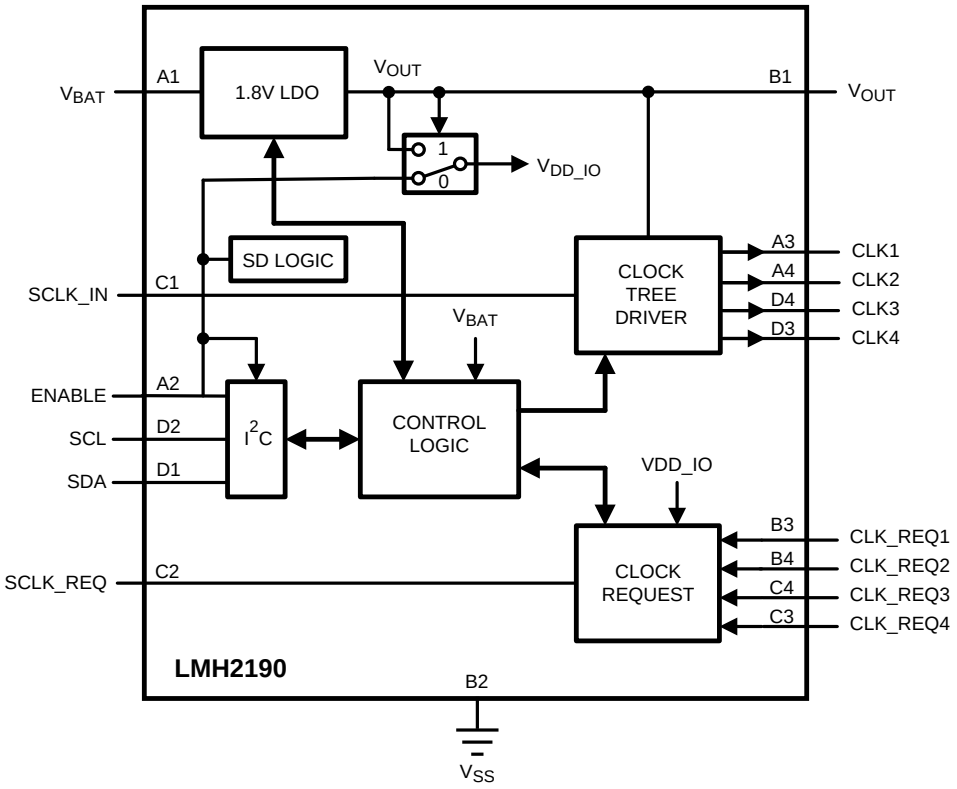


Figure 6. LMH2190 Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See Figure 19), Registers are in default configuration.

Supply Current vs. Supply Voltage

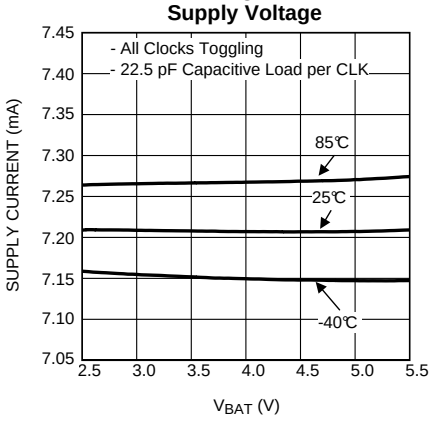


Figure 7.

Supply Current vs. Input Clock Frequency

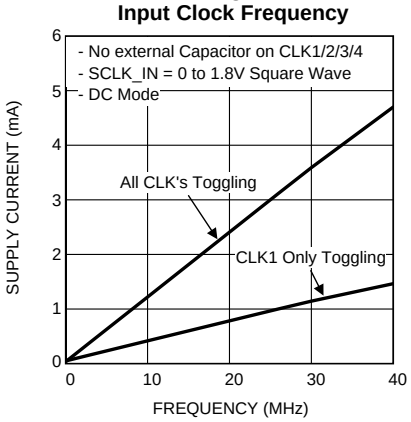


Figure 8.

Supply Current vs. Capacitive Load

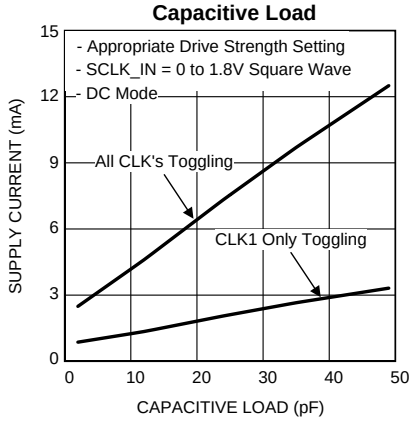


Figure 9.

LDO Output Voltage vs. Supply Voltage

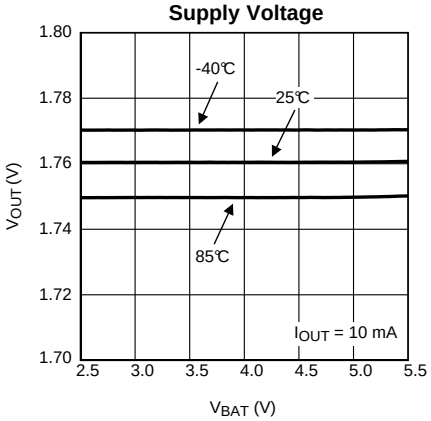


Figure 10.

LDO Output Voltage vs. LDO Output Current

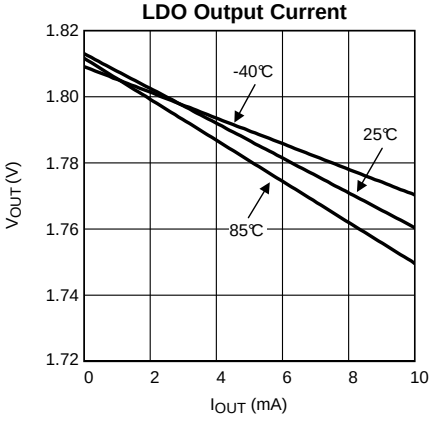


Figure 11.

LDO Output Voltage vs. Time

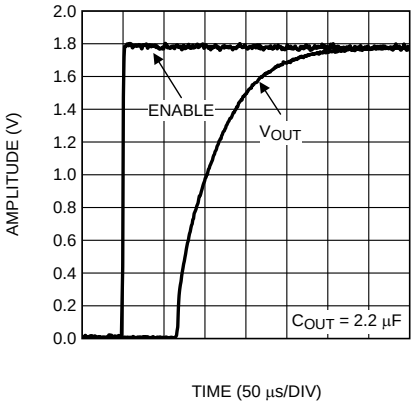


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See Figure 19), Registers are in default configuration.

Additive Phase Noise vs. Frequency Offset

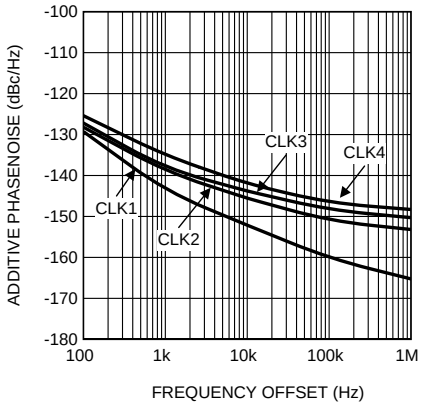


Figure 13.

CLK1 Response, C_L = 10 pF

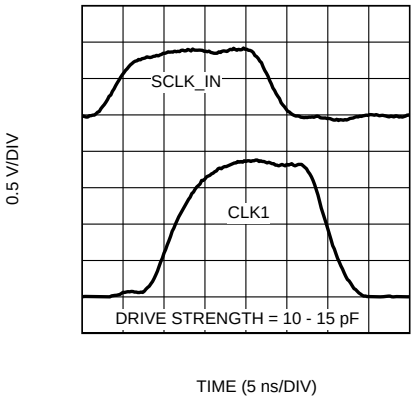


Figure 14.

CLK1 Response, C_L = 22pF

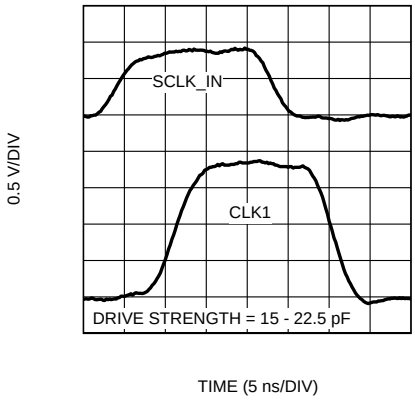


Figure 15.

CLK1 Response, C_L = 33 pF

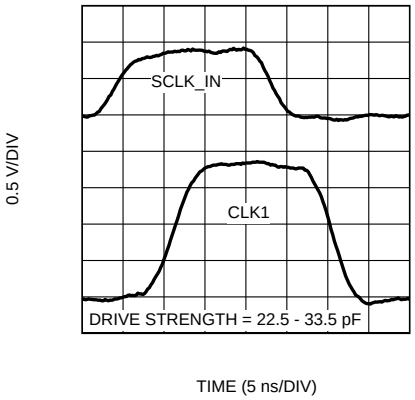


Figure 16.

CLK1 Response, C_L = 50 pF

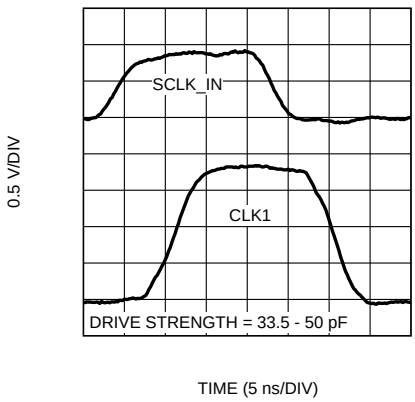


Figure 17.

Power Supply Rejection Ratio vs. Frequency

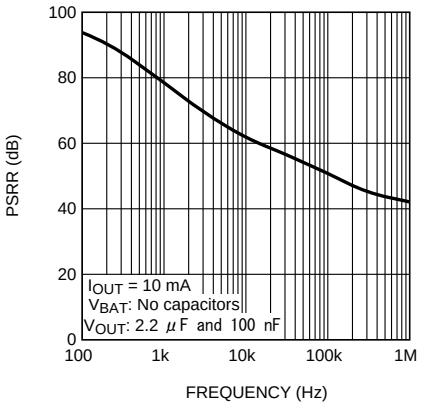


Figure 18.

APPLICATION INFORMATION

The LMH2190 is a quad channel configurable clock distribution device which supplies a digital system clock to peripherals in mobile handsets or other applications. Examples of peripherals are Bluetooth, Wireless LAN, and/or Digital Video Broadcast-H (DVB-H).

The LMH2190 provides a solution to clocking issues such as limited drive capability, frequency pulling and crosstalk. The drive capability of a TCXO can be insufficient when traces are long and/ or multiple peripherals are connected to one TCXO. The LMH2190's clock outputs can be configured independently to drive capacitive loads up to 50 pF per channel. The buffer function of the LMH2190 prevents frequency pulling of the TCXO. Frequency pulling can occur when the TCXO observes varying loads. A peripheral device that shuts down can cause this load variation for instance. Crosstalk between peripheral devices is minimal since each peripheral has its own LMH2190 digital clock output. Also isolation from peripheral to TCXO is specified by use of the LMH2190.

Adding a component in the clock path inherently means adding noise. The LMH2190 though has excellent phase noise specifications in order to minimize degradation of the clock quality. A typical LMH2190 application is depicted in Figure 19.

The LMH2190 clock tree driver can be divided into 4 blocks:

- Clock tree driver
  - The clock tree driver provides a clean clock to a maximum of 4 separately connected peripheral devices.
- Clock request logic
  - Independent clock request inputs allow the peripheral to control when the particular clock should be enabled. Further, the clock request inputs control the source clock request (SCLK_REQ) and enabling of the LDO.
- Low Dropout regulator (LDO)
  - The LDO provides a low noise, high PSRR supply voltage that enables low phase noise on the clock outputs, and low quiescent current for portable applications. It can also be used to provide a low noise supply to the TCXO eliminating the need for a separate LDO.
- I^2C Control logic
  - An I^2C control port enables re-configuration of settings of many features of the device in order to optimize the device performance based on the application. For these settings see Table 2, Table 3, Table 4, Table 5, and Table 6 in I^2C Registers.

All the blocks can be switched into a low power-consumption mode to save energy. This functionality is controlled via the ENABLE pin.

The following sections provide an explanation on PHASE NOISE and a detailed description of each block.

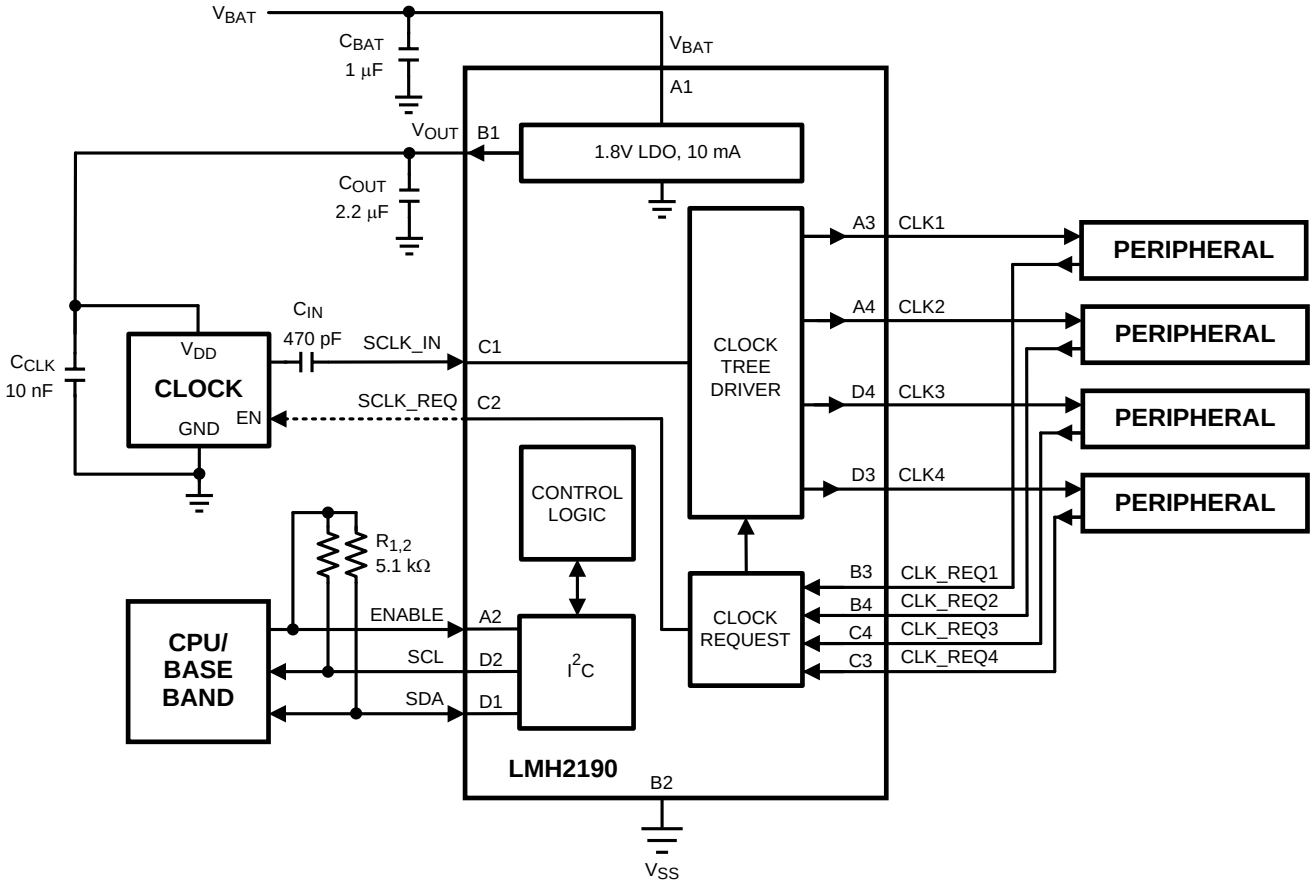


Figure 19. Typical LMH2190 Setup

PHASE NOISE

An important specification for oscillators and clock buffers is phase noise. It determines the timing and thus accuracy of various peripheral devices in a cell phone such as Bluetooth, WLAN and DVB-H.

Phase noise is expressed in the frequency domain and is usually specified at a number of offset frequencies from the carrier frequency. The phase noise of the oscillator and the LMH2190 together determine the phase noise of the clock that is distributed to the peripheral devices. Therefore an additive phase noise is specified for the LMH2190 rather than its total output phase noise since that depends on the TCXO connected to the LMH2190.

Knowing the TCXO phase noise and the additive phase noise of the LMH2190, the total phase noise to the peripheral can be calculated:

$$PN = 10 \text{ LOG} \left[10^{\frac{PN\_TCXO}{10}} + 10^{\frac{add.PN\_LMH2190}{10}} \right]$$

Where, PN is the total phase noise at the output of the LMH2190, PN_TCXO is the TCXO's phase noise and add.PN_LMH2190 is the additive phase noise of the LMH2190, all in dBc/Hz.

CLOCK TREE DRIVER

The clock tree driver consists of one input that drives 4 outputs (Figure 20). It is supplied by the highly accurate 1.8V LDO. In default configuration the outputs are switched on when the clock request inputs are high. The input as well as the output can be configured in several ways though I^2C programming.

Clock Tree Driver Input

The source clock input (SCLK_IN) is the input for the clock tree driver. It can be configured to DC or AC coupled mode. In shutdown mode, the input stage is completely switched off to prevent unnecessary power consumption when the source clock is still present.

In the DC coupled mode, the clock input may range from 32 kHz to 27 MHz. DC coupling mode requires that the input is a square wave.

In AC mode an external capacitor needs to be connected in series with the clock source and the SCLK_IN pin to block external DC. Internally, a DC bias network centers it at about $V_{OUT}/2$. This enables the use of a sine wave clock source with a amplitude between 0.8 V_{PP} and 1.8 V_{PP}. The bias voltage is enabled only when the clock request output is activated in order to eliminate the DC power. In the AC coupled mode, the clock input may range from 13 MHz up to 27 MHz. It is assumed to be a sine wave. Signals with sharp edges, such as square wave signals, should be prevented as the DC control loop will not be able to maintain its internal DC level.

Clock Tree Driver Outputs

The LMH2190's clock tree driver outputs have many modes of operation to reduce power consumption and minimize EMI. The output drive strength of the LMH2190 can be selected in 4 steps based on the load capacitance it needs to drive. The configuration can be done via the I^2C interface.

There are two dedicated methods for reducing EMI that can be selected through the I^2C interface. As shown in Figure 21 and Figure 22 the first method (default) skews all of the clock edges individually, so that the EMI generated by the switching is spread out over time. The second method inverts two of the outputs and also skews one pair from the other.

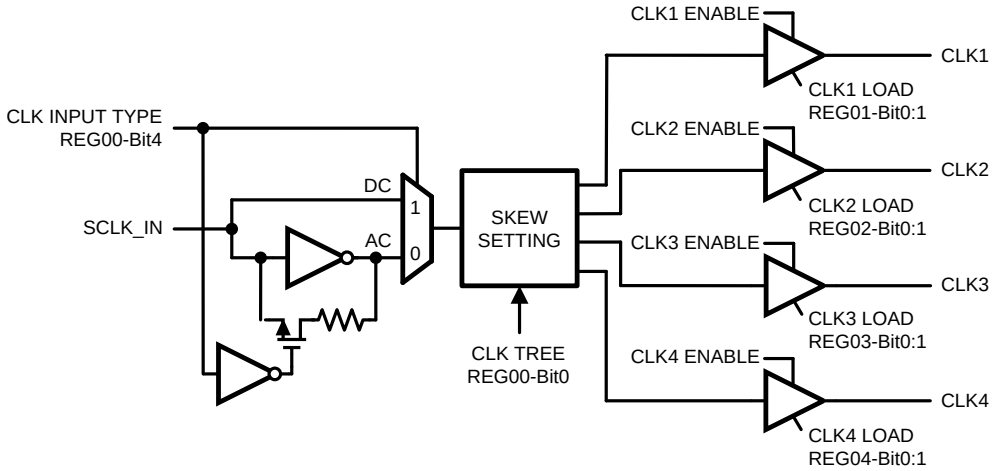


Figure 20. Clock Tree Driver

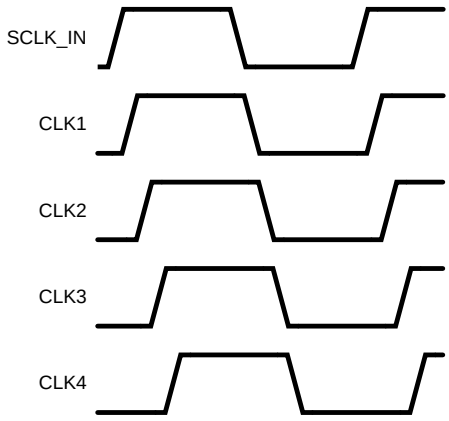


Figure 21. Clock Outputs Timing: With Skew only

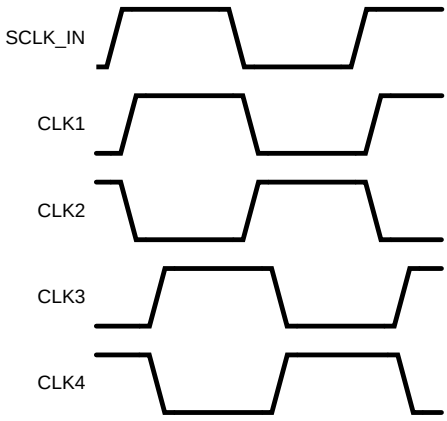


Figure 22. Clock Outputs Timing: With Skew and Inversion

CLOCK REQUEST LOGIC

The clock request logic enables an independent control of the clock tree driver outputs (CLK1 to CLK4) as well as an overall source clock request (SCLK_REQ) and LDO enabling. Since the clock request logic always needs to be active, it is supplied by either the output of the LDO (V_{OUT}) or by the external ENABLE. Further details about the selection between V_{OUT} and ENABLE can be found in the LOW DROPOUT REGULATOR section later in the datasheet.

Clock Request Inputs

A clock request input is provided for each clock output (Figure 23). This allows the peripheral device to control the LMH2190 when it wants to receive a clock. In case the peripheral device does not have clock request functionality, the CLKx_REQ can be wired to a logic high level to enable the clock output (in default register setting). Alternatively, it can be controlled through I^2C. The CLKx_REQ input can be configured to be active high or active low. When the LDO is off, the clock request logic still need to be powered such that it can turn on the LDO. This is why the ENABLE input is used to power the Clock Request Logic in case the LDO is off. Although the CLK_REQ logic is supplied with 1.8V LDO voltage (or ENABLE), the CLKx_REQ input can tolerate voltages up to V_{BAT}.

To prevent glitches on CLK outputs, enabling of the outputs is done synchronously. A latch is used to ensure that the CLK outputs will be enabled on the falling edge of the source clock input (SCLK_IN).

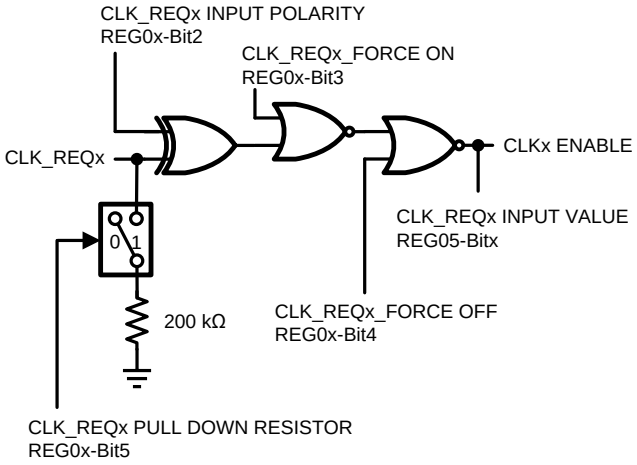


Figure 23. Clock Request Input

System Clock Request Output

In the typical mode of operation, the clock request output will be enabled if one of the 4 CLK_REQ inputs is high (Figure 24). However, this can be overridden via the I^2C interface which has a register bit that forces the output to be enabled, independent of the CLK_REQ input. The polarity of the output can be controlled via I^2C (CLK_REQ Output Polarity) along with whether the output is configured as push/pull, open drain or open source.

For the open drain case, there needs to be an external resistor that pulls the SCLK_REQ to a high level. This high level may be greater than the LDO voltage of 1.8V, but not more than the supply voltage (V_{BAT}) of the LMH2190.

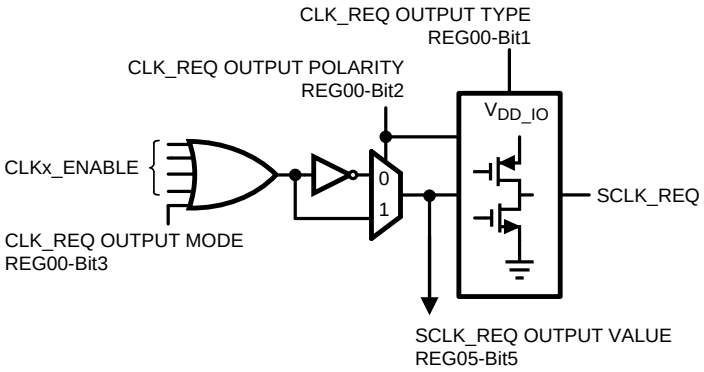


Figure 24. System Clock Request Output

The System Clock Request Output pin can be used to enable or disable an external TCXO to save power consumption. See Figure 25. The LDO powers the TCXO, while the SCLK_REQ enables or disables the TCXO. If the TXCO doesn't have an enable pin, power savings can be realized by switching off the LMH2190's LDO and therewith the TCXO.

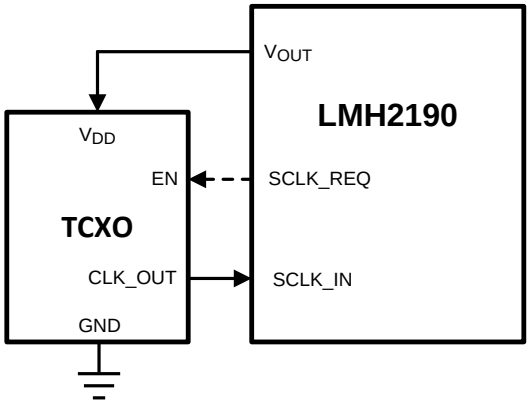


Figure 25. TCXO Powered from LMH2190's LDO

Note that the LMH2190 initializes to its default settings when V_{BAT} is powered-up. As a consequence, the LMH2190 is in it's default state until it is configured through I^2C. Because of this configuration the CLK1/2/3/4 outputs may transmit the clock to a peripheral upon startup when it is not requested by the peripheral and before the device is initialized through the I^2C port. This may happen for instance when the default settings of the device for SCLK_REQ and CLK_REQ1/2/3/4 polarities do not correspond to what is expected by the TCXO and the peripheral. Care must be taken to prevent any unwanted behavior in the peripheral device until the I^2C port correctly configures the device. The setting of the registers is maintained as long as the V_{BAT} voltage is present.

LOW DROPOUT REGULATOR

The linear and low dropout regulator (LDO) is used to regulate the input voltage, V_{BAT}, to generate an accurate 1.8V supply voltage. This allows the LMH2190 to suppress V_{BAT} voltage ripples. A voltage ripple would distort clock edges causing phase noise on the distributed clock signal.

In default mode the LDO is powered-up when one or more Clock Request inputs are high. Therefore the Clock Request Logic needs to be powered continuously such that it can wake-up the LMH2190 and its LDO. The V_{DD_IO} voltage that takes care of supplying the Clock Request Logic can therefore be driven by either the LDO output voltage or the ENABLE signal. Normally the V_{DD_IO} signal is connected to the LDO output, unless the LDO is in a low power shutdown mode. In that case the ENABLE signal will drive V_{DD_IO} (Figure 26). As soon as there is a clock request, the built in LDO will power up and takes over the sourcing of V_{DD_IO} from the ENABLE signal.

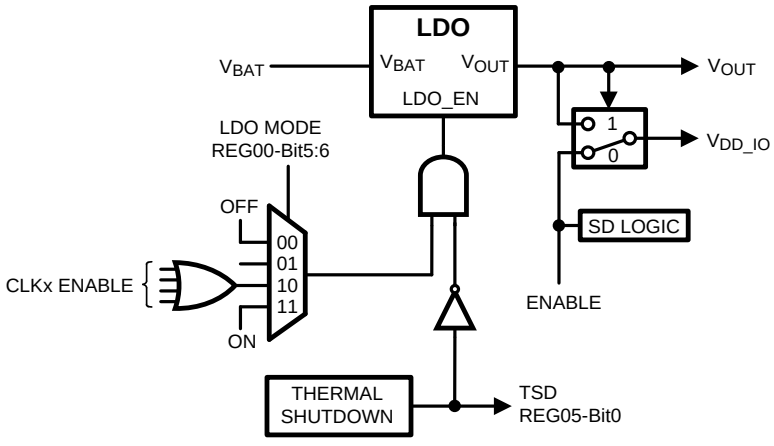


Figure 26. Linear Regulator Block Diagram

The LDO contains thermal overheating detection. If it does overheat, the LMH2190 (except the register logic) will shutdown and sets a status bit in the I^2C status register.

The LDO can be configured to be always ON for the case when it needs to supply power to the TCXO even when the LMH2190 is not requesting any clocks to be distributed.

It is possible to use an external 1.8V supply connected to V_{OUT} and shut off the internal LDO, although it is highly recommended to use the internally generated 1.8V. If an external supply is used, care should be taken during startup as the default configuration is for the internal LDO to be enabled. In this case, there could be contention between the two supplies which could cause excessive current flow.

I²C CONTROL LOGIC

The LMH2190 can be controlled by a I²C host device. The I²C address of the LMH2190 is 38h. It can configure the registers inside the LMH2190 to change the default configuration. The I²C communication is based on a READ/WRITE structure, following the I²C transmission protocol. According to the I²C specification one set of pull-up resistors needs to be present on the I²C bus.

Some of the features are for instance setting the polarity of the clock request inputs and outputs and setting the drive strength of the clock outputs. It also allows direct control of the clock request signals and the LDO via the I²C. The I²C interface is powered by the ENABLE, while the control logic and registers are powered by the V_{BAT}.

I²C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line should only change when SCL is LOW (Figure 27).

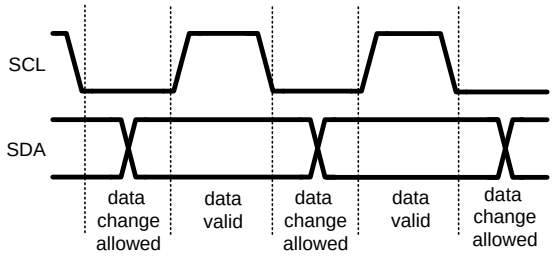


Figure 27. I²C Signals: Data Validity

I²C Start and Stop Condition

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH (Figure 28). STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

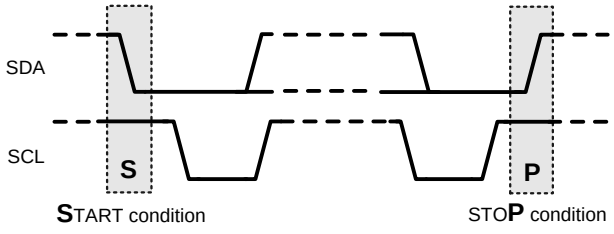


Figure 28. I²C Start and Stop Conditions

Transferring Data

Every frame on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I^2C master sends a chip address (Figure 29). This address is seven bits long followed by an eight bit which is a data direction bit (R/W). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

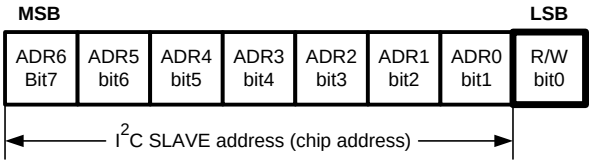


Figure 29. I^2C Chip Address

Register changes take effect at the SCL rising edge during the last ACK from slave. An example of a WRITE cycle is given in Figure 30. When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform (Figure 31).

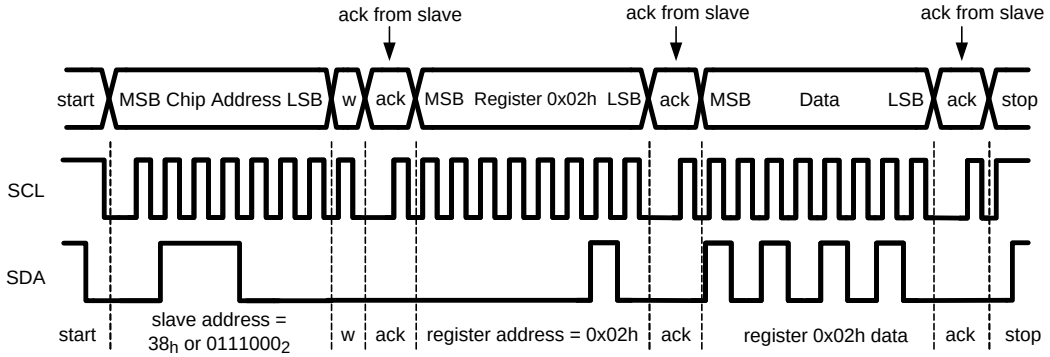


Figure 30. Example I^2C Write Cycle

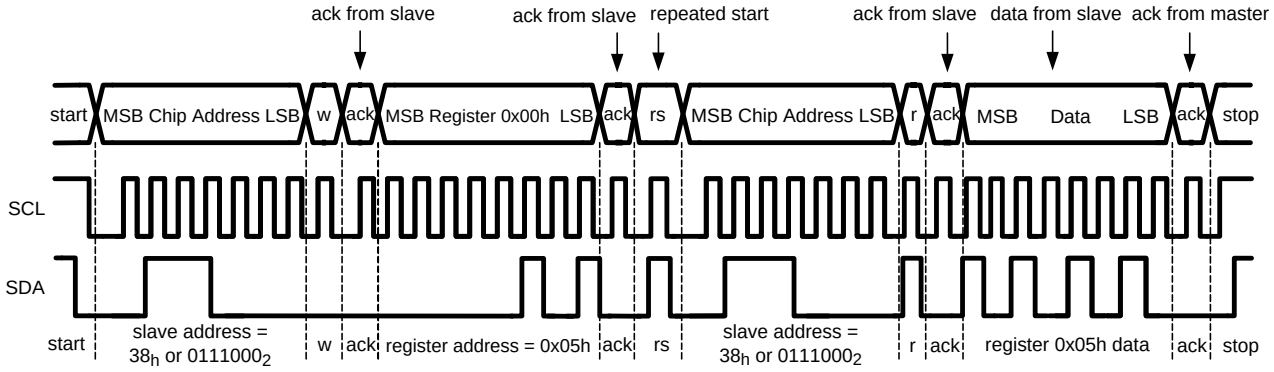


Figure 31. Example I^2C Read Cycle

I^2C Timing

The timing of the SDA and SCL signals is depicted in Figure 32 and the parameters are given in Table 1.

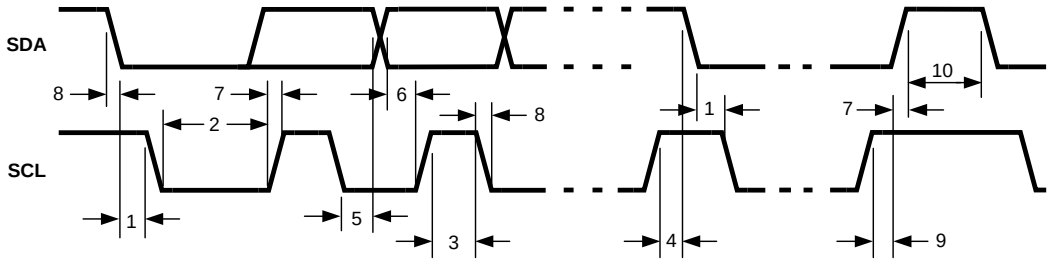


Figure 32. I²C Timing Diagram

Table 1. I²C Timing

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		ns
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LMH2190)	300	900	µs
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20+0.1 C_b	300	ns
8	Fall Time of SDA and SCL	10+0.1 C_b	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

I²C Registers

Table 2. Configuration Register (1)

Field	Bits	Description
Output Mode	[0]	Sets the timing relationship of the clock outputs (Figure 21 and Figure 22). **0 - All 4 outputs are skewed from each other** 1 - Two pair of outputs where one output of the pair is the inversion of the other and the second pair is skewed from the first pair.
Clock Request Output Type	[1]	Sets whether the output is push-pull or open drain. **0 - Push-Pull Output** 1 - Open Drain/Source Output (Open drain with Active low output, Open source with Active high output).
Clock Request Output Polarity	[2]	Sets whether the clock request output is active low or active high. 0 - Active low output **1 - Active high output**
Clock Request Output Mode	[3]	Sets how the clock request output operates. **0 - Use clock request inputs** 1 - Force the clock request output to be asserted.

(1) Address = 00H, type = R/W, reset value = 44H, 0100_0100, Bold face settings are the default configuration.

Table 2. Configuration Register(1) (continued)

Field	Bits	Description
Clock Input Type	[4]	Sets whether the input is AC or DC coupled. **0 - AC coupled** 1 - DC coupled
LDO Mode	[6-5]	Sets the regulator mode of operation. 00 - OFF 01 - Reserved **10 - Track Clock Requests** 11 - Force ON
Reserved	[7]	

Table 3. CLK1 Output Register(1)

Field	Bits	Description
CLK1 Load	[1-0]	Sets the drive strength of the clock output based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10 - 22.5pF to 33.5pF** 11 - 33.5pF to 50pF
CLK_REQ1 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1 - Logic high enables the clock output.**
CLK_REQ1 Force ON Control	[3]	Selects whether to use a clock request or I^2C logic to enable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be enabled (Force ON).
CLK_REQ1 Force OFF Control	[4]	Selects whether to use a clock request or I^2C logic to disable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be disabled (Force OFF). ”Force OFF" overrides ”Force ON".
CLK_REQ1 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0 - No internal pull down resistor is present.** 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

(1) Address = 01H, type = R/W, reset value = 06H, 0000_0110, Bold face settings are the default configuration.

Table 4. CLK2 Output Register(1)

Field	Bits	Description
CLK2 Load	[1-0]	Sets the drive strength of the clock output based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10 - 22.5pF to 33.5pF** 11 - 33.5pF to 50pF
CLK_REQ2 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1 - Logic high enables the clock output.**

(1) Address = 02H, type = R/W, reset value = 06H, 0000_0110, Bold face settings are the default configuration.

Table 4. CLK2 Output Register(1) (continued)

Field	Bits	Description
CLK_REQ2 Force ON Control	[3]	Selects whether to use a clock request or I^2C logic to enable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be enabled (Force ON).
CLK_REQ2 Force OFF Control	[4]	Selects whether to use a clock request or I^2C logic to disable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be disabled (Force OFF). "Force OFF" overrides "Force ON".
CLK_REQ2 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0 - No internal pull down resistor is present.** 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

Table 5. CLK3 Output Register(1)

Field	Bits	Description
CLK3 Load	[1-0]	Sets the drive strength of the clock output based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10 - 22.5pF to 33.5pF** 11 - 33.5pF to 50pF
CLK_REQ3 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1 - Logic high enables the clock output.**
CLK_REQ3 Force ON Control	[3]	Selects whether to use a clock request or I^2C logic to enable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be enabled (Force ON).
CLK_REQ3 Force OFF Control	[4]	Selects whether to use a clock request or I^2C logic to disable the output. **0 - Use the clock request pin to control the output**. 1 - Force the clock output to be disabled (Force OFF). "Force OFF" overrides "Force ON".
CLK_REQ3 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0 - No internal pull down resistor is present.** 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

(1) Address = 03H, type = R/W, reset value = 06H, 0000_0110, Bold face settings are the default configuration.

Table 6. CLK4 Output Register(1)

Field	Bits	Description
CLK4 Load	[1-0]	Sets the drive strength of the clock output based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10 - 22.5pF to 33.5pF** 11 - 33.5pF to 50pF
CLK_REQ4 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1 - Logic high enables the clock output.**
CLK_REQ4 Force ON Control	[3]	Selects whether to use a clock request or I^2C logic to enable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be enabled (Force ON).
CLK_REQ4 Force OFF Control	[4]	Selects whether to use a clock request or I^2C logic to disable the output. **0 - Use the clock request pin to control the output.** 1 - Force the clock output to be disabled (Force OFF). ”Force OFF" overrides ”Force ON".
CLK_REQ4 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0 - No internal pull down resistor is present.** 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

(1) Address = 04H, type = R/W, reset value = 06H, 0000_0110, Bold face settings are the default configuration.

Table 7. Status Register(1)

Field	Bits	Description
Thermal Shutdown (TSD)	[0]	Indicates if a thermal shutdown event has occurred. 0 - Thermal shutdown has not occurred. 1 - Thermal shutdown has occurred
CLK_REQ1 Input Value	[1]	Captures the state of the generated clock request input value. 0 - Generated clock request is low. 1 - Generated clock request is high.
CLK_REQ2 Input Value	[2]	Captures the state of the generated clock request input value. 0 - Generated clock request is low. 1 - Generated clock request is high.
CLK_REQ3 Input Value	[3]	Captures the state of the generated clock request input value. 0 - Generated clock request is low. 1 - Generated clock request is high.
CLK_REQ4 Input Value	[4]	Captures the state of the generated clock request input value. 0 - Generated clock request is low. 1 - Generated clock request is high.
SCLK_REQ Output Value	[5]	Captures the state of the system clock request output value. 0 - System clock request is low. 1 - System clock request is high.
Reserved	[6]	

(1) Address = 05H, type = R

Table 7. Status Register(1) (continued)

Field	Bits	Description
Reserved	[7]	

LAYOUT RECOMMENDATIONS

As with any other device, careful attention must be paid to the board layout. If the board isn't properly designed, the performance of the device can be less than might be expected. Especially the input clock trace (SCLK_IN) and output traces (CLK1/2/3/4) should be as short as possible to reduce the capacitive load observed by the clock outputs. Also proper decoupling close to the device is necessary. Beside a capacitor in the µF range (See Table 8), a capacitor of 100 nF on V_{BAT} and V_{OUT} is recommended close to device. The equivalent series resistance (ESR) of the capacitors should be sufficiently low. A standard capacitor is usually adequate. Advised values are given in Table 8. An evaluation board is available to ease evaluation and demonstrate a proper board layout.

Table 8. Recommended Component Values

Symbol	Parameter	Min	Typ	Max	Units
C_{BAT}(1)	Capacitor on V_{BAT}	0.47	1		µF
C_{OUT}(1)	Capacitor on V_{OUT}	1	2.2		
ESR	Equivalent Series Resistance	5		500	mΩ
C_{SCLK_IN}	Input AC Coupling Capacitor	330	470	10000	pF

(1) C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCC's) used in setting electrical characteristics.

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH2190TM-38/NOPB	ACTIVE	DSBGA	YFQ	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-20 to 85	AA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

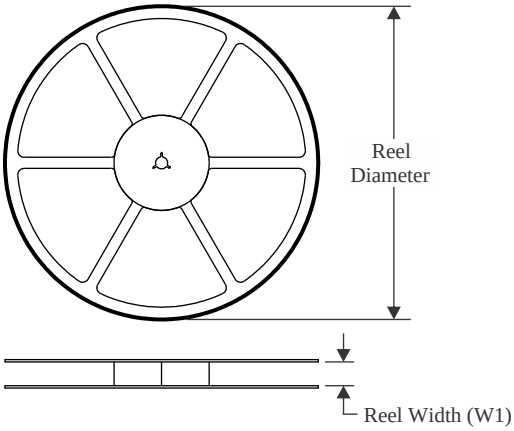
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

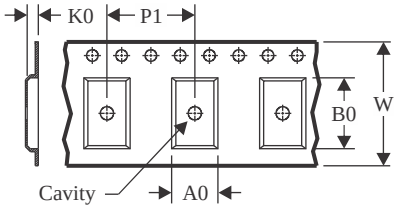
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

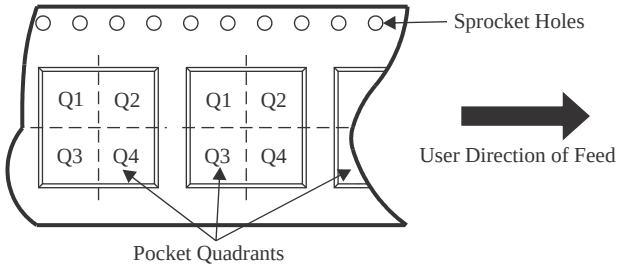


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

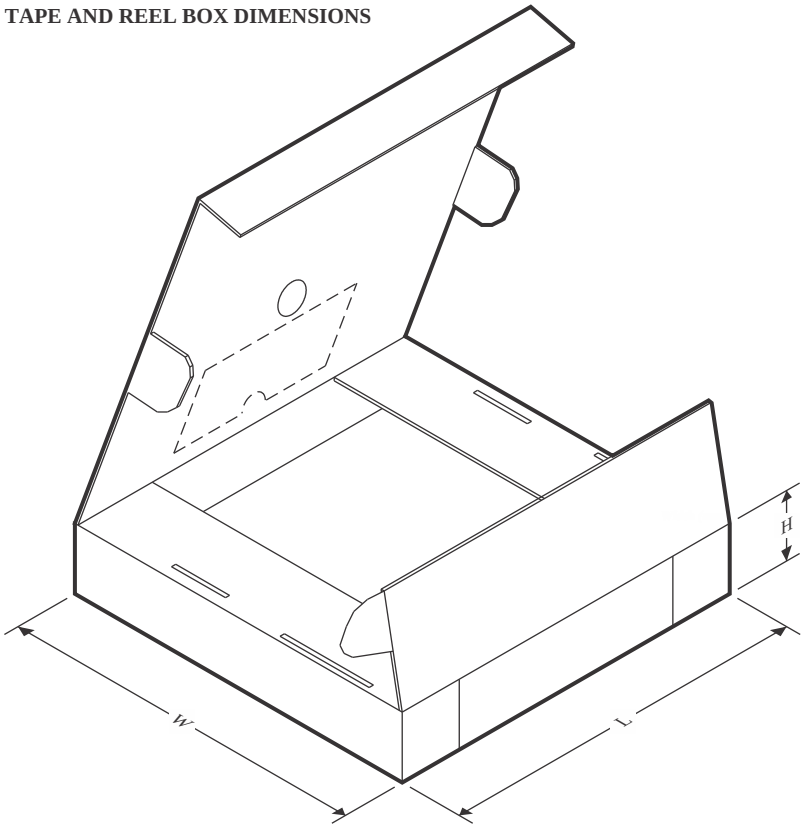
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH2190TM-38/NOPB	DSBGA	YFQ	16	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

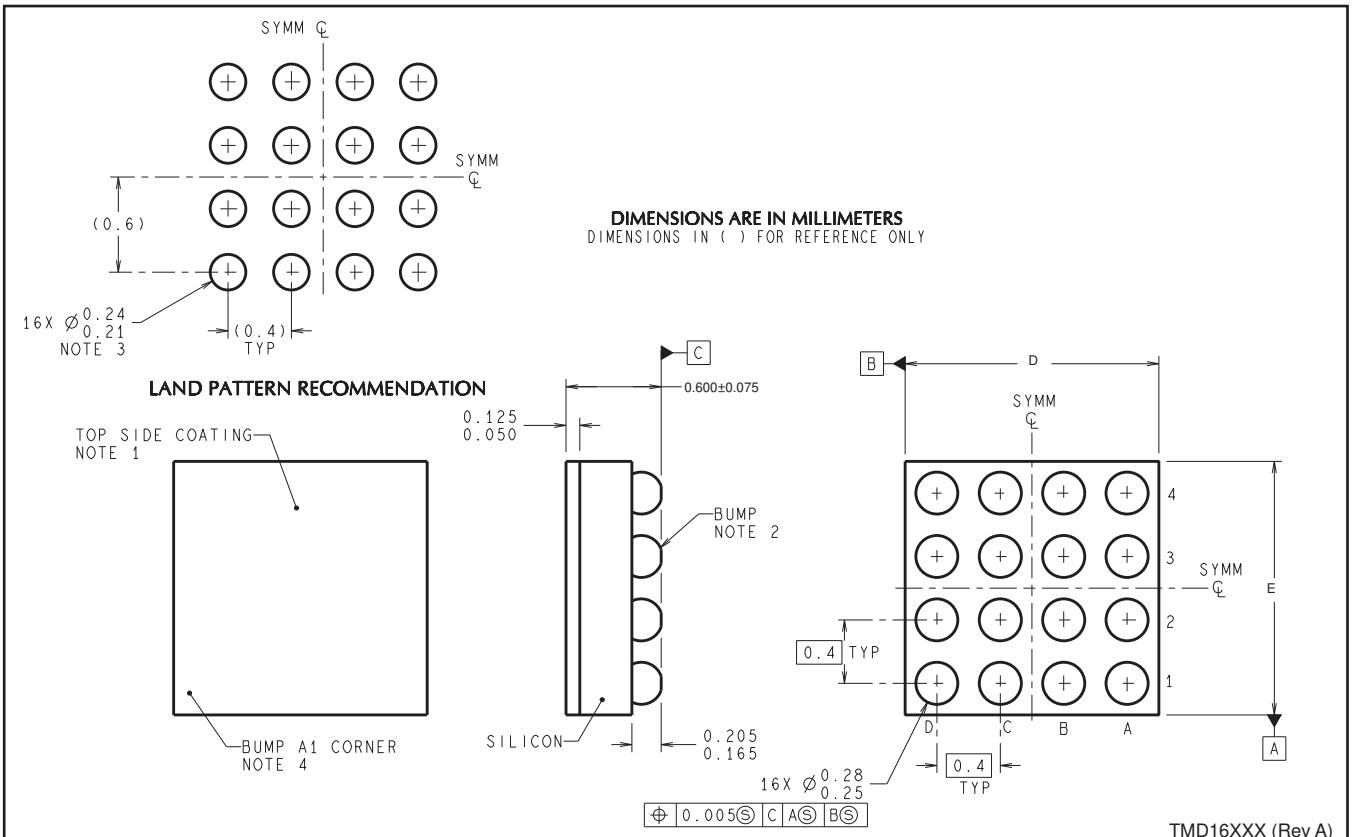
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH2190TM-38/NOPB	DSBGA	YFQ	16	250	208.0	191.0	35.0

YFQ0016



D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.64 mm, Min = 1.58 mm

4215081/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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