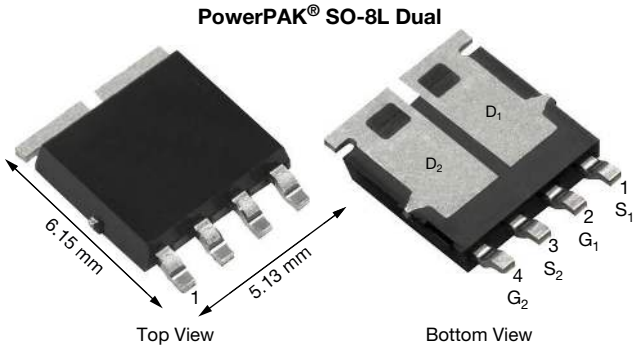
Automotive N- and P-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Dual



Top View Bottom View

FEATURES

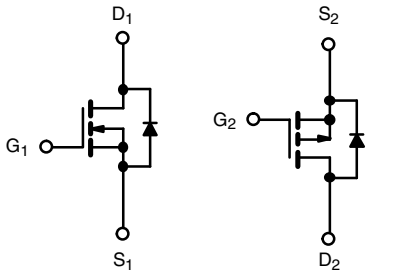
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET P-Channel MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	40	-40
$R_{DS(on)}$ (Ω) at V_{GS} = ± 10 V	0.0075	0.0170
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.0110	0.0230
I_D (A)	30	-30
Configuration	N- and p-pair	
Package		

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ504EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V_{DS}	40	-40	V
Gate-source voltage		V_{GS}	± 20		
Continuous drain current	T_C = 25 °C	I_D	30 [a]	-30 [a]	A
	T_C = 125 °C		29.3	-19.5	
Continuous source current (diode conduction) [a]		I_S	30	-30	
Pulsed drain current [b]		I_{DM}	90	-84	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	25	-24	
Single pulse avalanche Energy		E_{AS}	31.2	28.8	mJ
Maximum power dissipation [b]	T_C = 25 °C	P_D	34	34	W
	T_C = 125 °C		11	11	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	85	85	°C/W
Junction-to-case (drain)		R_{thJC}	4.3	4.3	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)								
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static								
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		N-Ch	40	-	-	V
		V_{GS} = 0 V, I_D = -250 µA		P-Ch	-40	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		N-Ch	1.5	2	2.5	
		V_{DS} = V_{GS}, I_D = -250 µA		P-Ch	-1.5	-2	-2.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	N-Ch	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = -40 V	P-Ch	-	-	-1	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	N-Ch	-	-	50	
		V_{GS} = 0 V	V_{DS} = -40 V, T_J = 125 °C	P-Ch	-	-	-50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	N-Ch	-	-	150	
		V_{GS} = 0 V	V_{DS} = -40 V, T_J = 175 °C	P-Ch	-	-	-150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	N-Ch	10	-	-	A
		V_{GS} = -10 V	V_{DS} ≤ 5 V	P-Ch	-10	-	-	
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 8 A	N-Ch	-	0.0061	0.0075	Ω
		V_{GS} = -10 V	I_D = -8 A	P-Ch	-	0.0138	0.0170	
		V_{GS} = 10 V	I_D = 8 A, T_J = 125 °C	N-Ch	-	-	0.0110	
		V_{GS} = -10 V	I_D = -8 A, T_J = 125 °C	P-Ch	-	-	0.0254	
		V_{GS} = 10 V	I_D = 8 A, T_J = 175 °C	N-Ch	-	-	0.0130	
		V_{GS} = -10 V	I_D = -8 A, T_J = 175 °C	P-Ch	-	-	0.0304	
		V_{GS} = 4.5 V	I_D = 5 A	N-Ch	-	0.0088	0.0110	
		V_{GS} = -4.5 V	I_D = -5 A	P-Ch	-	0.0186	0.0230	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 8 A		N-Ch	-	35	-	S
		V_{DS} = -15 V, I_D = -8 A		P-Ch	-	30	-	
Dynamic [b]								
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch	-	1355	1900	pF
		V_{GS} = 0 V	V_{DS} = -25 V, f = 1 MHz	P-Ch	-	3340	4600	
Output capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch	-	875	1400	
		V_{GS} = 0 V	V_{DS} = -25 V, f = 1 MHz	P-Ch	-	230	320	
Reverse transfer capacitance	C_{rss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch	-	35	50	
		V_{GS} = 0 V	V_{DS} = -25 V, f = 1 MHz	P-Ch	-	216	300	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 5 A	N-Ch	-	18	30	nC
		V_{GS} = -10 V	V_{DS} = -20 V, I_D = -5 A	P-Ch	-	56	85	
Gate-source charge [c]	Q_{gs}	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 5 A	N-Ch	-	3.5	-	
		V_{GS} = -10 V	V_{DS} = -20 V, I_D = -5 A	P-Ch	-	8.5	-	
Gate-drain charge [c]	Q_{gd}	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 5 A	N-Ch	-	2.6	-	
		V_{GS} = -10 V	V_{DS} = -20 V, I_D = -5 A	P-Ch	-	9.9	-	
Gate resistance	R_g	f = 1 MHz		N-Ch	0.3	0.72	1.2	Ω
				P-Ch	1.15	2.37	3.6	

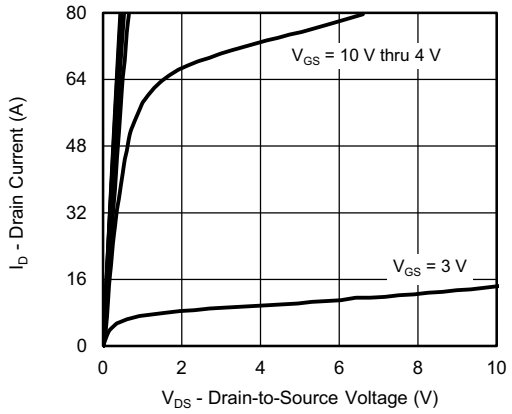
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 4 Ω, $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	11	20	ns
		V_{DD} = -20 V, R_L = 4 Ω, $I_D \cong$ -5 A, V_{GEN} = -10 V, R_g = 1 Ω	P-Ch	-	15	25	
Rise time [c]	t_r	V_{DD} = 20 V, R_L = 4 Ω, $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	4	10	
		V_{DD} = -20 V, R_L = 4 Ω, $I_D \cong$ -5 A, V_{GEN} = -10 V, R_g = 1 Ω	P-Ch	-	6	10	
Turn-off delay time [c]	$t_{d(off)}$	V_{DD} = 20 V, R_L = 4 Ω, $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	21	35	
		V_{DD} = -20 V, R_L = 4 Ω, $I_D \cong$ -5 A, V_{GEN} = -10 V, R_g = 1 Ω	P-Ch	-	45	70	
Fall time [c]	t_f	V_{DD} = 20 V, R_L = 4 Ω, $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	5	10	
		V_{DD} = -20 V, R_L = 4 Ω, $I_D \cong$ -5 A, V_{GEN} = -10 V, R_g = 1 Ω	P-Ch	-	7	12	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}		N-Ch	-	-	90	A
			P-Ch	-	-	-84	
Forward voltage	V_{SD}	I_S = 8 A, V_{GS} = 0 V	N-Ch	-	0.803	1.2	V
		I_S = -8 A, V_{GS} = 0 V	P-Ch	-	-0.790	-1.2	
Body diode reverse recovery time	t_{rr}	I_F = 5 A, di/dt = 100 A/µs	N-Ch	-	48	100	ns
		I_F = -5 A, di/dt = 100 A/µs	P-Ch	-	26	55	
Body diode reverse recovery charge	Q_{rr}	I_F = 5 A, di/dt = 100 A/µs	N-Ch	-	54	110	nC
		I_F = -5 A, di/dt = 100 A/µs	P-Ch	-	22	45	
Reverse recovery fall time	t_a	I_F = 5 A, di/dt = 100 A/µs	N-Ch	-	25	-	ns
		I_F = -5 A, di/dt = 100 A/µs	P-Ch	-	15	-	
Reverse recovery rise time	t_b	I_F = 5 A, di/dt = 100 A/µs	N-Ch	-	23	-	
		I_F = -5 A, di/dt = 100 A/µs	P-Ch	-	11	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$	I_F = 5 A, di/dt = 100 A/µs	N-Ch	-	-2.1	-	A
		I_F = -5 A, di/dt = 100 A/µs	P-Ch	-	-1.7	-	

Notes

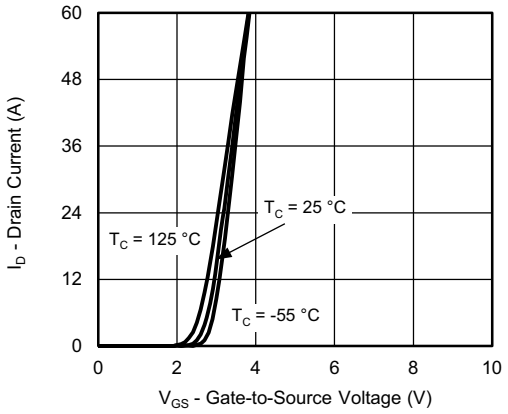
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

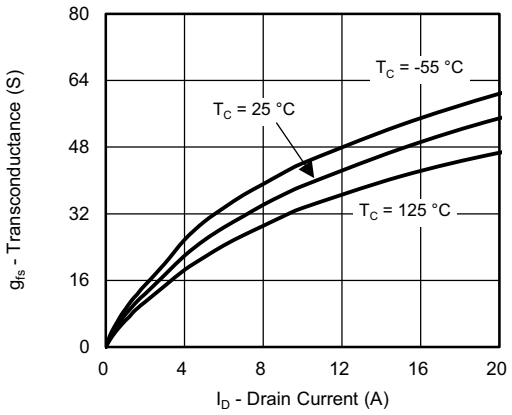
N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



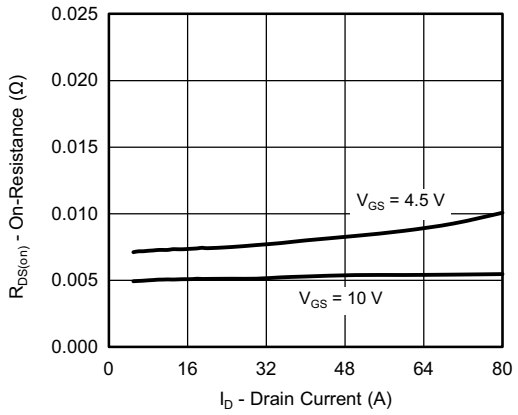
Output Characteristics



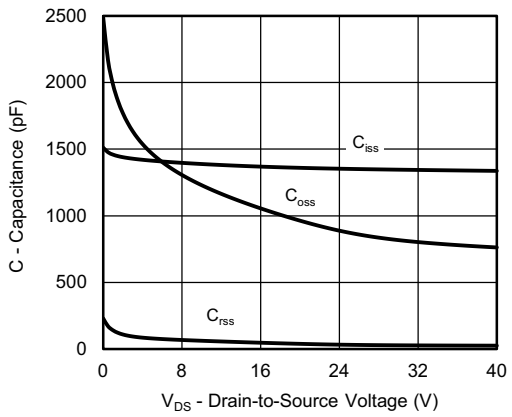
Transfer Characteristics



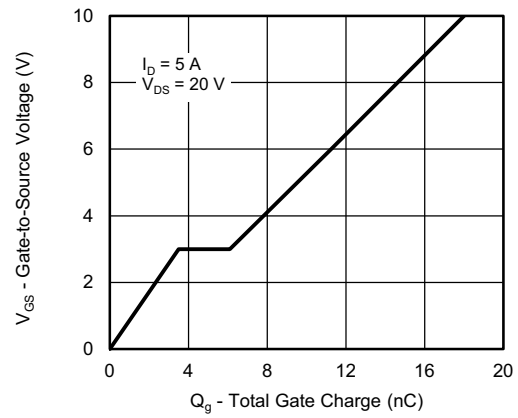
Transconductance



On-Resistance vs. Drain Current

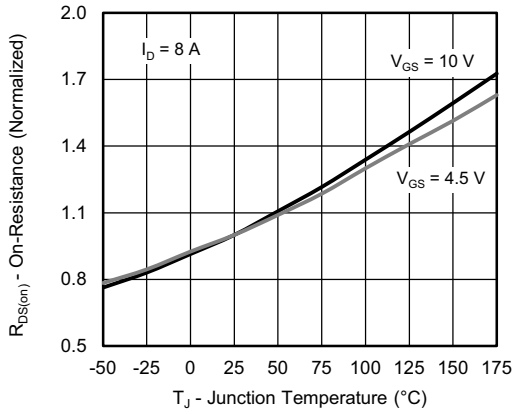


Capacitance

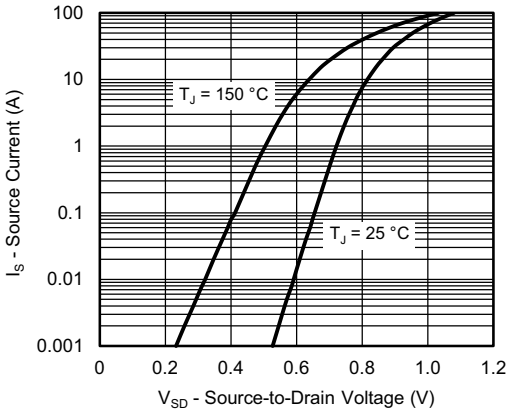


Gate Charge

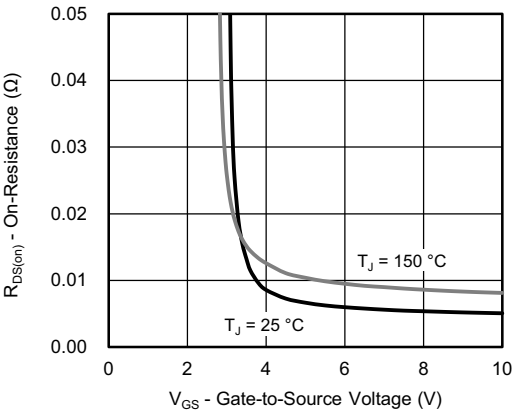
N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



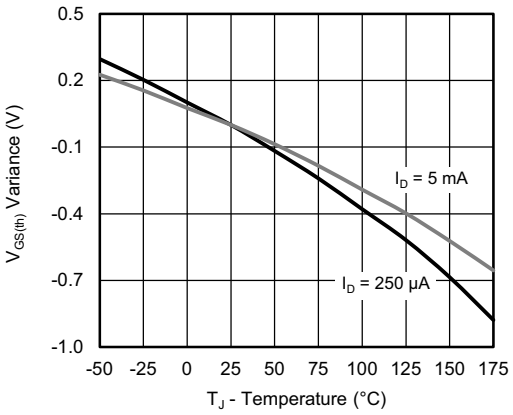
On-Resistance vs. Junction Temperature



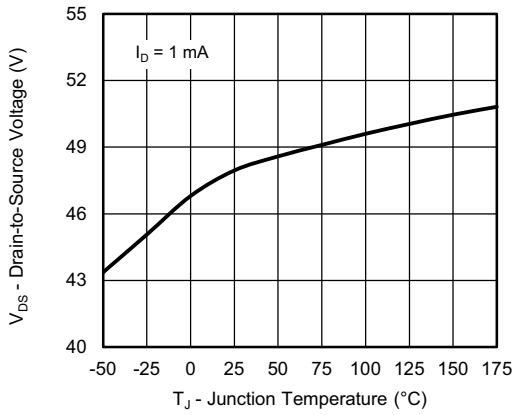
Source Drain Diode Forward Voltage



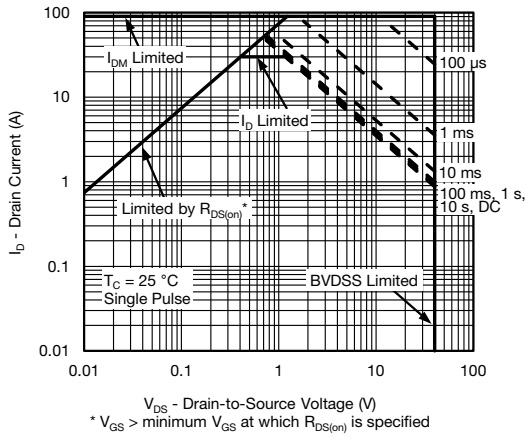
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

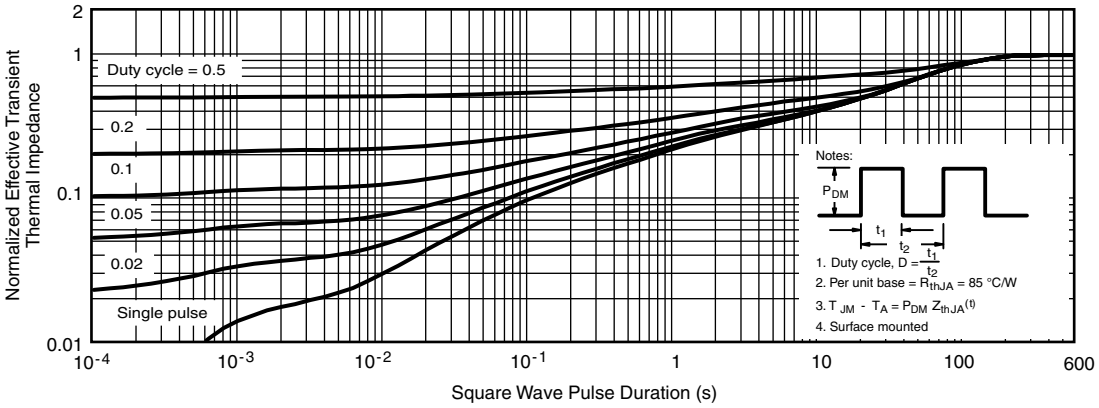


Drain Source Breakdown vs. Junction Temperature

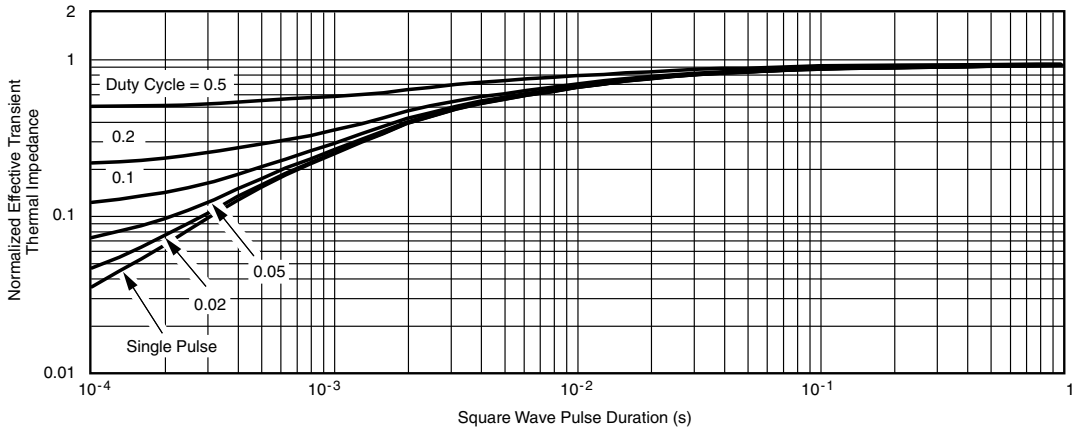


Safe Operating Area

N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



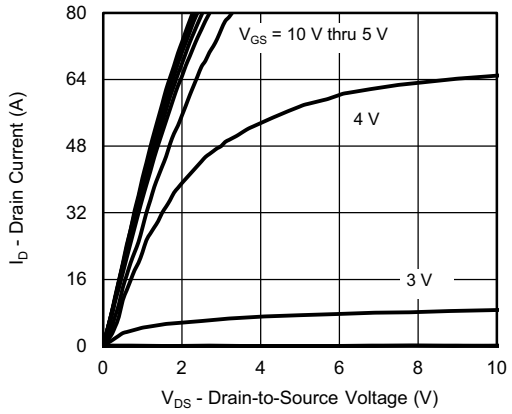
Normalized Thermal Transient Impedance, Junction-to-Case

Note

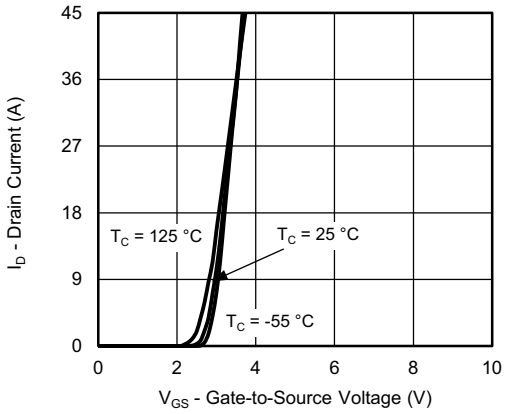
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

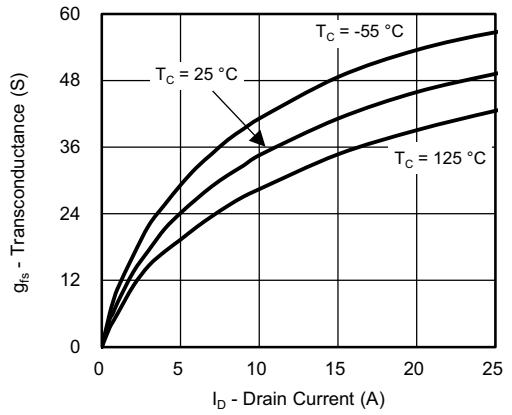
P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



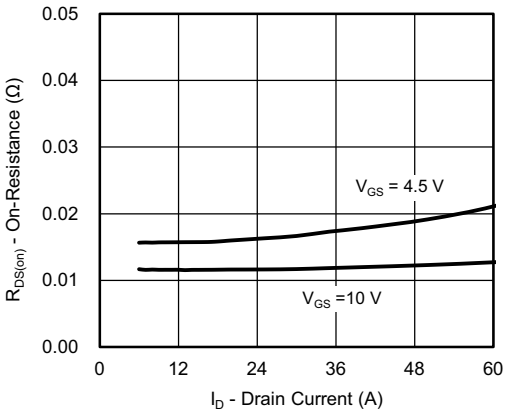
Output Characteristics



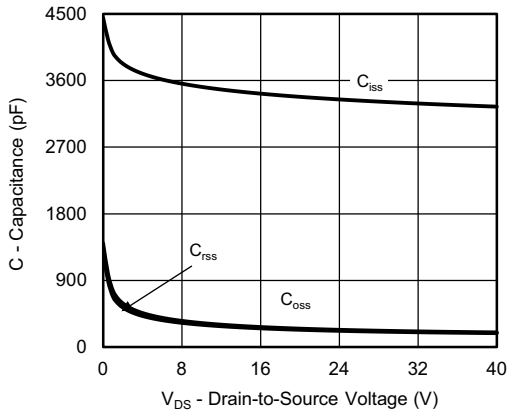
Transfer Characteristics



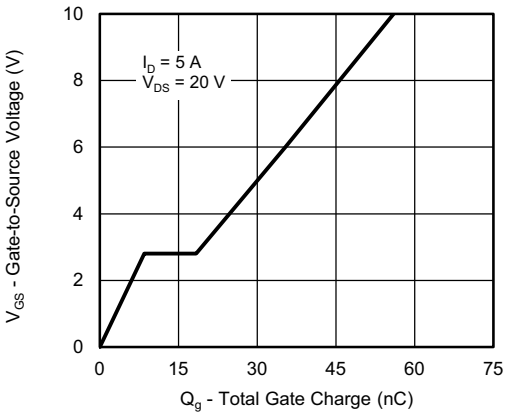
Transconductance



On-Resistance vs. Drain Current

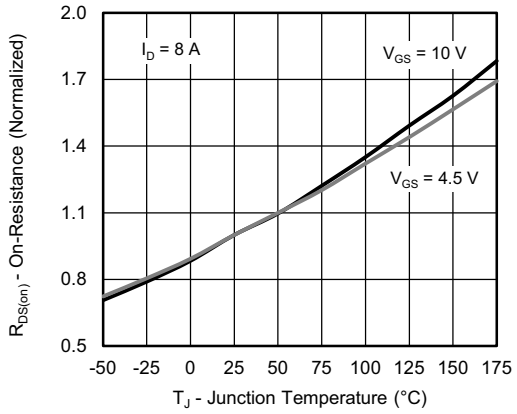


Capacitance

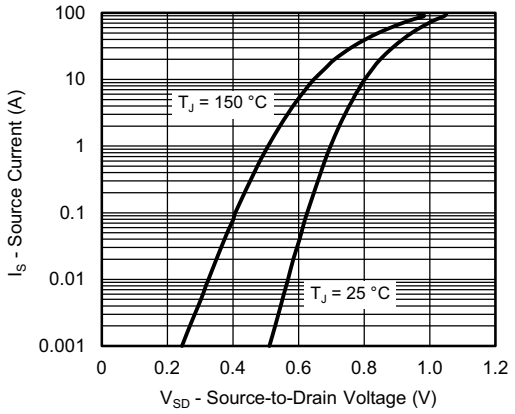


Gate Charge

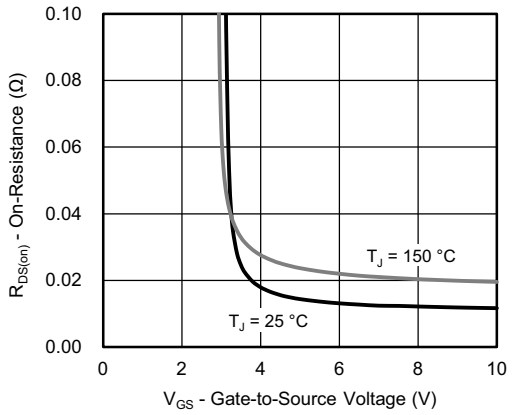
P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



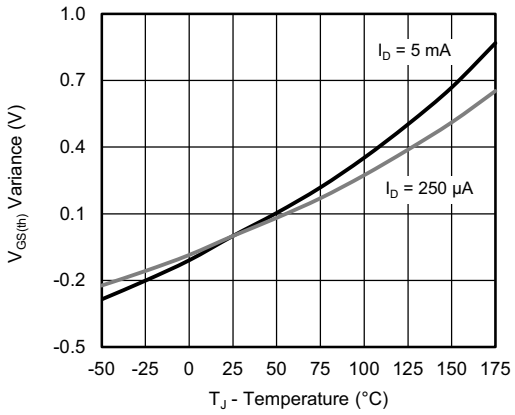
Threshold Voltage



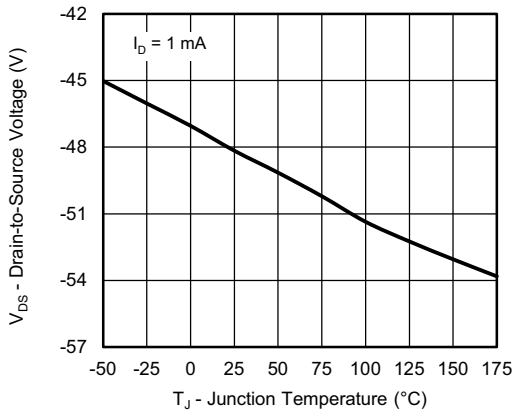
Source Drain Diode Forward Voltage



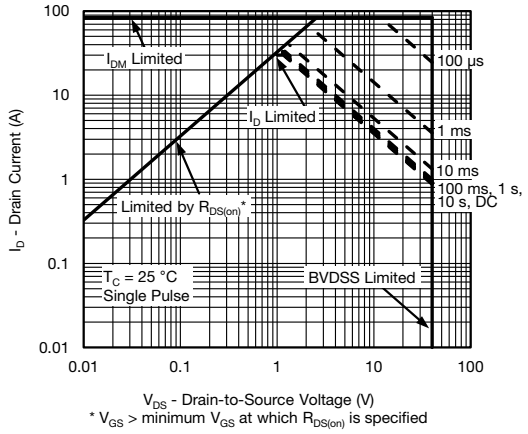
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

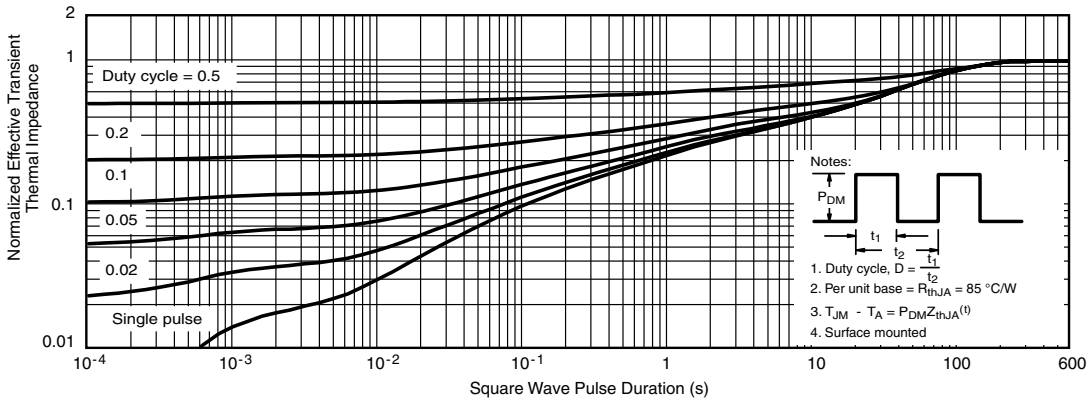


Drain Source Breakdown vs. Junction Temperature

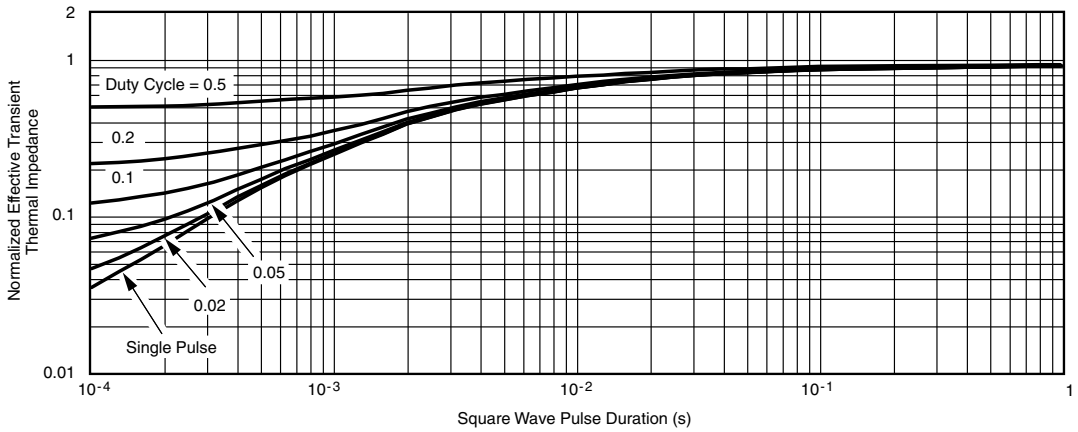


Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

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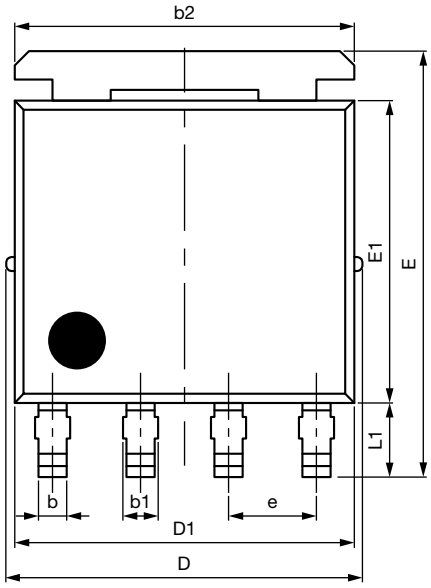
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

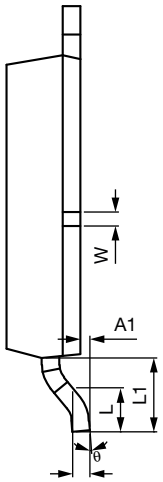
  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76029.

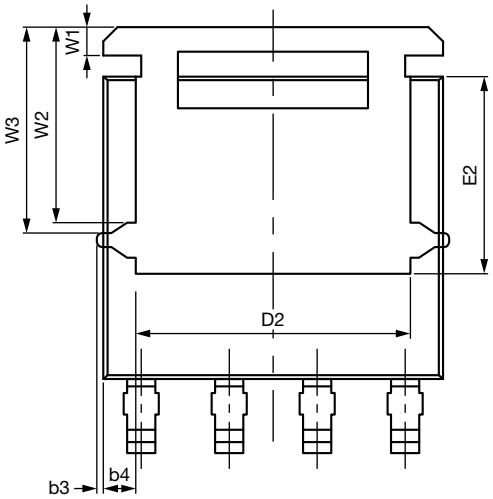
PowerPAK® SO-8L Case Outline 2



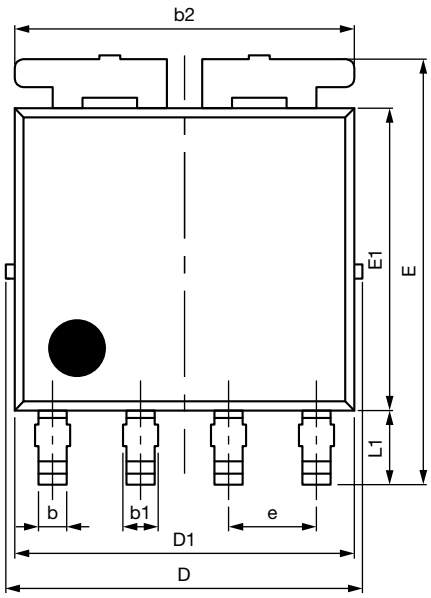
Topside view (single)



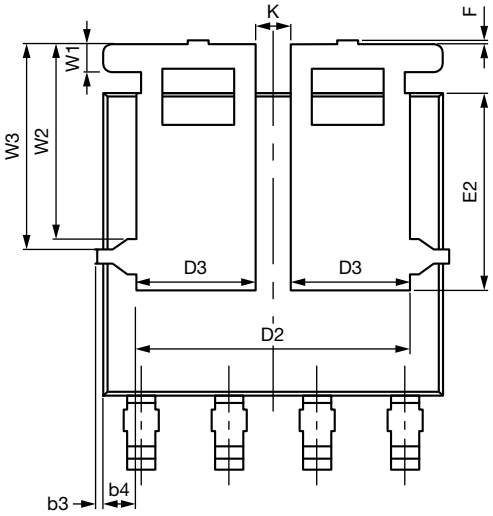
0.25 gauge line



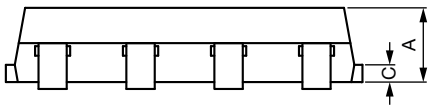
Backside view (single)



Topside view (dual)



Backside view (dual)

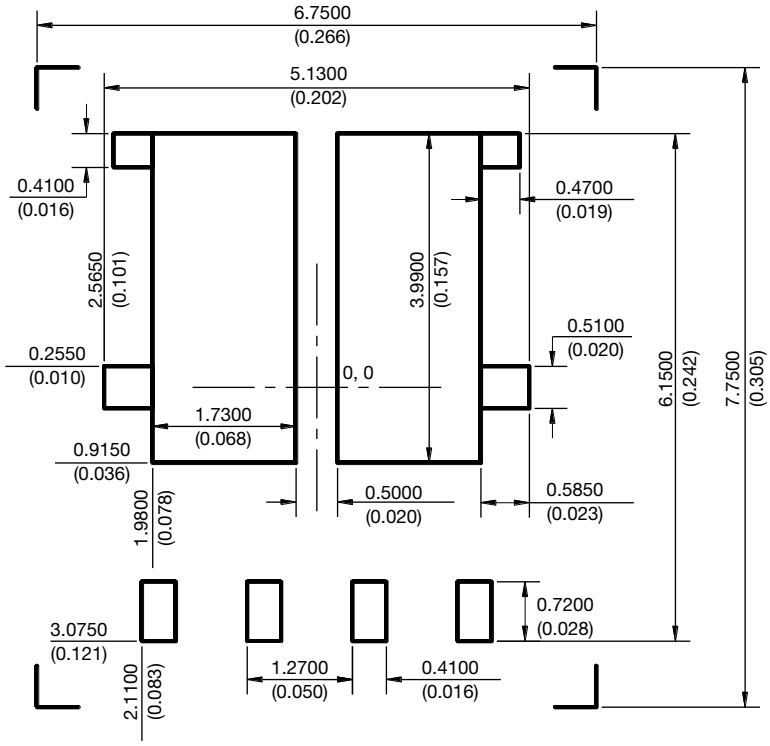


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C21-1498-Rev. C, 01-Nov-2021 DWG: 6044						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads
Dimensions in mm (inches)
Keep-out 6.75 (0.266) x 7.75 (0.305)

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