C8051F996-GDI

Tested Ultra-Low-Power 8 kB Flash Capacitive Sensing MCU Die in Wafer Form

Ultra Low Power Consumption
- 150 µA/MHz in active mode (24.5 MHz clock)
- 2 µs wakeup time
- 10 nA sleep mode with memory retention
- 50 nA sleep mode with brownout detector
- 300 nA sleep mode with LFO
- 600 nA sleep mode with external crystal

Supply Voltage 1.8 to 3.6 V
- Built-in LDO regulator allows a high analog supply voltage and low digital core voltage
- 2 built-in supply monitors (brownout detector) for sleep mode and active modes

12-Bit or 10-Bit Analog to Digital Converter
- ±1 LSB INL (10-bit mode); ±1.5 LSB INL (12-bit mode) no missing codes
- Programmable throughput up to 300 ksps (10-bit mode) or 75 ksps (12-bit mode)
- 10 external inputs
- On-chip voltage reference; 0.5x gain allows measuring voltages up to twice the reference voltage
- 16-bit auto-averaging accumulator with burst mode provides increased ADC resolution
- Data dependent windowed interrupt generator
- Built-in temperature sensor

Capacitive Sense Interface
- Supports buttons, sliders, wheels, and capacitive proximity sensing
- Fast 40 µs per channel conversion time
- 16-bit resolution, 14 input channels
- Auto scan and wake-on-touch
- Auto-accumulate up to 64x samples

Analog Comparator
- Programmable hysteresis and response time
- Configurable as wake-up or reset source

6-Bit Programmable Current Reference
- Up to ±500 µA, can be used as a bias or for generating a custom reference voltage
- PWM enhanced resolution mode

High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to **25 MIPS** throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 512 bytes RAM
- 8 kB Flash; in-system programmable

Digital Peripherals
- 17 port I/O; high sink current and programmable drive strength

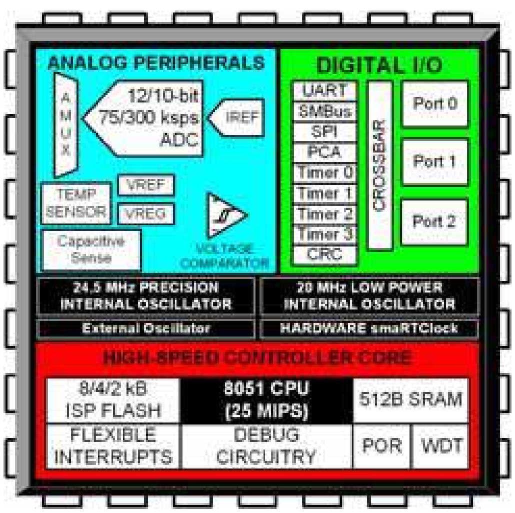
  Hardware SMBus™/I^{2}C™, SPI™, and UART serial ports available concurrently
- Four general purpose 16-bit counter/timers
- Programmable 16-bit counter/timer array with three capture/compare modules and watchdog timer

Clock Sources
- Internal oscillators: 24.5 MHz, 2% accuracy supports UART operation; 20 MHz low power oscillator requires very little bias current.
- External oscillator: Crystal, RC, C, or CMOS Clock
- SmaRTClock oscillator: 32 kHz Crystal or internal
- Can switch between clock sources on-the-fly; useful in implementing various power saving modes

On-Chip Debug
- On-chip debug circuitry facilitates full-speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory and registers
- Complete development kit

Temperature Range: –40 to +85 °C

Full Technical Data Sheet
- C8051F99x-C8051F98x



1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (Bytes)	SmaRTClock Real Time Clock	SMBus/I^{2}C, UART, Enhanced SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	Analog-to-Digital Converter Inputs	ADC with Internal Voltage Reference and Temperature Sensor	Capacitive Touch (QuickSense™) Inputs	Programmable Current Reference	Analog Comparators	Unique Identifier (UID)	Wafer Thickness
C8051F996-C-G1DI	25	8	512	✓	✓	4	✓	17	10	12-bit	14	✓	1		28.54 mil / 725 µm (no back-grind)
C8051F996-C-GDI	25	8	512	✓	✓	4	✓	17	10	12-bit	14	✓	1		12 mil (back-grind)
C8051F996-C1-G1DI*	25	8	512	✓	✓	4	✓	17	10	12-bit	14	✓	1	✓	28.54 mil / 725 µm (no back-grind)
C8051F996-C1-GDI*	25	8	512	✓	✓	4	✓	17	10	12-bit	14	✓	1	✓	12 mil (back-grind)

***Note:** This part is obsolete.

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2. Pad Definitions

Table 2.1 lists the pad definitions for the C8051F996-GDI. For a full description of each pad, refer to the C8051F99x-C8051F98x data sheet.

Table 2.1. Pad Definitions for the C8051F996-GDI

Name	Physical Pad Number	Type	Description
V_{DD}	3	P In	Power Supply Voltage. Must be 1.8 to 3.6 V.
GND	2	G	Required Ground.
$\overline{RST}$/ C2CK	6	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. A 1 kΩ to 5 kΩ pullup to V_{DD} is recommended. Clock signal for the C2 Debug Interface.
P2.7/ C2D	7	D I/O D I/O	Port 2.7. This pin can only be used as GPIO. The Crossbar cannot route signals to this pin and it cannot be configured as an analog input. Bi-directional data signal for the C2 Debug Interface.
P1.6/ XTAL3	9	D I/O A In	Port 1.6. SmaRTClock Oscillator Crystal Input.
P1.7/ XTAL4	8	D I/O A Out	Port 1.7. SmaRTClock Oscillator Crystal Output.
P0.0/ V_{REF}	1	D I/O or A In A In	Port 0.0. External V_{REF} Input.
P0.1/ AGND	25	D I/O or A In G	Port 0.1. Optional Analog Ground.
P0.2/ XTAL1/ RTCOUT	24	D I/O or A In A In D Out	Port 0.2. External Clock Input. This pin is the external oscillator return for a crystal or resonator. Buffered SmaRTClock oscillator output.

Table 2.1. Pad Definitions for the C8051F996-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.3/	23	D I/O or A In	Port 0.3.
XTAL2/		A Out	External Clock Output. This pin is the excitation driver for an external crystal or resonator.
		D In	External Clock Input. This pin is the external clock input in external CMOS clock mode.
		A In	External Clock Input. This pin is the external clock input in capacitor or RC oscillator configurations.
WAKEOUT		D Out	Wake-up request signal to wake up external devices.
P0.4/	22	D I/O or A In	Port 0.4.
TX		D Out	UART TX Pin.
P0.5/	21	D I/O or A In	Port 0.5.
RX		D In	UART RX Pin.
P0.6/	20	D I/O or A In	Port 0.6.
CNVSTR		D In	External Convert Start Input for ADC0.
P0.7/	19	D I/O or A In	Port 0.7.
IREF0		A Out	IREF0 Output.
P1.0	16	D I/O or A In	Port 1.0. May also be used as SCK for SPI1.
CP0+		A In	Comparator0 positive input.
P1.1	14	D I/O or A In	Port 1.1.
CP0-		A In	Comparator0 negative input.
P1.2	13	D I/O or A In	Port 1.2.
P1.3	12	D I/O or A In	Port 1.3.

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Table 2.1. Pad Definitions for the C8051F996-GDI (Continued)

Name	Physical Pad Number	Type	Description
P1.4	11	D I/O or A In	Port 1.4.
P1.5	10	D I/O or A In	Port 1.5.

3. Bonding Instructions

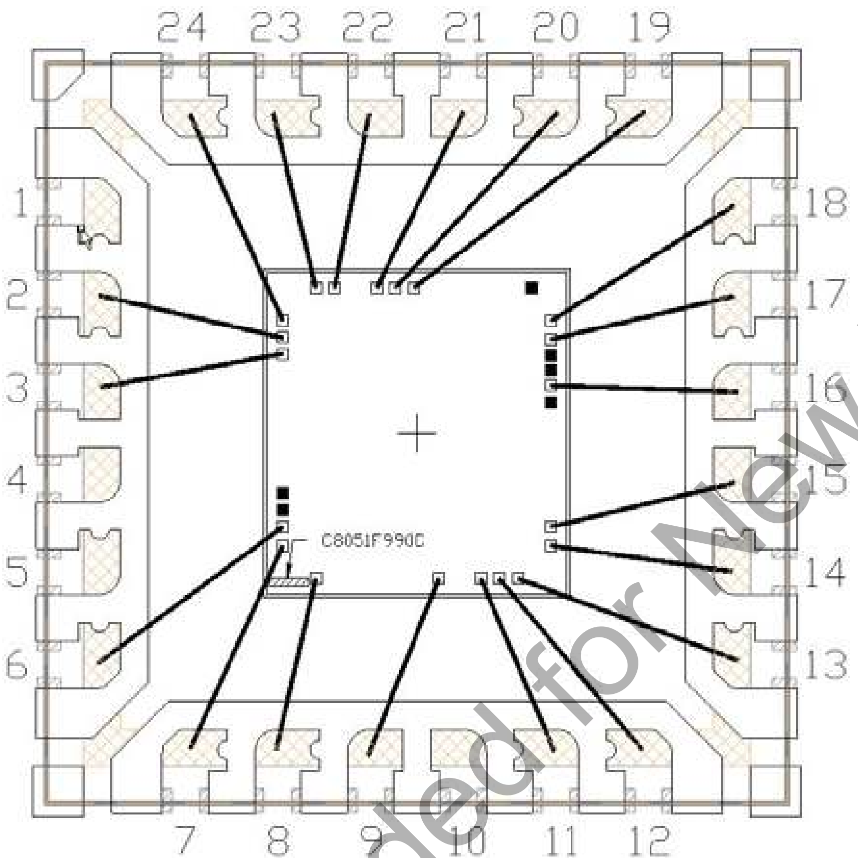

Figure 3.1. Die Bonding (QFN-24)

Table 3.1. Bond Pad Coordinates (Relative to Center of Die)

Physical Pad Number	Example Package Pin Number (QFN-24)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
1	24	P0.0/VREF	–724	606
	1	NC		
2	2	GND	–724	515
3	3	VDD	–724	429
4	Reserved	—	–724	–322
5	Reserved	—	–724	–413
6	6	/RST/C2CK	–724	–506
7	7	P2.7/C2D	–724	–606
8	8	P1.7/XTAL4	–545	–785
***Note:** Pins marked “Reserved” should not be connected.				

Table 3.1. Bond Pad Coordinates (Relative to Center of Die) (Continued)

Physical Pad Number	Example Package Pin Number (QFN-24)	Package Pin Name	Physical Pad X (µm)	Physical Pad Y (µm)
9	9	P1.6/XTAL3	117	–785
	10	NC		
10	11	P1.5	345	–785
11	12	P1.4	445	–785
12	13	P1.3	545	–785
13	14	P1.2	724	–606
14	15	P1.1/CP0–	724	–506
15	Reserved	—	724	168
16	16	P1.0/CP0+	724	256
17	Reserved	—	724	343
18	Reserved	—	724	418
19	17	P0.7/IREF0	724	506
20	18	P0.6/CNVSTR	724	606
21	Reserved	—	618	785
22	19	P0.5/RX	–17	785
23	20	P0.4/TX	–117	785
24	21	P0.3/XTAL2	–217	785
25	22	P0.2/XTAL1	–445	785
26	23	P0.1/AGND	–545	785
***Note:** Pins marked "Reserved" should not be connected.				

Table 3.2. Wafer and Die Information

Wafer ID	C8051F990C
Wafer Dimensions	8 in
Die Dimensions	1.65 mm x 1.78 mm
Wafer Thickness (no backgrind)	28.54 mil ±1 mil (725 µm)
Wafer Thickness (with backgrind)	12 mil ±1 mil
Wafer Identification	Notch
Scribe Line Width	80 µm
Die Per Wafer*	Contact Sales for info
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	60 µm x 60 µm
Maximum Processing Temperature	250 °C
Electronic Die Map Format	.txt
Bond Pad Pitch Minimum	75 µm
***Note:** This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

4. Determining the Device Part Number at Run Time

In many applications, user software may need to determine the MCU part number at run time in order to determine the hardware capabilities. The part number can be determined by reading the value of the DEVICEID Special Function Register. The value of the DEVICEID register can be decoded as follows:

0xD6—C8051F996-C
0xE6—C8051F996-C1

SFR Definition 4.1. DEVICEID: Device Identification

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xE3

Bit	Name	Function
7:0	DEVICEID[7:0]	**Device Identification.** These bits contain a value that can be decoded to determine the device part number.

5. Unique Identifier (UID)

The C8051F996-C1 has a pre-programmed 32-bit (4-byte) Unique Identifier (UID). The UID resides in the last four bytes of XRAM. The UID can be read by firmware using MOVX instructions and through the debug port.

Firmware can overwrite the UID during normal operation, and the bytes in memory will be automatically reinitialized with the factory-programmed UID value after any device reset. Firmware using this area of memory should always initialize the memory to a known value, as any previous data stored at these locations will be overwritten and not retained through a reset.

Table 5.1. UID Implementation Information

Device	External Memory (XRAM) Addresses
C8051F996-C1	**(MSB)** 0x00FF, 0x00FE, 0x00FD, 0x00FC **(LSB)**

6. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).

7. Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet this requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, undergone backgrinding or are on tape. Initial response time for FA requests that meet this requirements will be 3 weeks.

Document Change List

Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 8.

Revision 1.1 to Revision 1.2

- Removed C8051F996-G1DI and C8051F996-GDI rows from Table 1.1.
- Changed “Package” column heading to “Wafer Thickness” in Table 1.1.
- Added “Unique Identifier” column to Table 1.1.
- Updated Wafer ID in Table 3.2.
- Updated Table 3.2 with new Wafer Thickness (no backgrind) row.
- Added “with backgrind” to existing Wafer Thickness row in Table 3.2.
- Changed “C8051F996-B1” to “C8051F996-C” throughout.
- Added “4. Determining the Device Part Number at Run Time” on page 9.
- Added “5. Unique Identifier (UID)” on page 9.
- Added “7. Failure Analysis (FA) Guidelines” on page 10.

Revision 1.2 to Revision 1.3

- Updated “Table 1.1. Product Selection Guide” on page 2 to note obsolete parts.

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