

## TA9110K – 6W CW, 30 - 4000MHz GaN Power Transistor

### 1.0 Features

- Small signal gain @ 1000MHz: 17dB
- Large signal gain @ 1000MHz: 14dB
- PSAT @ 1000MHz: 40dBm
- PAE @ PSAT @ 1000MHz: 55%
- 28V – 32V Typical operation
- Operating frequency: 30MHz to 4.0GHz



**Figure 1.1 Device Image**  
(16 Pin 3x3x0.8mm QFN Package)

### 2.0 Applications

- Private mobile radio handsets
- Public safety radios
- Cellular infrastructure
- Military radios

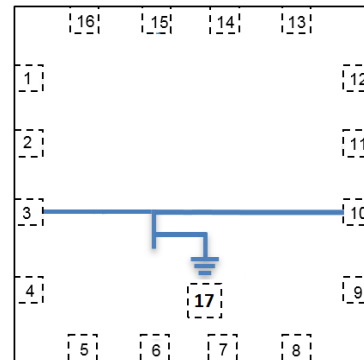


**RoHS/REACH/Halogen Free  
Compliance**

### 3.0 Description

The TA9110K is a broadband GaN power transistor capable of delivering 6W CW from 30MHz to 4.0GHz frequency band. The transistor can be used at lower frequencies with reduced output power. The input and output can be matched for best power and efficiency for the desired band.

The TA9110K is packaged in a compact, low cost Quad Flat No lead (QFN) 3x3x0.8mm, 16 leads plastic package.



**Figure 3.1 Function Block Diagram**  
(Top View)

### 4.0 Ordering Information

**Table 4.1 Ordering Information**

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TA9110K	16 Pin 3x3x0.8mm QFN	Tape and Reel	1000	13" (330mm)	18mm	TA9110KMTRPBF
Tuned Evaluation Board, 30 - 2700MHz						TA9110K-EVB-A

## 5.0 Pin Description

**Table 5.1 Pin Definition**

Pin Number	Pin Name	Description
1,2, 4-9, 11-16	NC	No internal connection, can be connected to ground
3	V <sub>GG</sub> & RF <sub>IN</sub>	Gate voltage and RF input
10	V <sub>DD</sub> & RF <sub>OUT</sub>	Drain voltage and RF output
17 <sup>[1]</sup>	Paddle/Slug	Ground

**Note:** [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

## 6.0 Absolute Maximum Ratings

**Table 6.1 Absolute Maximum Ratings @T<sub>A</sub>=+25°C Unless Otherwise Specified**

Parameter	Symbol	Value	Unit
<b>Electrical Ratings</b>			
Breakdown voltage	V <sub>DS</sub>	+120	V
Gate voltage	V <sub>GS</sub>	-10 to +2.0	V
Drain current	I <sub>DS</sub>	0.75	A
Gate current	I <sub>GS</sub>	2.1	mA
Power dissipation CW	P <sub>diss</sub>	12	W
RF input power CW, @1000MHz	RF <sub>IN</sub>	28	dBm
Storage Temperature Range	T <sub>st</sub>	-55 to +150	°C
Operating Temperature Range	T <sub>op</sub>	-40 to +85	°C
Maximum Junction Temperature	T <sub>J</sub>	+225	°C
<b>Thermal Ratings</b>			
Thermal Resistance (junction-to-case) – Bottom side	R <sub>θJC</sub>	8.9	°C/W
Soldering Temperature	T <sub>SOLD</sub>	260	°C
<b>ESD Ratings</b>			
Human Body Model (HBM)	Level 1A	250 to <500	V
Charged Device Model (CDM)	Level C1	250 to <500	V
<b>Moisture Rating</b>			
Moisture Sensitivity Level	MSL	1	-

### Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

## 7.0 RF Electrical Specifications

**Table 7.1 Electrical Specifications** @ $T_A=+25^{\circ}\text{C}$  Unless Otherwise Specified;

Parameter	Condition	Minimum	Typical	Maximum	Unit
Small Signal Gain	1000MHz		17		dB
Large Signal Gain	$P_{OUT} = 38\text{dBm}$ , 1000MHz		14		dB
$P_{SAT}$	1000MHz		40		dBm
Power Added Efficiency (PAE)	$P_{OUT} = 38\text{dBm}$		46		%
Drain Voltage			32		V
Ruggedness	All phase, $P_{OUT} = 38\text{dBm}$	VSWR = 10:1			

**Note:** Data taken from 30 - 27000MHz broadband reference design (EVB),  $V_D=+32\text{V}$ ;  $I_{DQ}=40\text{mA}$ , CW

## 8.0 Recommended Operating Conditions

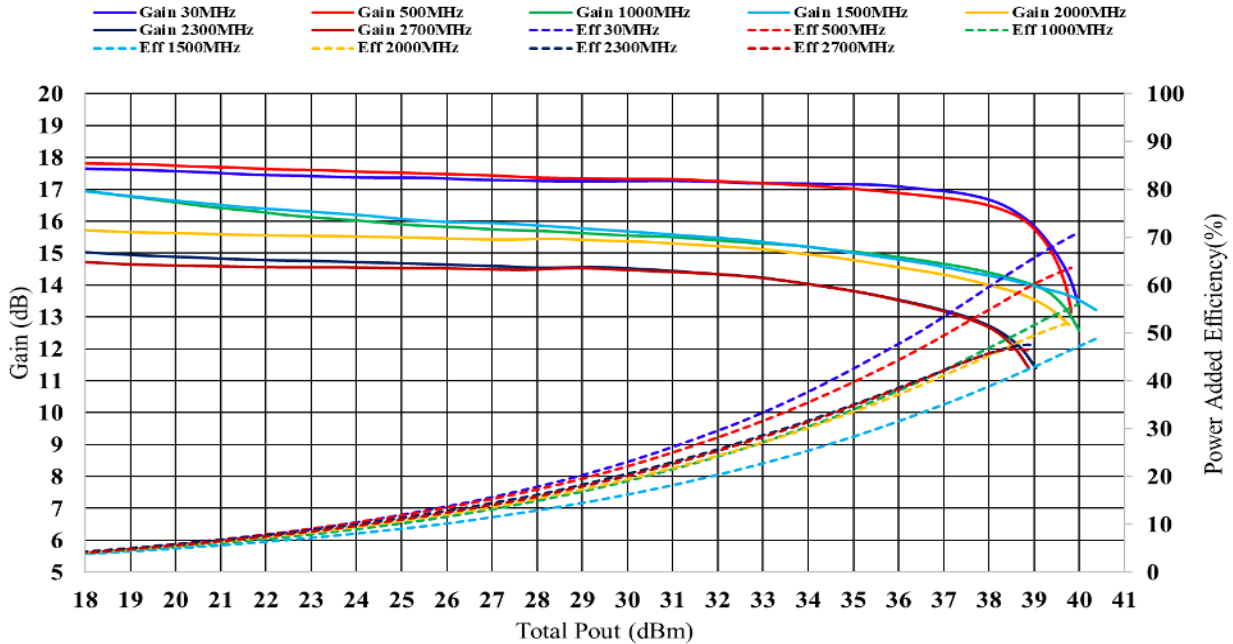
**Table 8.1 Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	$V_{DD}$	+12	+32	+34	V
Gate Voltage	$V_{GG}$	-3.0	-2.55	-2.4	V
Drain Bias Current	$I_{DQ}$		40		mA
Drain Current	$I_{DS}$		500		mA
Power Dissipation CW <sup>[1]</sup>	$P_{diss} @ 38\text{dBm } P_{out}$			10	W
Operating Temperature Range		-40	+25	+85	$^{\circ}\text{C}$

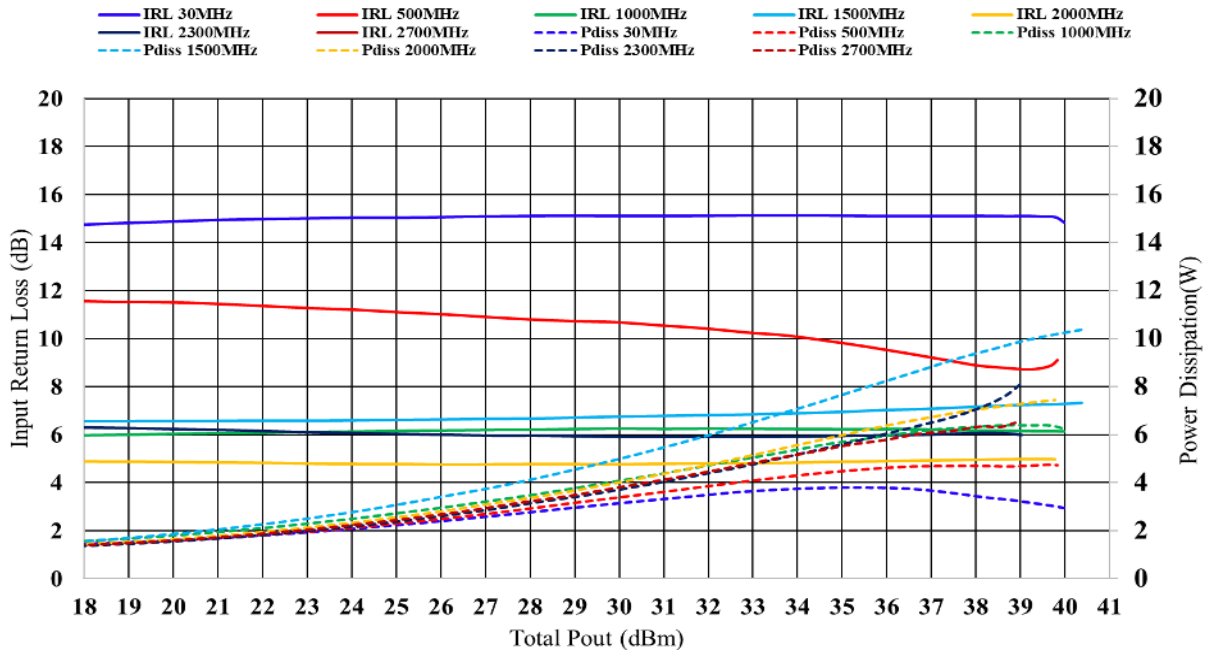
**Note:** [1] @ $T_C = +85^{\circ}\text{C}$

## 9.0 Typical Characteristics

### 9.1 30 - 2700MHz EVB (Vd=32V, I<sub>DQ</sub>=40mA, CW, T<sub>A</sub>=+25°C)

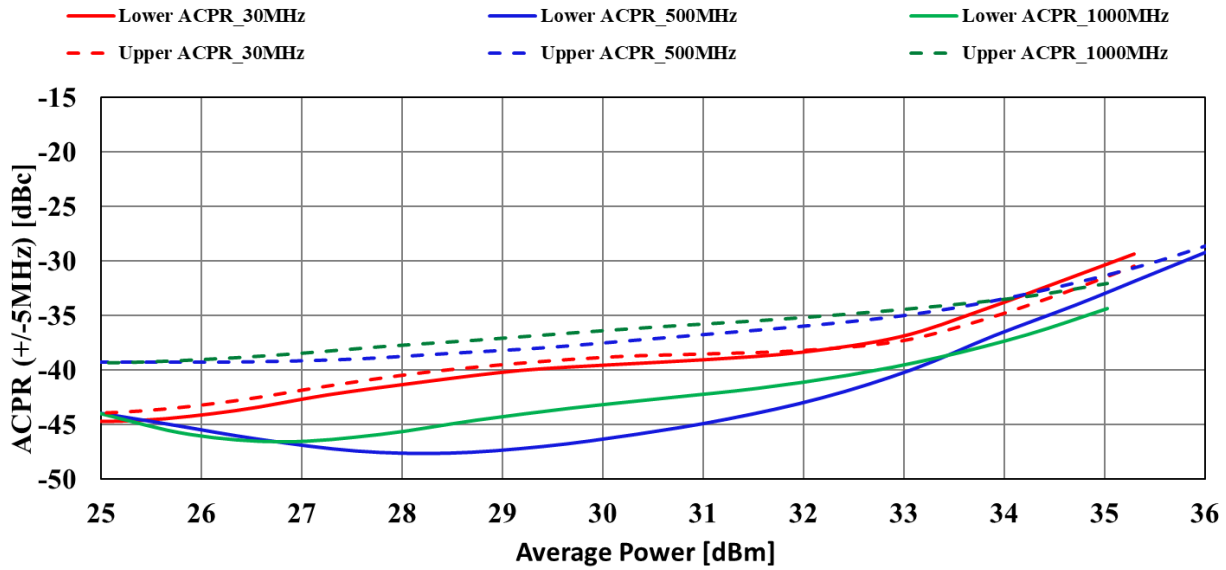


**Figure 9.1 Gain and PAE vs P<sub>OUT</sub> (30-2700MHz)**

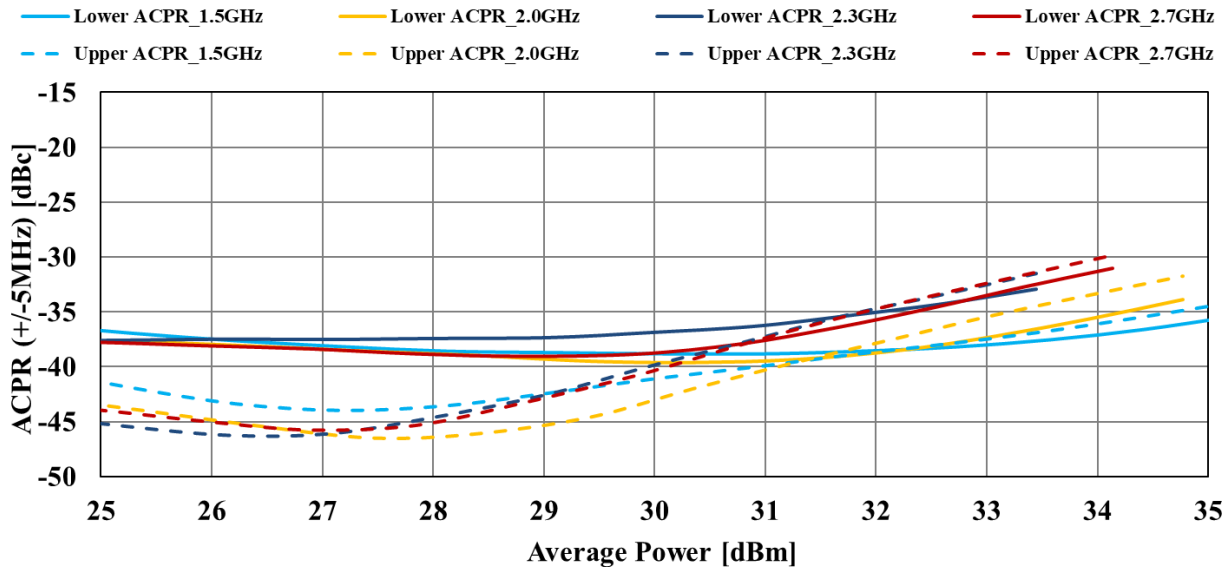


**Figure 9.2 IRL and P<sub>diss</sub> vs P<sub>OUT</sub> (30-2700MHz)**

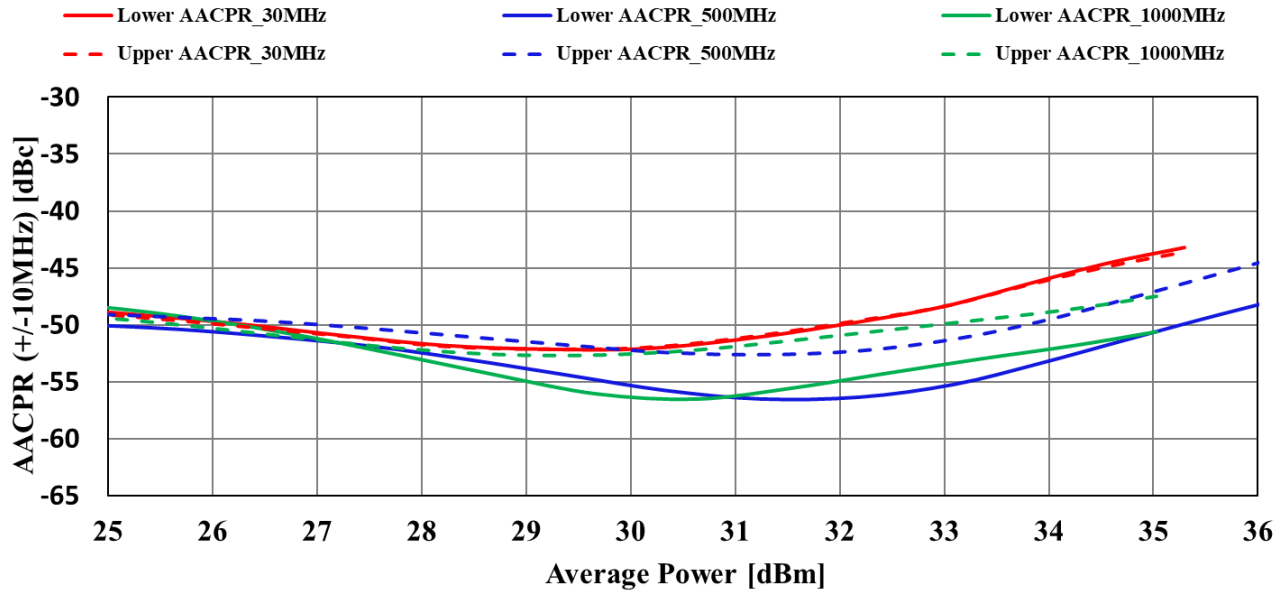
**9.2 30 - 2700MHz EVB (Vd=32V, I<sub>DQ</sub>=40mA, LTE, 8dB PAPR, 4.515MHz BW, T<sub>A</sub>=+25°C)**



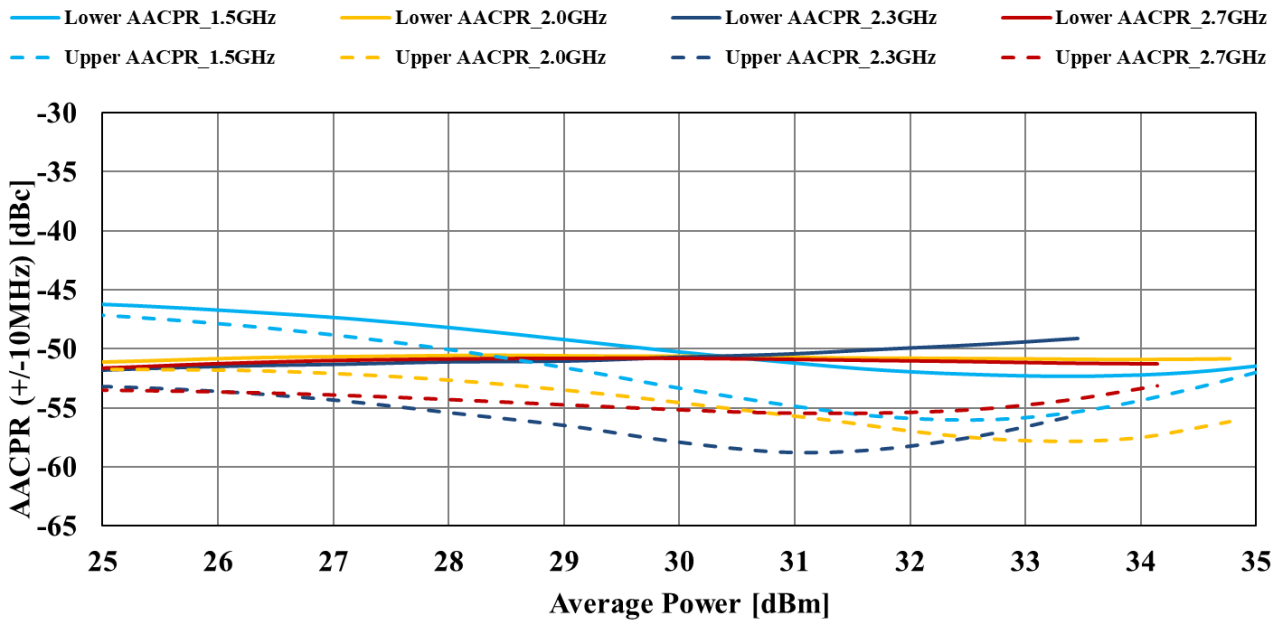
**Figure 9.3 ACPR vs P<sub>OUT</sub> (30-1000MHz)**



**Figure 9.4 ACPR vs P<sub>OUT</sub> (1500-2700MHz)**



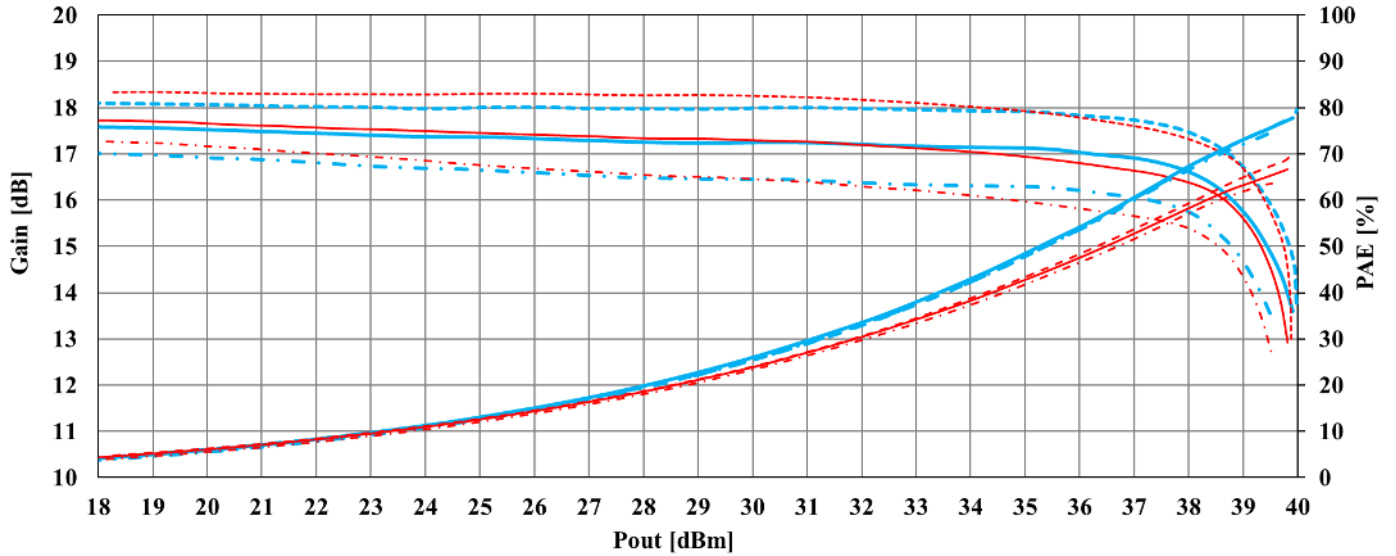
**Figure 9.5 AACPR vs P<sub>OUT</sub> (30-1000MHz)**



**Figure 9.6 AACPR vs P<sub>OUT</sub> (1500-2700MHz)**

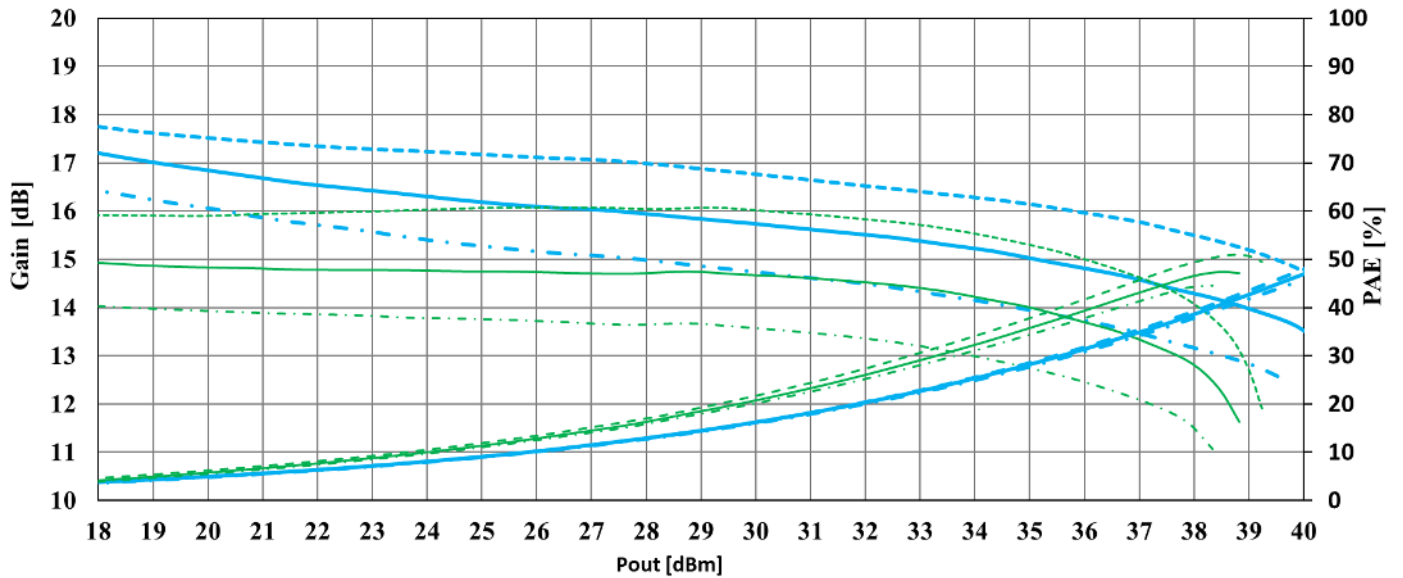
**9.3 30 - 2700MHz EVB (Vd=32V, I<sub>DQ</sub>=40mA, CW, Over Temp -40 to +85degC)**

- Gain 30MHz\_-40C    — Gain 30MHz\_+25C    - - Gain 30MHz\_+85C    - - - Gain 500MHz\_-40C    — Gain 500MHz\_+25C    - - - Gain 500MHz\_+85C  
 --- PAE 30MHz\_-40C    — PAE 30MHz\_+25C    - - PAE 30MHz\_+85C    - - - PAE 500MHz\_-40C    — PAE 500MHz\_+25C    - - - PAE 500MHz\_+85C



**Figure 9.7 Gain and PAE vs P<sub>OUT</sub> (30, 500MHz)**

- Gain 1.5GHz\_-40C    — Gain 1.5GHz\_+25C    - - Gain 1.5GHz\_+85C    - - - Gain 2.7GHz\_-40C    — Gain 2.7GHz\_+25C    - - - Gain 2.7GHz\_+85C  
 --- PAE 1.5GHz\_-40C    — PAE 1.5GHz\_+25C    - - PAE 1.5GHz\_+85C    - - - PAE 2.7GHz\_-40C    — PAE 2.7GHz\_+25C    - - - PAE 2.7GHz\_+85C



**Figure 9.8 Gain and PAE vs P<sub>OUT</sub> (1500, 2700MHz)**

## 10.0 Bias and Sequencing

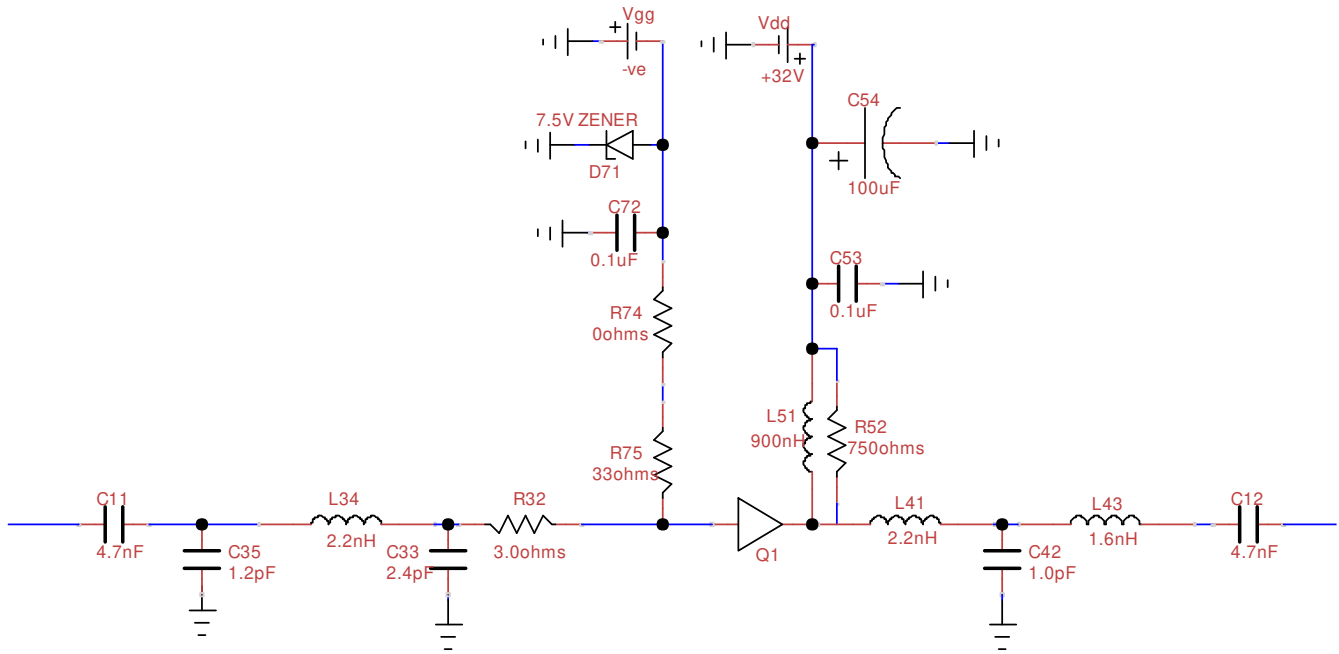
**Table 10.1 Bias and Sequencing**

Turn ON Device	Turn OFF Device
<ol style="list-style-type: none"> <li>1. Set <math>V_G</math> to -5V</li> <li>2. Set <math>V_D</math> to +32V</li> <li>3. Adjust <math>V_G</math> to reach required <math>I_{DQ}</math> current</li> <li>4. Apply RF power</li> </ol>	<ol style="list-style-type: none"> <li>1. Turn RF power off</li> <li>2. Turn off <math>V_D</math></li> <li>3. Turn off <math>V_G</math></li> </ol>

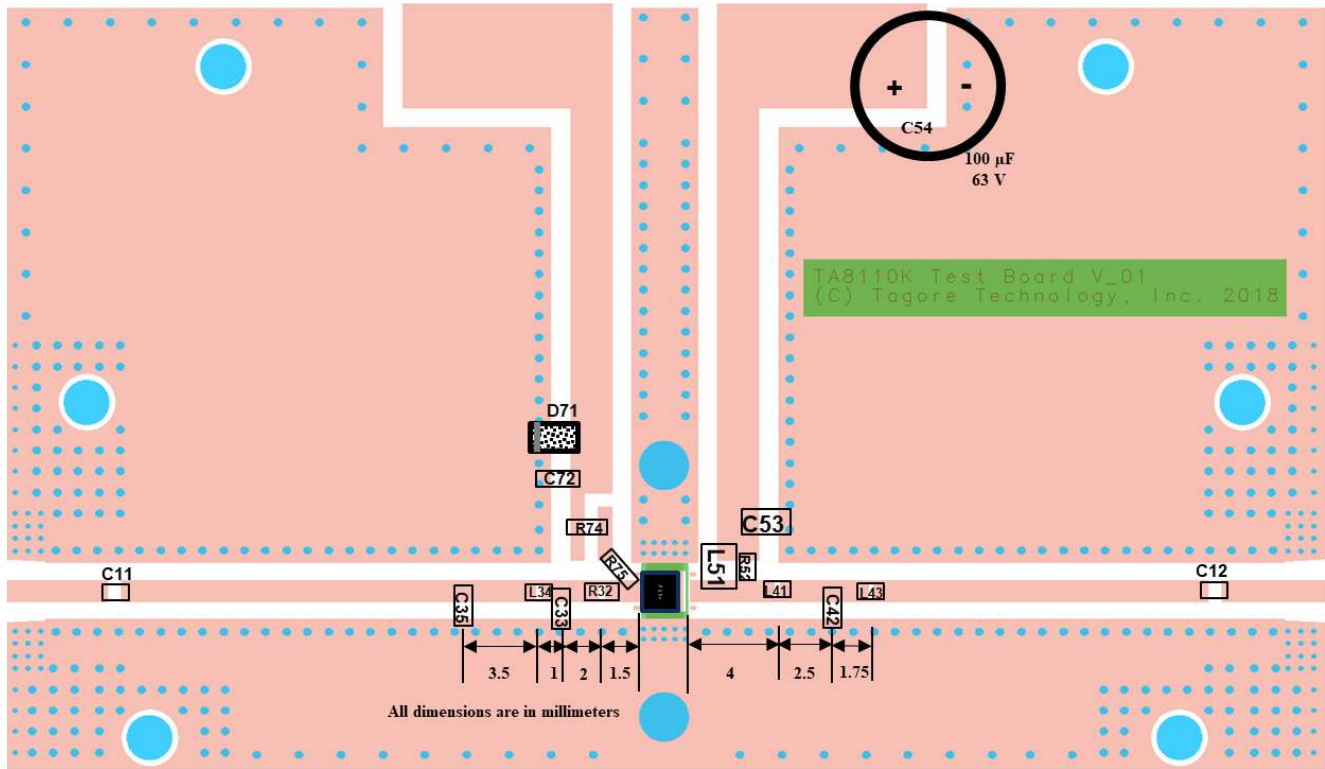


## 11.0 Evaluation Boards

### 11.1 30 - 2700MHz EVB



**Figure 11.1 Schematic of the 30 - 2700MHz EVB**

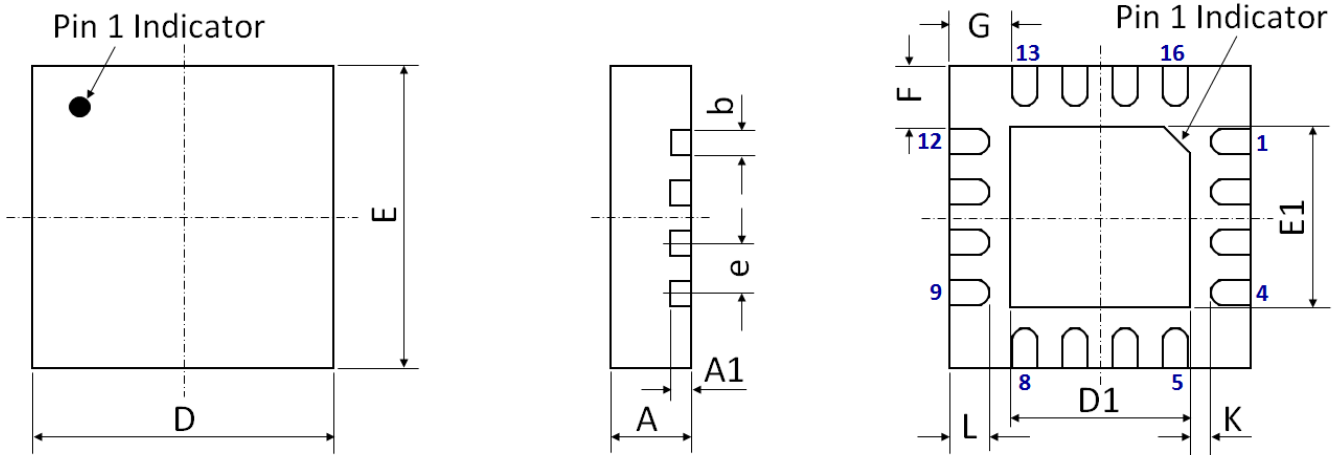


**Figure 11.2 Board Layout of the 30 - 2600MHz EVB**

**Table 11.1 BOM of the 30 - 2700MHz EVB**

Component ID	Value	Manufacturer	Recommended Part Number
C11,12	4.7nF, 50V	Murata	GRM1885C1H472JA01D
R32	3Ω	Vishay	RCS06033R00FKEA
C33	2.4pF	ATC	600S2R4CT250XT
L34,L41	2.2nH	Coilcraft	0402HP-2N2XJE
C35	1.2pF	ATC	600S1R2CT250XT
C42	1pF	ATC	600S1R0CT250XT
L43	1.6nH	Coilcraft	0603HC-1N6XGLW
L51	900nH	Coilcraft	1008AF-901XJLC
R52	750Ω	Vishay	CRCW0603750RFKEB
C53	0.1μF, 50V	Murata	GRM31C5C1H104JA01L
C54	100μF	Nichicon	UPW1J101MPD1TD
D71	7.5 V Zener	On Semiconductor	MMSZ5236BT1G
C72	0.1μF, 10V	AVX	0603ZC104K4T2A
R74	0Ω	Vishay	CRCW06030000Z0EAC
R75	33Ω	ROHM Semiconductor	ESR03EZPJ330
Q1		Tagore Technology	TA9110K
PCB	Rogers RO4350B, 20 mils, 2 oz copper		

## 12.0 Device Package Information



**Figure 12.1 Device Package Drawing**  
(All dimensions are in mm)

**Table 12.1 Device Package Dimensions**

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

**Note:** Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

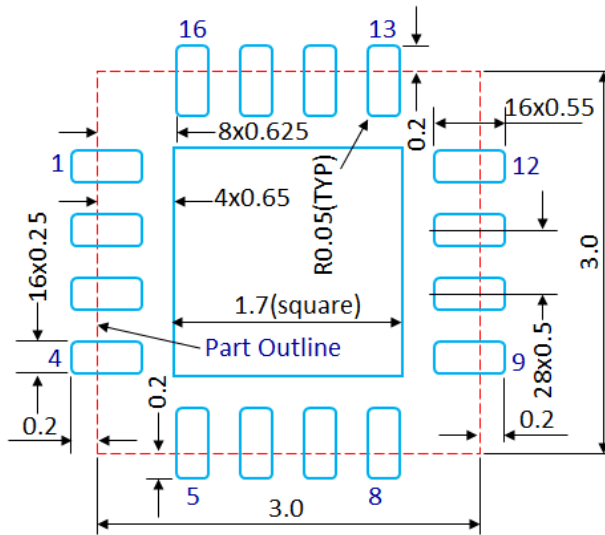
**Attention:**

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

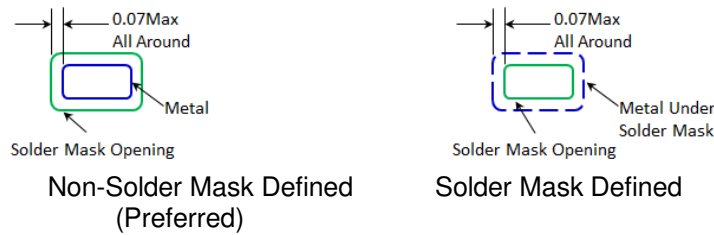
### 13.0 PCB Land Design

**Guidelines:**

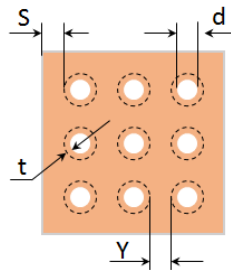
- [1] 2-layer PCB is recommended
- [2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias
- [3] Thermal vias shall only be placed on the center pad and should be filled/plugged with solder or copper
- [4] The maximum via number for the center pad is 3(X)×3(Y)=9



**Figure 13.1 PCB Land Pattern**  
(Dimensions are in mm)



**Figure 13.2 Solder Mask Pattern**  
(Dimensions are in mm)



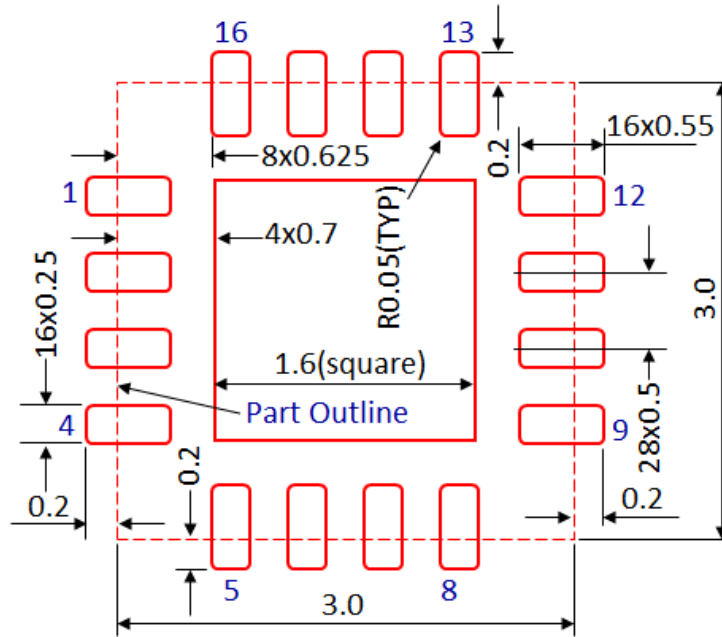
**Figure 13.3 Thermal Via Pattern**  
(Recommended Values:  $S \geq 0.15\text{mm}$ ;  $Y \geq 0.20\text{mm}$ ;  $d = 0.3\text{mm}$ ; Plating Thickness  $t = 25\mu\text{m}$  or  $50\mu\text{m}$ )

### 14.0 PCB Stencil Design

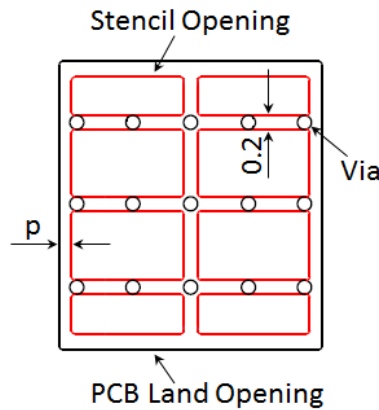
**Guidelines:**

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

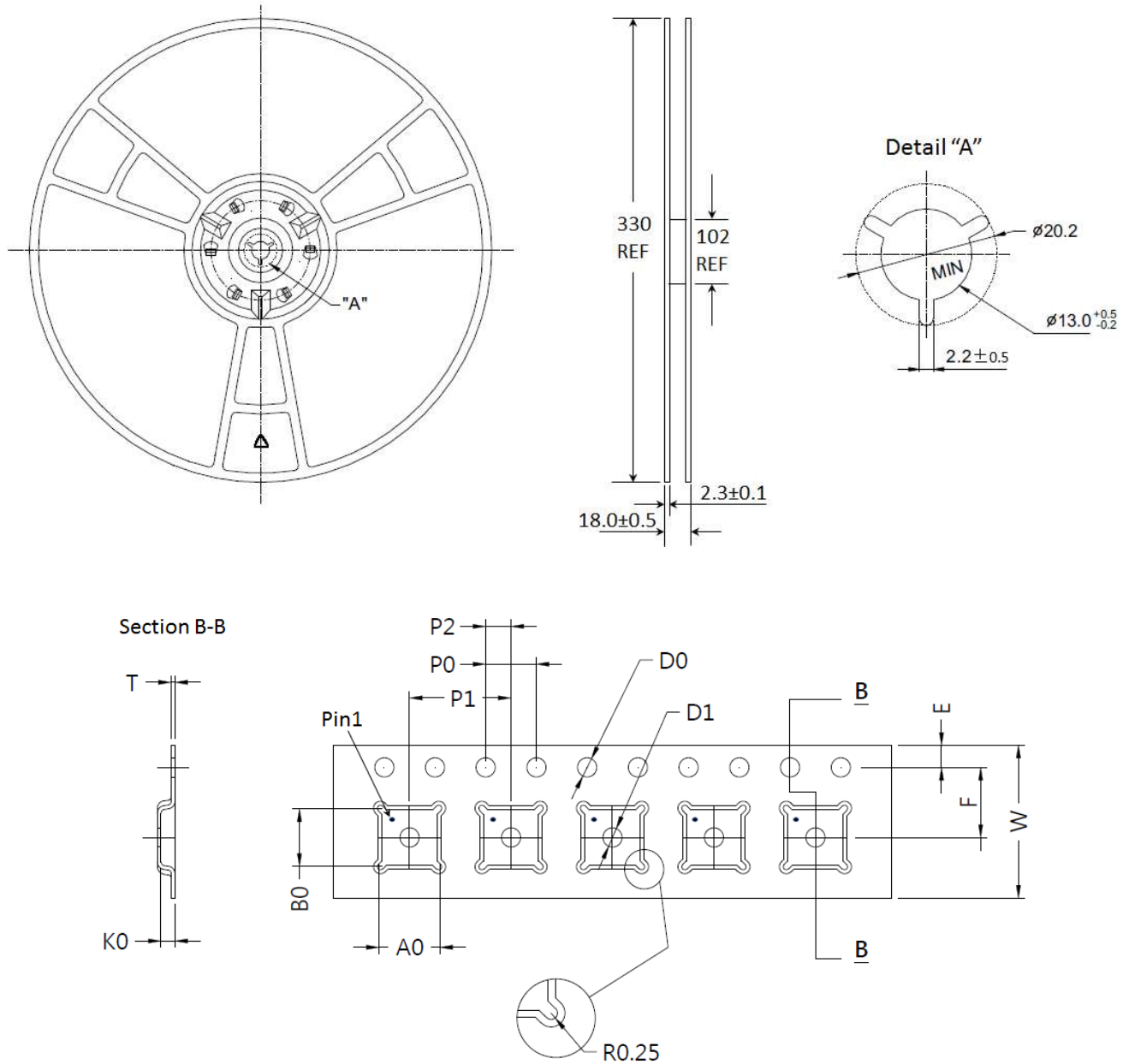


**Figure 14.1 Stencil Openings**  
(Dimensions are in mm)



**Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible**  
(Dimensions are in mm)

**15.0 Tape and Reel Information**



**Figure 15.1 Tape and Reel Drawing**

**Table 15.1 Tape and Reel Dimensions**

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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