TPS560200EVM-537 0.5-A, Single Channel Regulator Evaluation Module

This user's guide contains information for the TPS560200 as well as support documentation for the TPS560200EVM-537 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS560200EVM-537.

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1 Introduction

The TPS560200 is a single, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 600 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS560200 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS560200 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS560200 dc/dc synchronous converter is designed to provide up to a 0.5-A output from an input voltage source of 4.5 V to 17 V. The output voltage range is from 0.8 V to 5.5 V. Rated input voltage and output current ranges for the evaluation module are given in Table 1.

The TPS560200EVM-537 evaluation module (EVM) is a single, synchronous buck converter providing 1.05 V at 0.5 A from 4.5-V to 17-V input. This user's guide describes the TPS560200EVM-537 performance.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS560200EVM-537	V_{IN} = 4.5 V to 17 V	0 A to 0.5 A

2 Performance Specification Summary

A summary of the TPS560200EVM-537 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2. TPS560200EVM-537Performance Specifications Summary

Specifications		Test Conditions	Min	Typ	Max	Unit
Input voltage range (V_{IN})			4.5	12	17	V
CH1	Output voltage			1.05		V
	Operating frequency	V_{IN} = 12 V, I_O = 0.5 A		600		kHz
	Output current range		0		0.5	A
	Over current limit	V_{IN} = 12 V, L_O = 10 µH	0.55			A
	Output ripple voltage	V_{IN} = 12 V, I_O = 0.5 A		10		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS560200. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using Equation 1.

$$R2 = \frac{R1 \times 0.8\ V}{V_{OUT} - 0.8V} \quad (1)$$

Table 3 lists the R1 values for some common output voltages. For higher output voltages of 1.8 V or above, a feedforward capacitor (C3) may be required to improve phase margin. Pads for this component (C3) are provided on the printed-circuit board. Note that the values given in Table 3 are standard values and not the exact value calculated using Table 3.

Table 3. Output Voltages

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L1 (µH)			C4 + C5 (µF)
				Min	Typ	Max	
1.0	6.19	20.0			10		10 + 10
1.05	6.19	20.0			10		10 + 10
1.2	10.0	20.0			10		10 + 10
1.5	17.4	20.0			10		10 + 10
1.8	24.9	20.0	optional		10		10 + 10
2.5	42.2	20.0	optional		10		10 + 10
3.3	61.9	20.0	optional		10		10 + 10
5.0	105	20.0	optional		10		10 + 10

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS560200EVM-537. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS560200EVM-537 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 1 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

Table 4. Connection and Test Points

Reference Designator	Function
J1-1	V_{IN} positive sense and monitor point
J1-2	V_{IN} (see Table 1 for V_{IN} range)
J2-1	Ground return for V_{IN}
J2-2	V_{IN} negative sense and monitor point
J3-1	V_{OUT} positive sense and monitor point
J3-2	V_{OUT}, 1.05 V at 0.5-A maximum
J4-1	Ground return for V_{OUT}
J4-2	V_{OUT} negative sense and monitor point
JP1	EN control. Shunt EN to GND to disable, open EN to enable.
TP1	Switch node test point
TP2	Test point for loop response measurements

4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) is covered to shunt EN to GND, disabling the output.
2. Apply appropriate V_{IN} voltage to VI (J1-2) and GND (J2-1).
3. Remove the jumper at JP1 (Enable control) to uncover EN and GND, enabling the output.

4.3 Efficiency

Figure 1 shows the efficiency for the TPS560200EVM-537 at an ambient temperature of 25°C.

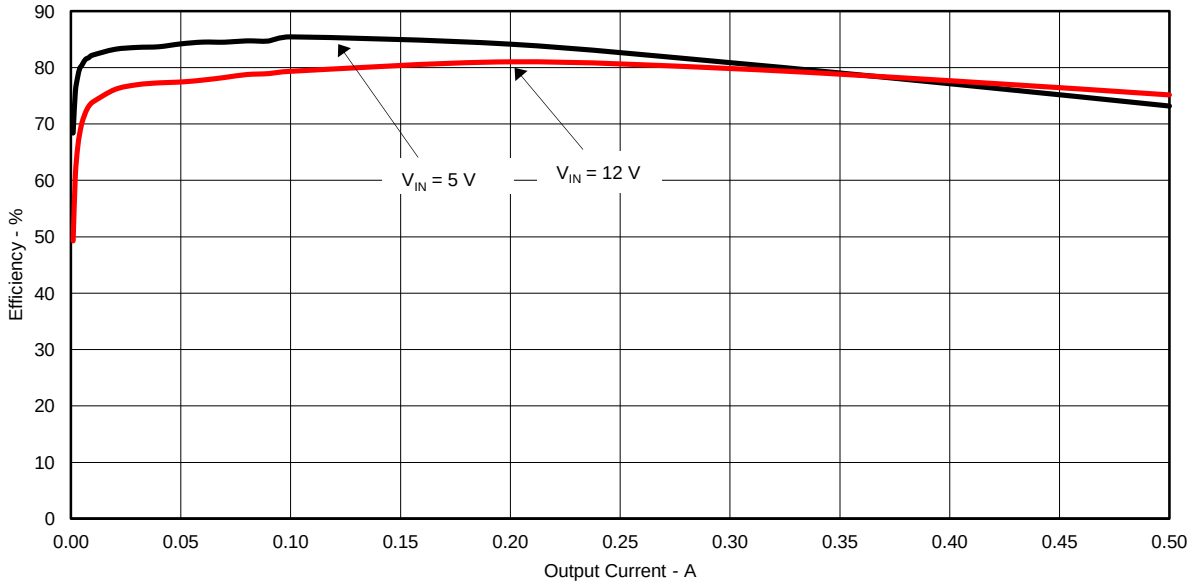

Figure 1. TPS560200EVM-537 Efficiency

Figure 2 shows the efficiency at light loads for the TPS560200EVM-537 at an ambient temperature of 25°C.

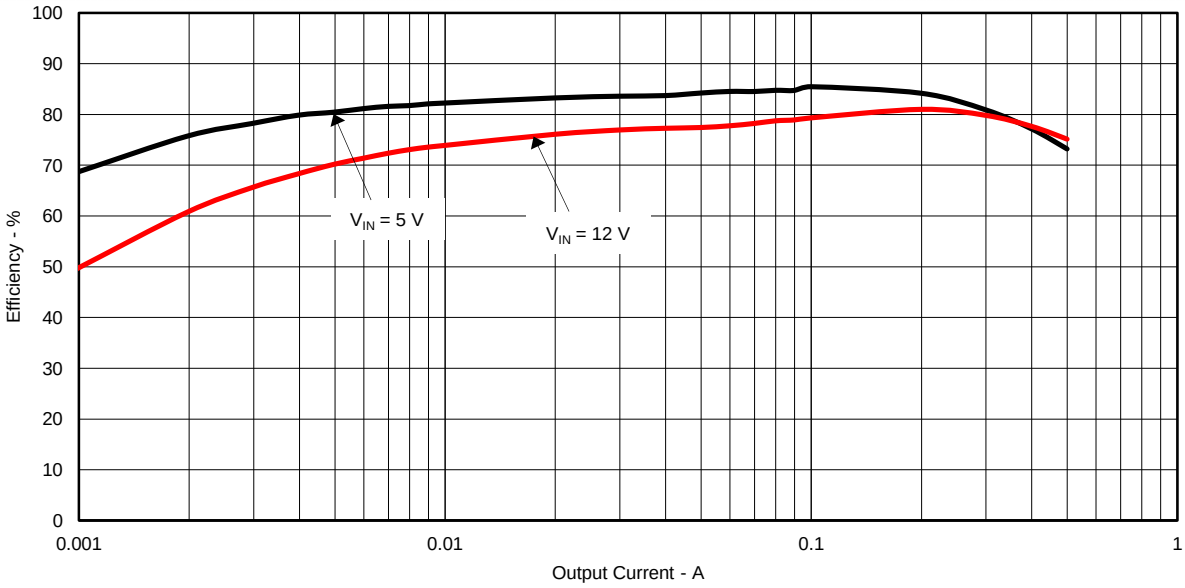

Figure 2. TPS560200EVM-537 Light Load Efficiency

4.4 Load Regulation

The load regulation for the TPS560200EVM-537 is shown in Figure 3.

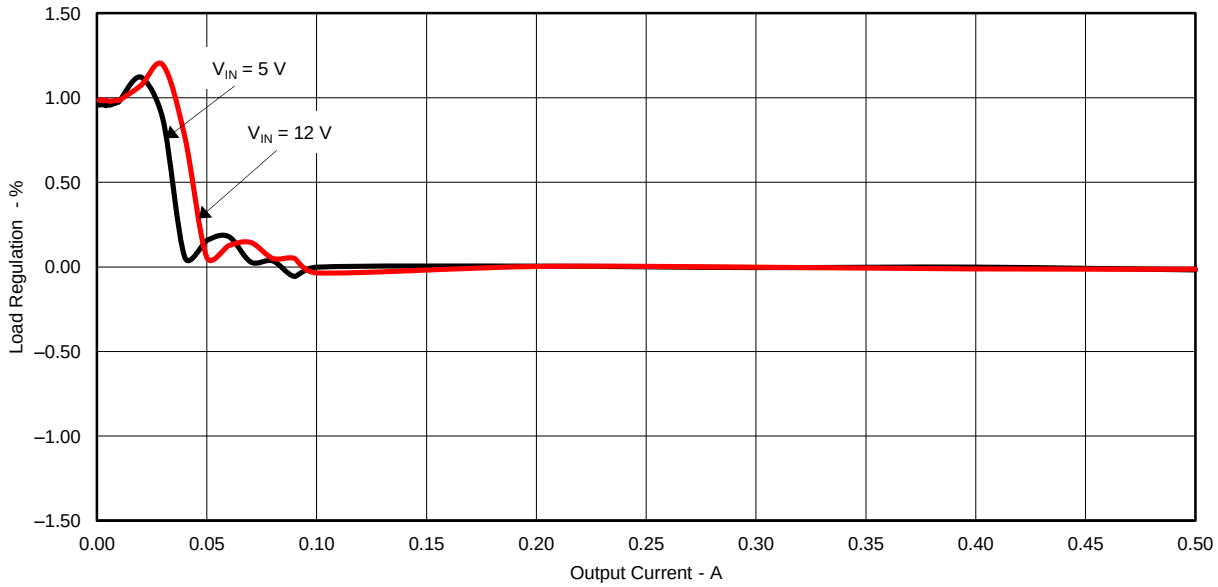

Figure 3. TPS560200EVM-537 Load Regulation

4.5 Line Regulation

The line regulation for the TPS560200EVM-537 is shown in Figure 4.

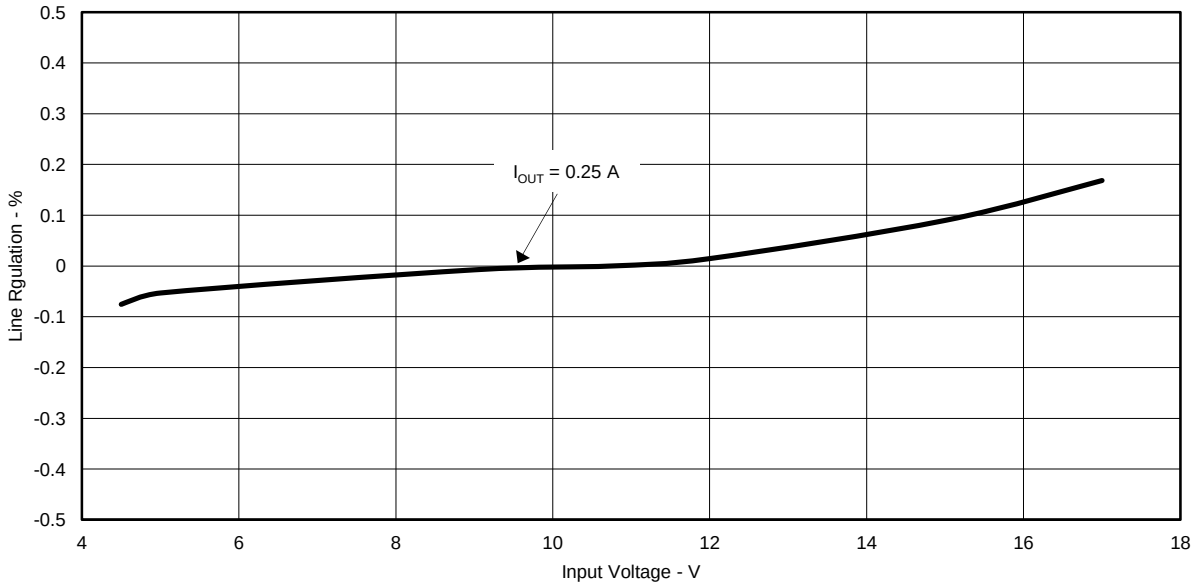

Figure 4. TPS560200EVM-537 Line Regulation

4.6 Load Transient Response

The TPS560200EVM-537 response to load transient is shown in Figure 5 and Figure 6. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown.

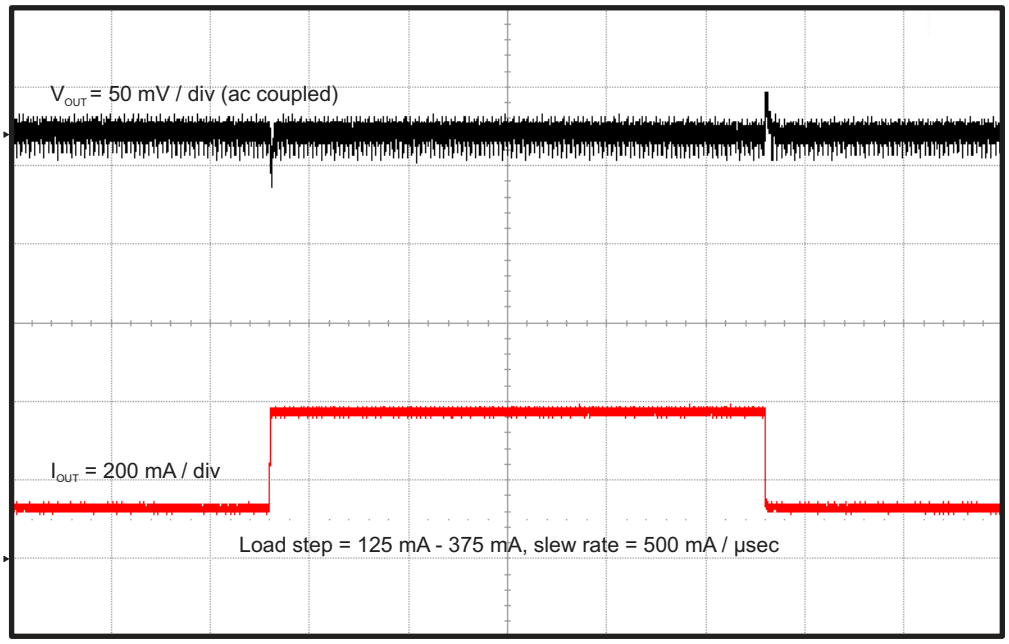

Figure 5. TPS560200EVM-537 Load Transient Response, 25% to 75% Load Step

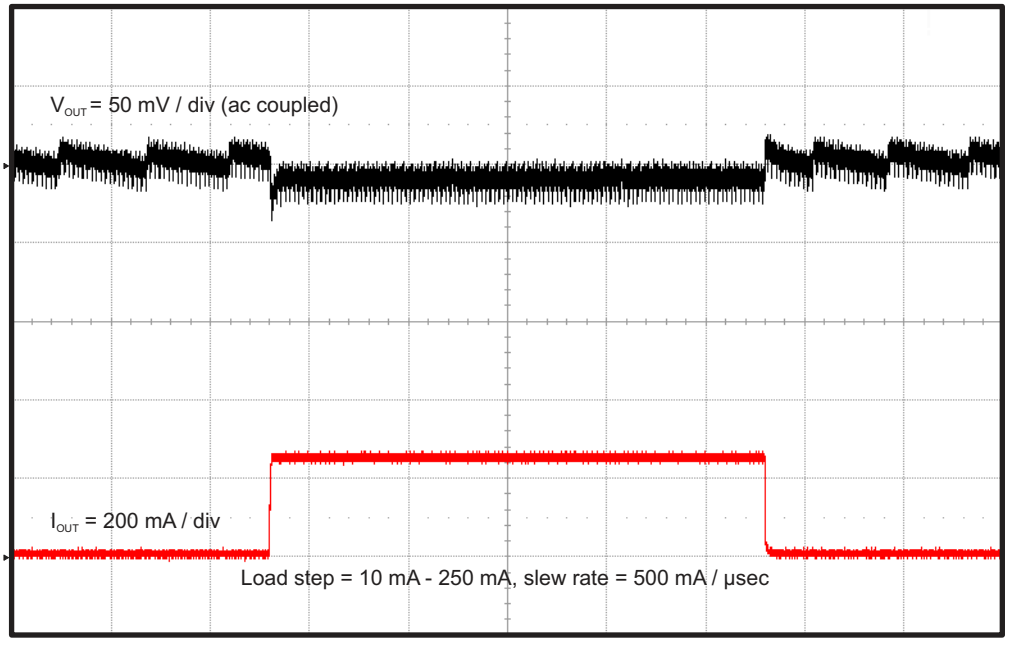

Figure 6. TPS560200EVM-537 Load Transient Response, No Load to 50% Load Step

4.7 Output Voltage Ripple

The TPS560200EVM-537 output voltage ripple is shown in Figure 7, Figure 8, and Figure 9. The output currents are as indicated.

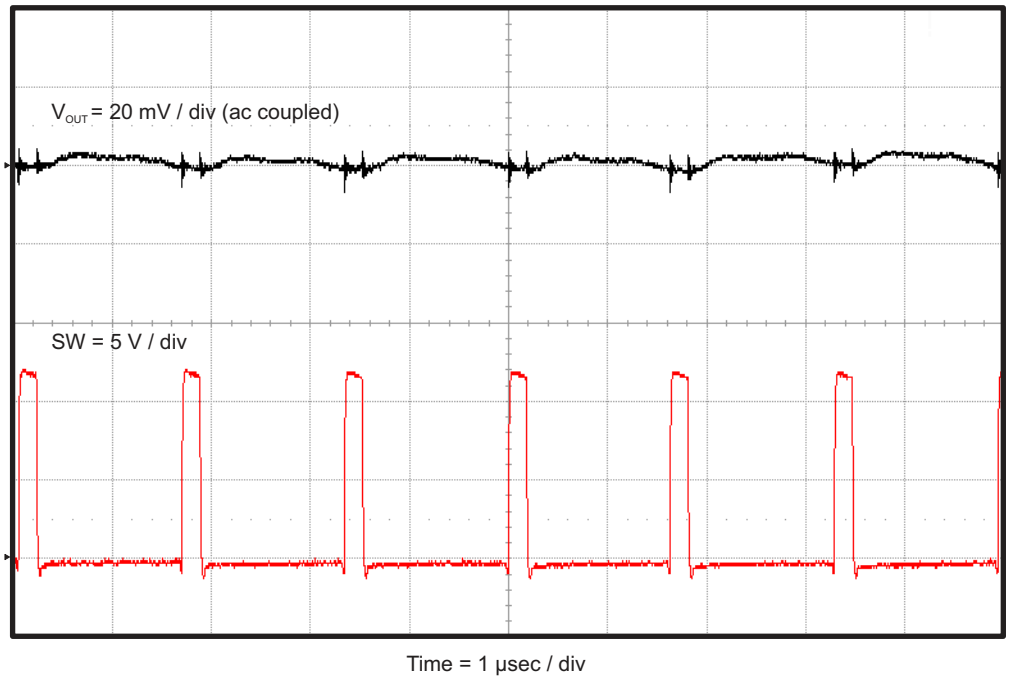

Figure 7. TPS560200EVM-537 Output Voltage Ripple, I_{OUT} = 0.5 A

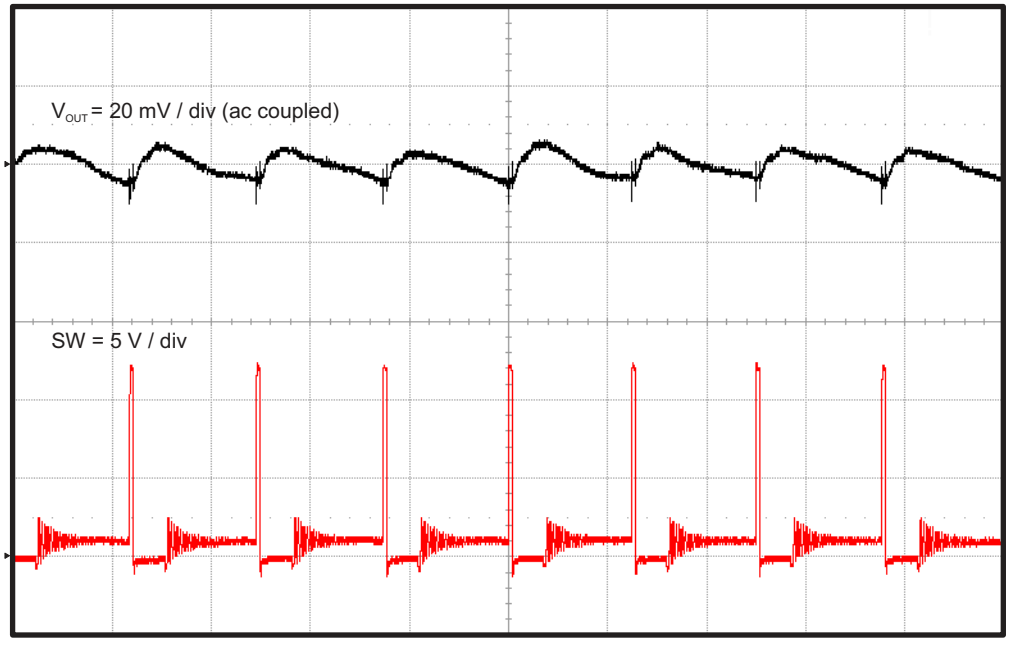

Figure 8. TPS560200EVM-537 Output Voltage Ripple, I_{OUT} = 30 mA

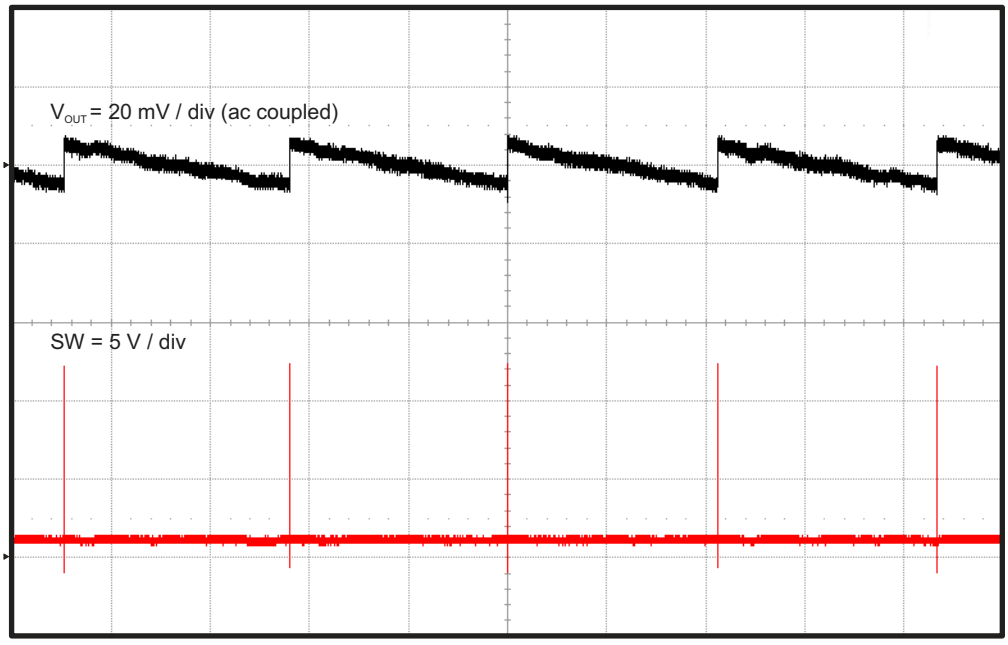

Figure 9. TPS560200EVM-537 Output Voltage Ripple, I_{OUT} = 0 A

4.8 Input Voltage Ripple

The TPS560200EVM-537 input voltage ripple is shown in Figure 10. The output current is as indicated.

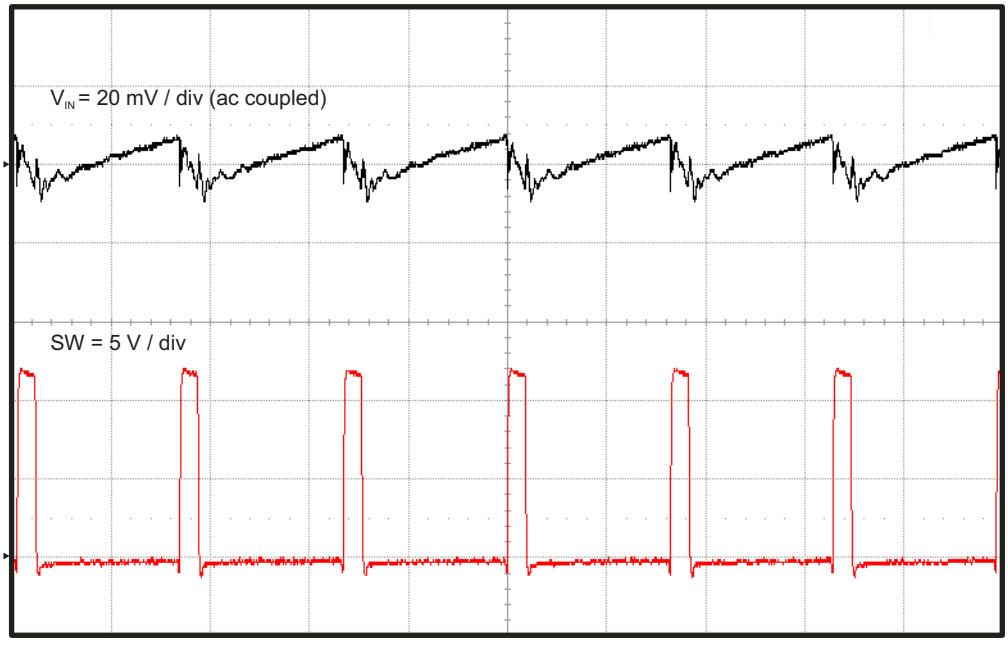

Figure 10. TPS560200EVM-537 Input Voltage Ripple, I_{OUT} = 0.5 A

4.9 Start-Up

The TPS560200EVM-537 start-up waveform relative to V_{IN} is shown in Figure 11. Load = 4 Ω resistive.

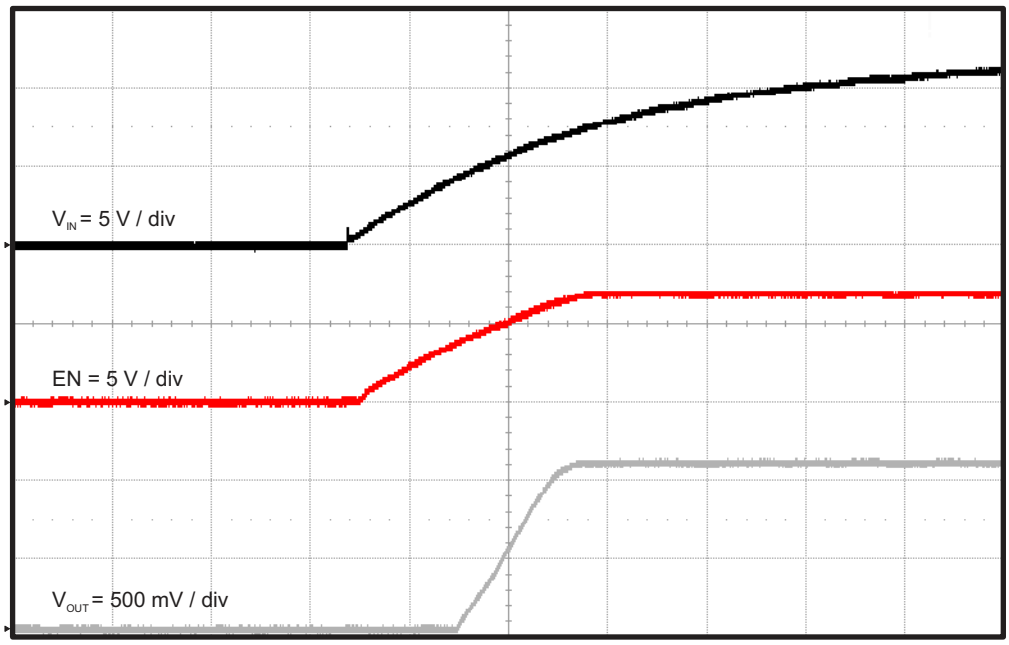

Figure 11. TPS560200EVM-537 Start-Up Relative to V_{IN}

The TPS560200EVM-537 start-up waveform relative to enable (EN) is shown in Figure 12. Load = 4 Ω resistive.

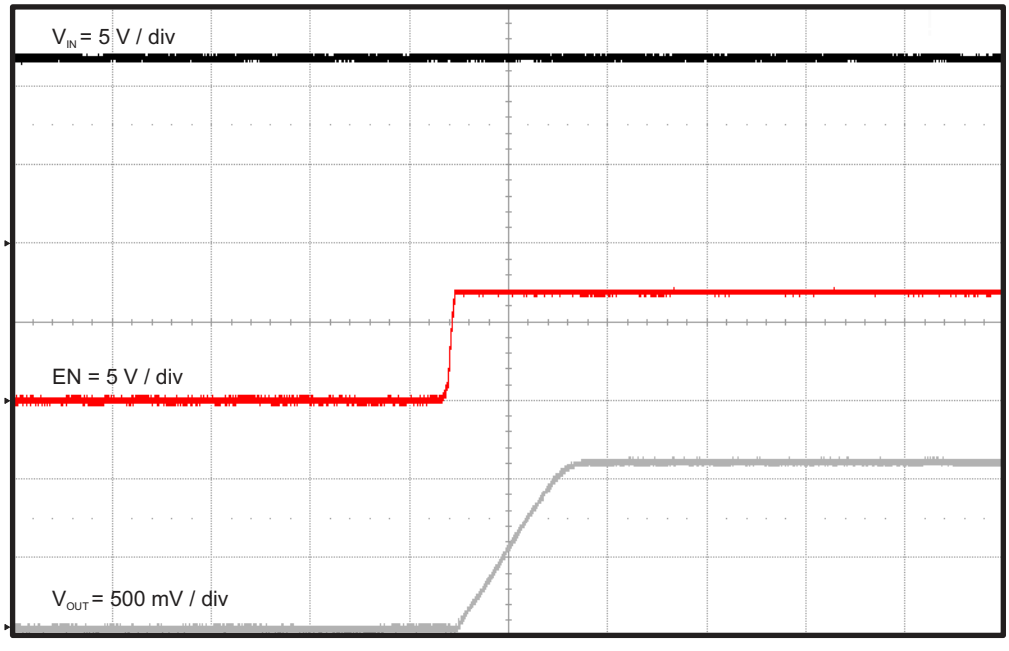

Figure 12. TPS560200EVM-537 Start-Up Relative to EN

4.10 Shut-Down

The TPS560200EVM-537 shut-down waveform relative to V_{IN} is shown in Figure 13. Load = 4 Ω resistive.

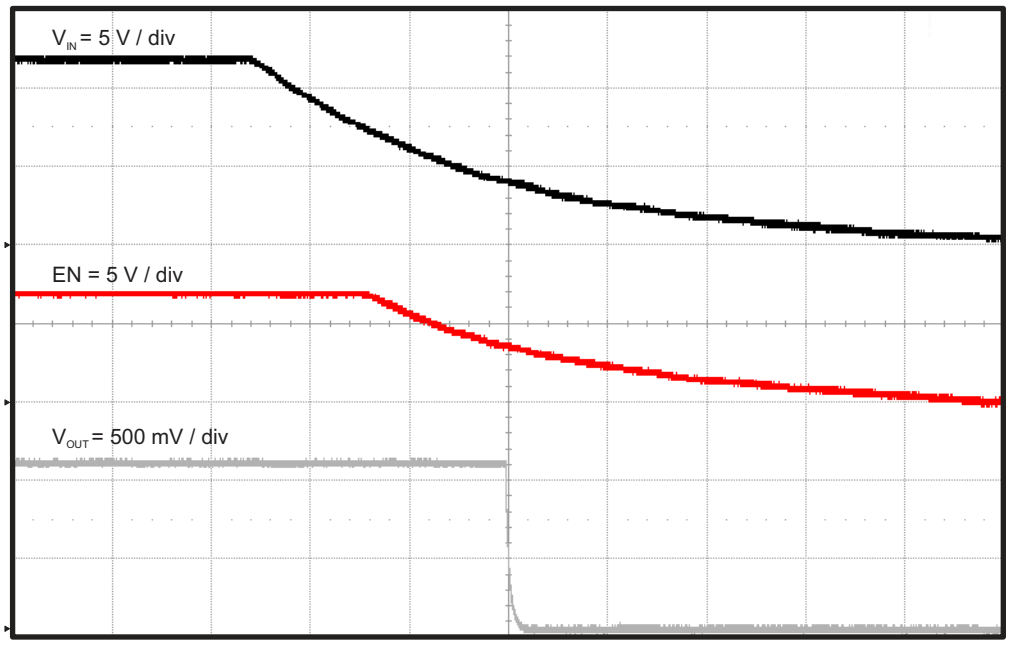

Figure 13. TPS560200EVM-537 Shut-Down Relative to V_{IN}

The TPS560200EVM-537 shut-down waveform relative to EN is shown in Figure 14. Load = 4 Ω resistive.

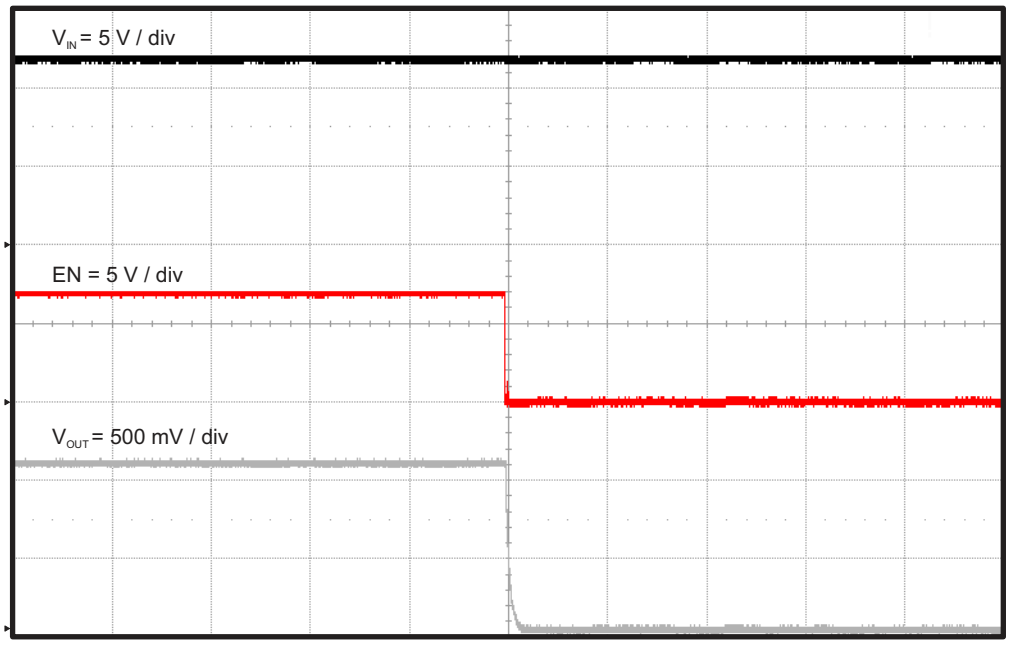

Figure 14. TPS560200EVM-537 Shut-Down Relative to EN

5 Board Layout

This section provides a description of the TPS560200EVM-537, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS560200EVM-537 is shown in Figure 15 through Figure 17. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS560200 and a large area filled with ground. All of the signal traces also are located on the top side. The input decoupling capacitors, C1 and C2, are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane.

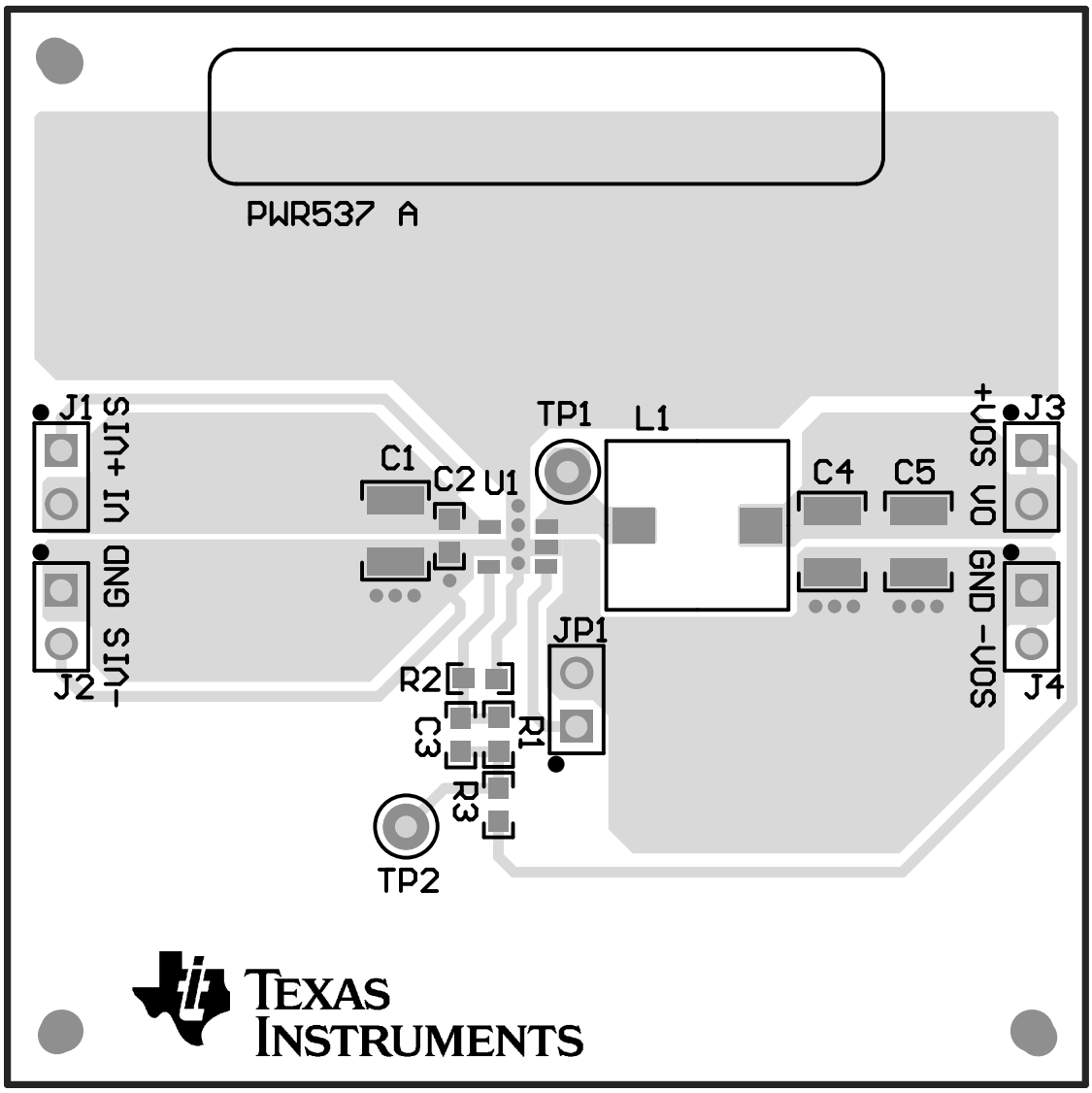

Figure 15. Top Assembly

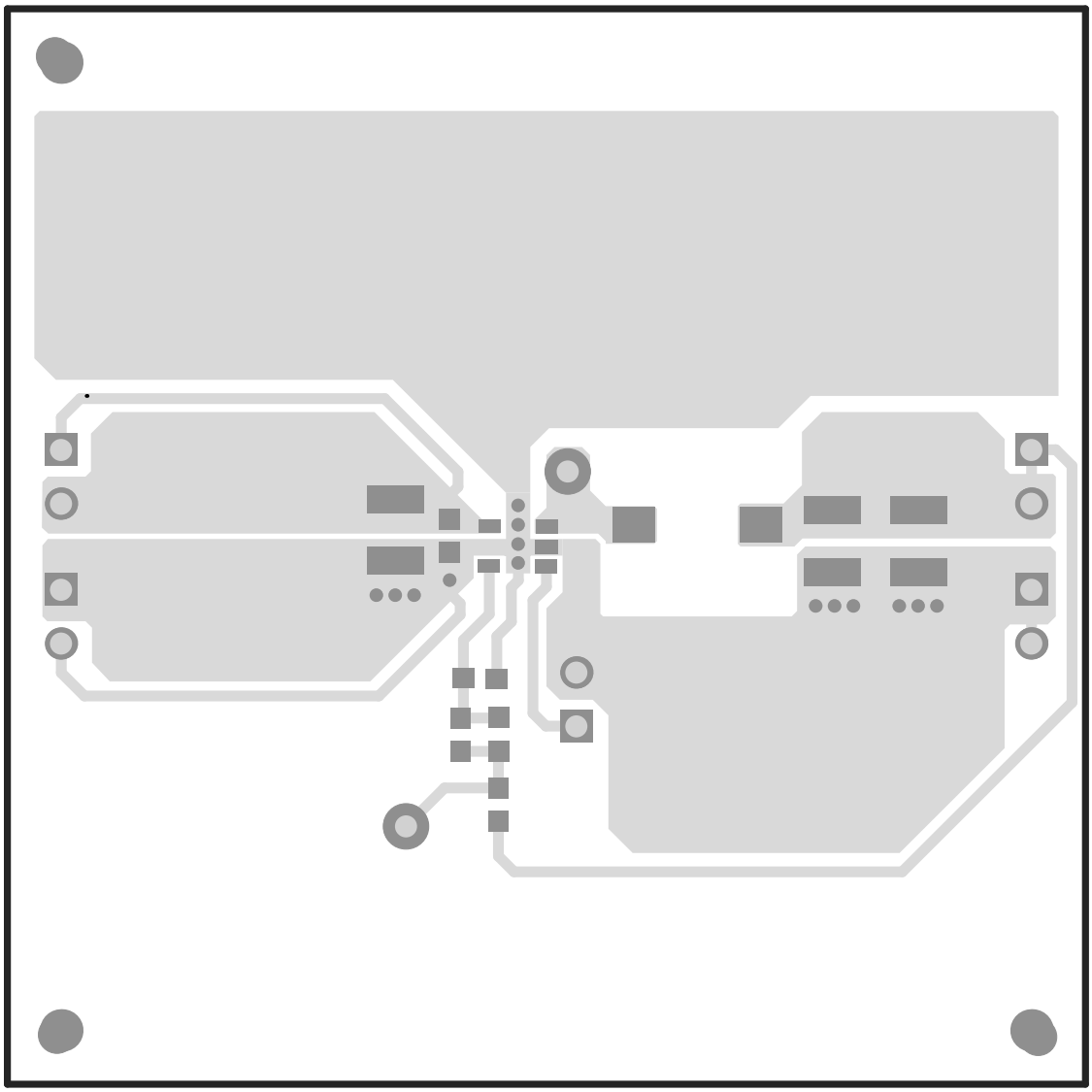

Figure 16. Top Layer

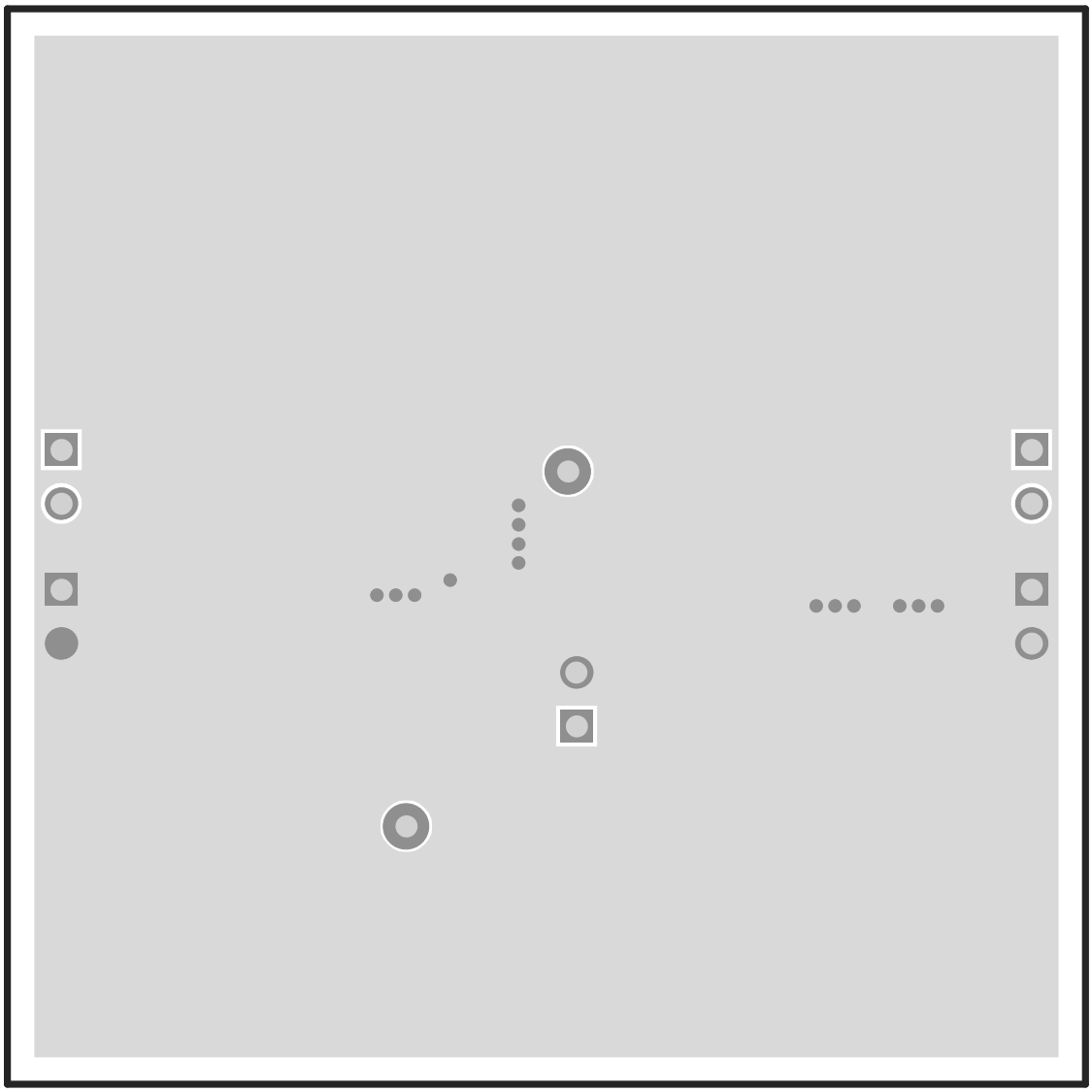

Figure 17. Bottom Layer

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 18 is the schematic for the TPS560200EVM-537.

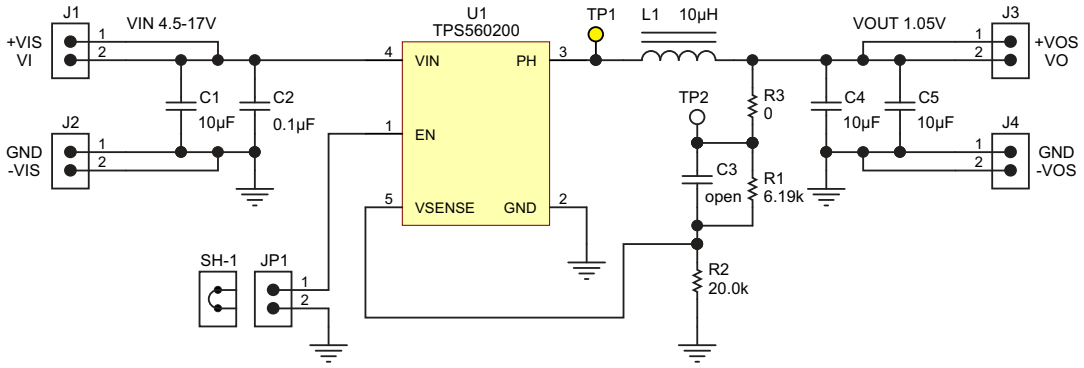

Figure 18. TPS560200EVM-537Schematic Diagram

6.2 Bill of Materials

Table 5. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board		PWR537	Any
C1	1	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1210	1210	GRM32DR61E106KA12L	MuRata
C2	1	0.1uF	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C3	0		CAP, CERM	0603		
C4, C5	2	10uF	CAP, CERM, 10uF, 10V, +/-10%, X5R, 1210	1210	C1210C106K8PACTU	Kemet
J1, J2, J3, J4, JP1	5		Header, 100mil, 2x1, Tin plated, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
L1	1	10uH	Inductor, Shielded Drum Core, Ferrite, 10uH, 2A, 0.045 ohm, SMD	WE-PD-M	744777910	Wurth Elektronik eiSos
LBL1	1		Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R1	1	6.19k	RES, 6.19k ohm, 1%, 0.1W, 0603	0603	CRCW06036K19FKEA	Vishay-Dale
R2	1	20.0k	RES, 20.0k ohm, 1%, 0.1W, 0603	0603	CRCW060320K0FKEA	Vishay-Dale
R3	1	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	ERJ-3GEY0R00V	Panasonic
SH-1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1	1	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP2	1	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1		Step Down Converter, 4.5V to 17 V Input, 500 mA	5 Pin SOT23	TPS560200DBV5	Texas Instruments

6.3 Reference

1. *TPS560200, 4.5V to 17V Input, 0.5-A Synchronous Step-Down SWIFT™ Converter with Advanced Eco-mode™* data sheet (SLVSC81)

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