

General Description

The AOZ5118QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss. AOZ5118QI comes with low noise technology enhancement at switching node to reduce noise interference.

The AOZ5118QI uses a PWM and SMOD# input for accurate control of the power MOSFETs switching activities, is compatible with 3V and 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5118QI a highly versatile power module. The bootstrap switch is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low parasitics, keeping their effects to a minimum.

Features

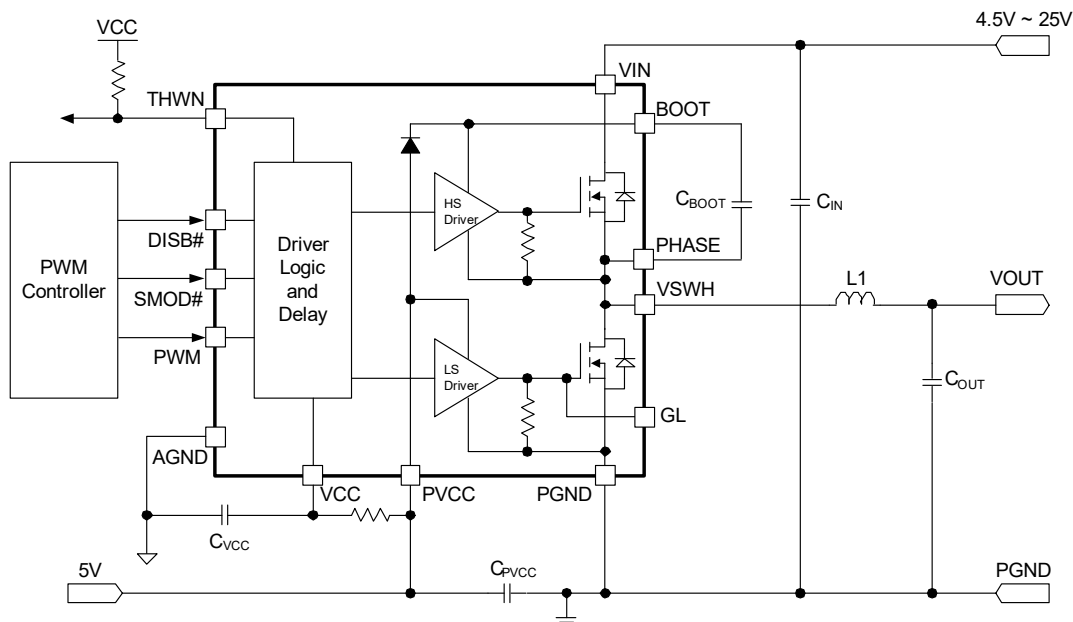
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- 65A continuous output current
 - Up to 80A with 10ms on pulse
 - Up to 120A with 10us on pulse
- Up to 2MHz switching operation
- 3V/5V PWM and Tri-State input compatible
- Supports Intel® Power State 4
- Thermal Warning Output
- Thermal Shutdown
- Under-Voltage LockOut Protection
- SMOD# control for Diode Emulation / CCM operation
- Low Profile 5x5 QFN-31L package

Applications

- Notebook computers
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming consoles



Typical Application Circuit



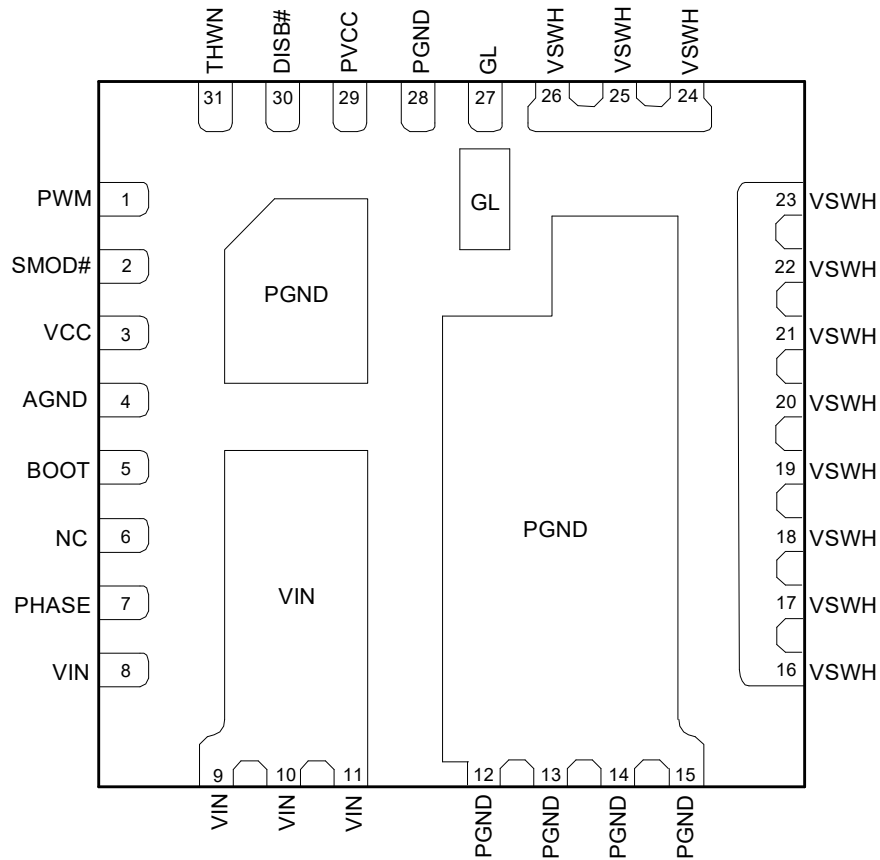
Ordering Information

| Part Number | Junction Temperature Range | Package | Environmental |
|-------------|----------------------------|------------|---------------|
| AOZ5118QI | -40°C to +150°C | QFN5x5-31L | RoHS |



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Pin Configuration

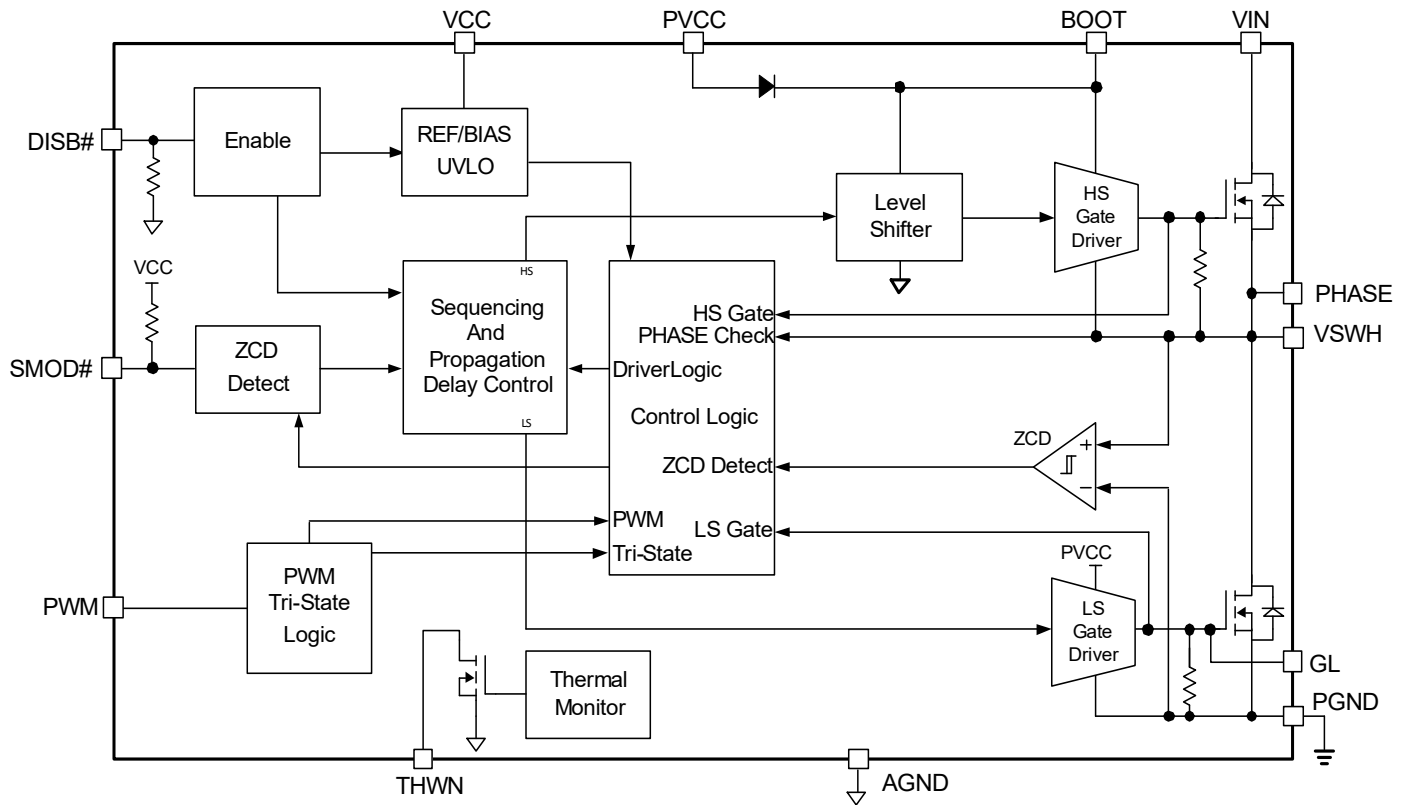


QFN5x5-31L
(Top View)

Pin Description

| Pin Number | Pin Name | Pin Function |
|--|----------|---|
| 1 | PWM | PWM input signal from the controller IC. When DISB#=0V, the internal resistor divider will be disconnected and this pin will be at high impedance. |
| 2 | SMOD# | Skip Mode 3-state input (see Table 1 Logic Table): 1. SMOD# = High: The zero cross comparator and the state of PWM determine if the module should perform Zero Cross Detection. 2. SMOD# = Mid: Connects PWM to internal resistor divider placing a bias voltage on an undriven PWM pin. Otherwise, logic is equivalent to SMOD# in the high state. 3. SMOD# = Low: Placing PWM into Tri-State pulls the High-Side and Low-Side MOSFET gates low without delay. There is an internal pull-up resistor to VCC on this pin. |
| 3 | VCC | 5V Bias for Internal Logic Blocks. Ensure the position a 1 μ F MLCC directly between VCC and AGND (Pin 4). |
| 4 | AGND | Signal Ground. |
| 5 | BOOT | High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7). |
| 6 | NC | Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN. |
| 7 | PHASE | This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5). |
| 8, 9, 10, 11 | VIN | Power stage High Voltage Input (Drain connection of High-Side MOSFET). |
| 12, 13, 14, 15 | PGND | Power Ground pin for power stage (Source connection of Low-Side MOSFET). |
| 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26 | VSWH | Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal. |
| 27 | GL | Low-Side MOSFET Gate connection. This is for test purposes only. |
| 28 | PGND | Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1 μ F directly between PGND and PVCC (Pin 29). |
| 29 | PVCC | 5V Power Rail for High-Side and Low-Side MOSFET Drivers. Ensure to position a 1 μ F MLCC directly between PVCC and PGND (Pin 28). |
| 30 | DISB# | Output disable pin. When this pin is pulled to a logic low level, the IC is disabled. There is an internal pull-down resistor to AGND. |
| 31 | THWN | Thermal warning indicator. This is an open-drain output. When the temperature at the driver IC die reaches the Over Temperature Threshold, this pin is pulled low. |

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

| Parameter | Rating |
|---|----------------------------|
| Low Voltage Supply (VCC, PVCC) | -0.3V to 6.5V |
| High Voltage Supply (VIN) | -0.3V to 30V |
| Control Inputs (PWM, SMOD#, DISB#) | -0.3V to (VCC+0.3V) |
| Output (THWN) | -0.3V to (VCC+0.3V) |
| Bootstrap Voltage DC (BOOT-PGND) | -0.3V to 35V |
| Bootstrap Voltage Transient ⁽¹⁾ (BOOT-PGND) | -8V to 40V |
| Bootstrap Voltage DC (BOOT-PHASE/VSWH) | -0.3V to 6.5V |
| BOOT Voltage Transient ⁽¹⁾ (BOOT-PHASE/VSWH) | -0.3V to 9V |
| Switch Node Voltage DC (PHASE/VSWH) | -0.3V to 30V |
| Switch Node Voltage Transient ⁽¹⁾ (PHASE/VSWH) | -8V to 38V |
| Low-Side Gate Voltage DC (GL) | (PGND-0.3V) to (PVCC+0.3V) |
| Low-Side Gate Voltage Transient ⁽¹⁾ (GL) | (PGND-2.5V) to (PVCC+0.3V) |
| VSWH Current DC | 65A |
| VSWH Current 10ms Pulse | 80A |
| VSWH Current 10us Pulse | 120A |
| Storage Temperature (T _S) | -65°C to 150°C |
| Max Junction Temperature (T _J) | 150°C |
| ESD Rating ⁽²⁾ | 1.5kV |

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5Ω in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

| Parameter | Rating |
|--|----------------|
| High Voltage Supply (VIN) | 4.5V to 25V |
| Low Voltage / MOSFET Driver Supply (VCC, PVCC) | 4.5V to 5.5V |
| Control Inputs (PWM, SMOD#, DISB#) | 0V to VCC |
| Operating Frequency | 200kHz to 2MHz |

Electrical Characteristics⁽³⁾

$T_J = 0^{\circ}\text{C}$ to 150°C , $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $PVCC = VCC = DISB\# = 5\text{V}$, unless otherwise specified. Min/Max values are guaranteed by test, design or statistical correlation.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------------------|---------------------------------------|---|------|------|------|-------------------------------|
| GENERAL | | | | | | |
| V_{IN} | Power Stage Power Supply | | 4.5 | | 25 | V |
| V_{CC} | Low Voltage Bias Supply | $PVCC = VCC$ | 4.5 | | 5.5 | V |
| $R_{\theta JC}^{(4)}$ | Thermal Resistance | Reference to High-Side MOSFET temperature rise | | 2.5 | | $^{\circ}\text{C} / \text{W}$ |
| $R_{\theta JA}^{(4)}$ | | Freq = 300kHz. AOS Demo Board. | | 12.5 | | $^{\circ}\text{C} / \text{W}$ |
| INPUT SUPPLY AND UVLO | | | | | | |
| V_{CC_UVLO} | Undervoltage LockOut | VCC Rising | | 3.1 | 3.3 | V |
| V_{CC_HYST} | | VCC Hysteresis | | 400 | | mV |
| I_{VCC} | Control Circuit Shutdown Bias Current | $DISB\# = 0\text{V}$, $SMOD\# = 5\text{V}$ | | 0.1 | 1 | μA |
| | | $DISB\# = 0\text{V}$, $SMOD\# = 0\text{V}$ | | 6 | 13 | μA |
| I_{PVCC} | Drive Circuit Operating Current | PWM = 400kHz, 20% Duty Cycle | | 17.5 | | mA |
| PWM INPUT | | | | | | |
| V_{PWMH} | Logic High Input Voltage | | 2.65 | | | V |
| V_{PWML} | Logic Low Input Voltage | | | | 0.7 | V |
| R_{PWM} | PWM Pin Input Resistance | $SMOD\# = 0\text{V}$ or 5V | 10 | | | $\text{M}\Omega$ |
| | | $SMOD\# = 1.7\text{V}$ | | 200 | | $\text{k}\Omega$ |
| V_{TRI} | PWM Tri-State Window | | 1.4 | | 2.0 | V |
| V_{PWM_FLOAT} | PWM Tri-State Voltage Clamp | $SMOD\# = 1.7\text{V}$ | | 1.7 | | V |
| DISB# INPUT | | | | | | |
| $V_{DISB\#_ON}$ | Enable Input Voltage | | 2.0 | | | V |
| $V_{DISB\#_OFF}$ | Disable Input Voltage | | | | 0.8 | V |
| $R_{DISB\#}$ | DISB# Input Resistance | Pull-Down Resistor | | 475 | | $\text{k}\Omega$ |
| t_{EN_DEL} | Enable Delay Time | $DISB\#$: L \rightarrow H, $V_{SWH} = \text{PWM}$ | | | 40 | μs |
| t_{DIS_DEL} | Disable Delay Time | $DISB\#$: H \rightarrow L, $V_{SWH} = \text{Floating}$ | | 21 | 50 | ns |
| SMOD# INPUT | | | | | | |
| $V_{SMOD\#_H}$ | Logic High Input Voltage | | 2.65 | | | V |
| $V_{SMOD\#_L}$ | Logic Low Input Voltage | | | | 0.7 | V |
| $V_{SMOD\#_MID}$ | Logic Mid-State Input Voltage | | 1.4 | | 2.0 | V |
| $R_{SMOD\#}$ | SMOD# Input Resistance | Pull-Up Resistor | | 475 | | $\text{k}\Omega$ |
| $t_{SMOD\#_DEL}$ | SMOD# Propagation Delay Time | | | | 40 | ns |
| ZCD FUNCTION | | | | | | |
| V_{ZCD} | Zero Cross Detect Voltage | | | -6 | | mV |
| t_{ZCD_BLANK} | ZCD Blanking Time | $SMOD\# = 5\text{V}$ | | 300 | | ns |

Electrical Characteristics⁽³⁾

$T_J = 0^\circ\text{C}$ to 150°C , $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $PVCC = VCC = DISB\# = 5\text{V}$, unless otherwise specified. Min/Max values are guaranteed by test, design or statistical correlation.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------------------------|--|------|------|------|------------------|
| GATE DRIVER TIMINGS | | | | | | |
| t_{PDLU} | PWM to High-Side Gate | PWM: H \rightarrow L, GH ⁽⁵⁾ : H \rightarrow L | | 13 | | ns |
| t_{PDLL} | PWM to Low-Side Gate | PWM: L \rightarrow H, GL: H \rightarrow L | | 15 | | ns |
| t_{PDHU} | LS to HS Gate Deadtime | GL: H \rightarrow L, GH ⁽⁵⁾ : L \rightarrow H | | 13 | | ns |
| t_{PDHL} | HS to LS Gate Deadtime | VSWH: H \rightarrow 1V, GL: L \rightarrow H | | 12 | | ns |
| t_{TSEXIT} | Tri-State Propagation Delay | PWM: $V_{TRI} \rightarrow$ H, VSWH: L \rightarrow H PWM: $V_{TRI} \rightarrow$ L, GL: L \rightarrow H | | 13 | 25 | ns |
| THERMAL NOTIFICATION | | | | | | |
| T_{JTHWN} | Junction Thermal Threshold | Temperature Rising | | 150 | | $^\circ\text{C}$ |
| T_{JHYST} | Junction Thermal Hysteresis | | | 15 | | $^\circ\text{C}$ |
| I_{THWN} | THWN Open Drain Current | | | | 5 | mA |
| THERMAL SHUTDOWN | | | | | | |
| T_{JTHDN} | Junction Thermal Threshold | Temperature Rising | | 180 | | $^\circ\text{C}$ |
| T_{JTHDN_HYS} | Junction Thermal Hysteresis | | | 25 | | $^\circ\text{C}$ |

Notes:

3. All voltages are specified with respect to the corresponding AGND pin.
4. Characterization value. Not tested in production.
5. GH is an internal pin.

Logic Table and Timing Diagrams

Table 1: Input Control Truth Table

| DISB# | SMOD# ⁽⁶⁾ | PWM ⁽¹⁾ | GH (Not a Pin) | GL |
|-------|----------------------|--------------------|----------------|--------------------|
| L | X | X | L | L |
| H | X | H | H | L |
| H | X | L | L | H |
| H | Tri-State | Tri-State | L | ZCD ⁽⁷⁾ |
| H | H | Tri-State | L | ZCD ⁽⁷⁾ |
| H | L | Tri-State | L | L ⁽⁸⁾ |

Notes:

- 6. PWM input is driven to Tri-State with internal divider resistors when SMOD# is driven to Tri-State and PWM input is not driven externally.
- 7. GL goes low following 80 ns de-bounce time, 220 ns blanking time and then VSWH exceeding ZCD threshold.
- 8. There is no delay before GL goes low.

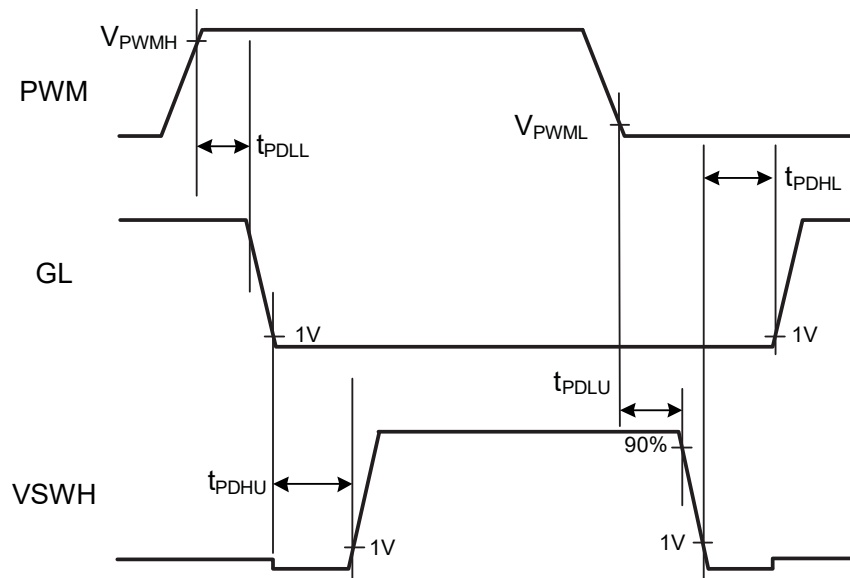


Figure 1. PWM Logic Input Timing Diagram

Logic Table and Timing Diagrams (Continued)

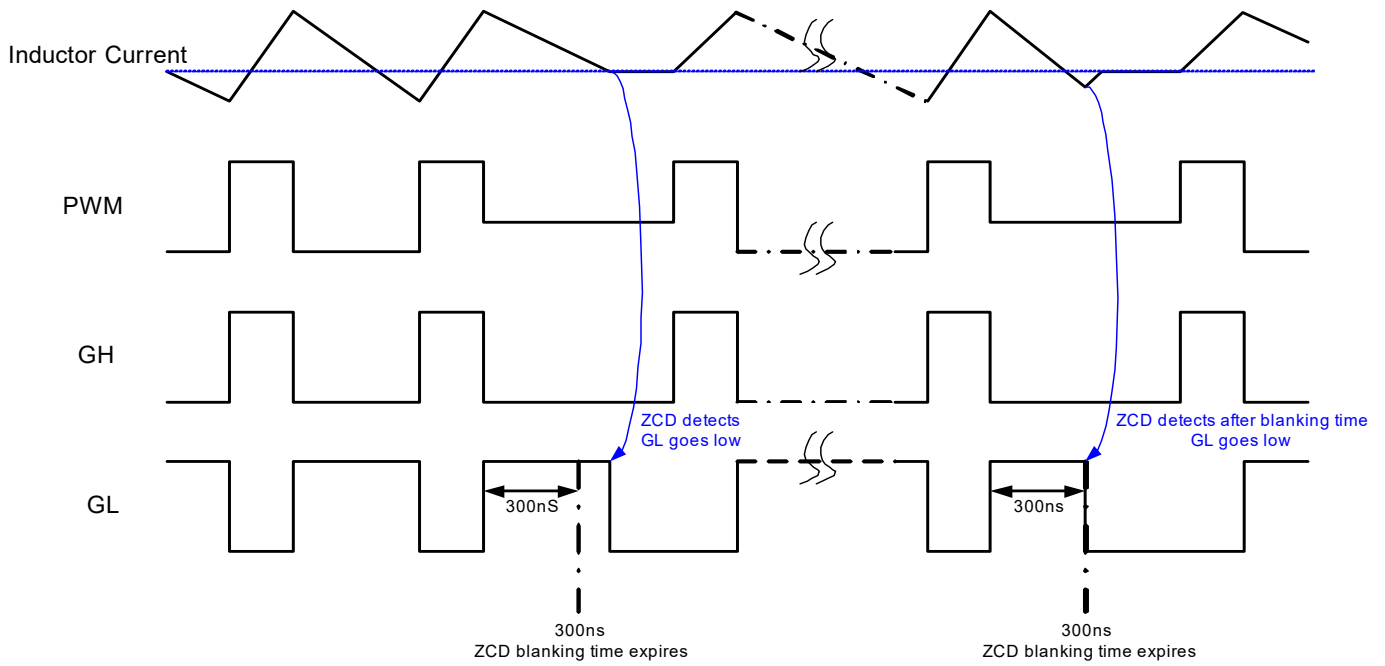


Figure 2. PWM Tri-State Input Logic Timing Diagram, SMOD# = 5V

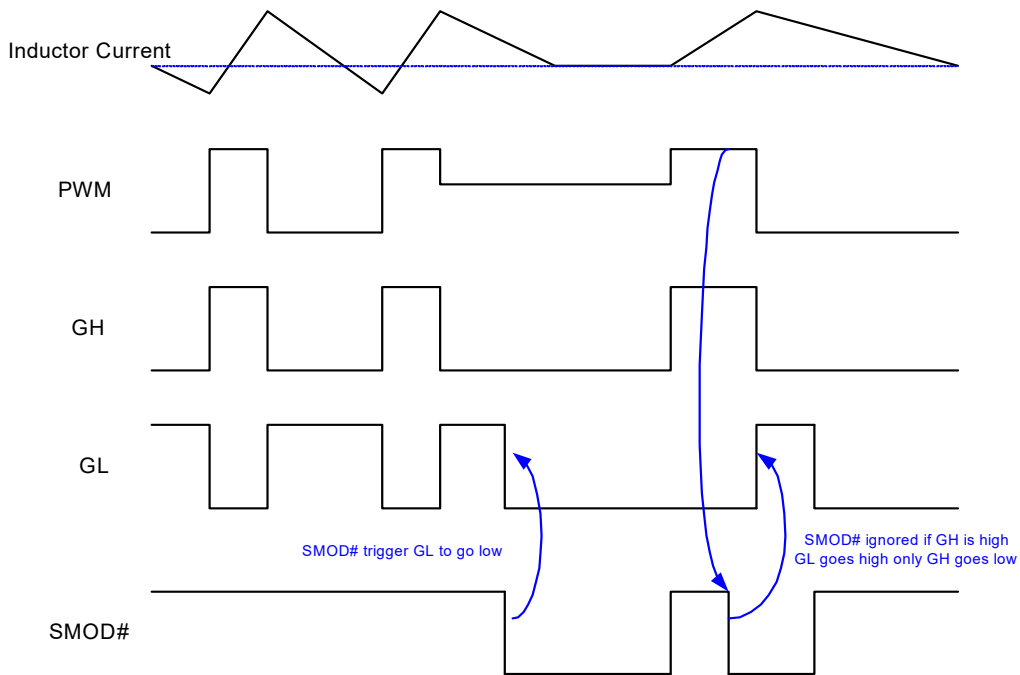


Figure 3. SMOD# Logic Timing Diagram

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $PV_{CC} = V_{CC} = \text{DISB}\# = 5\text{V}$, unless otherwise specified.

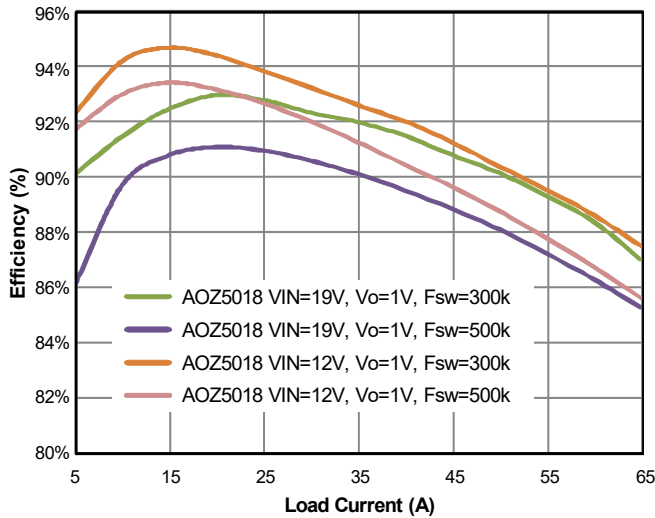


Figure 4. Efficiency vs. Load Current

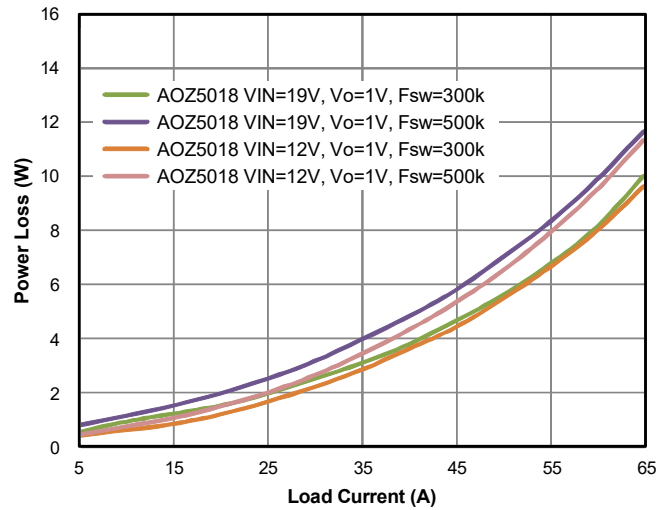


Figure 5. Power Loss vs. Load Current

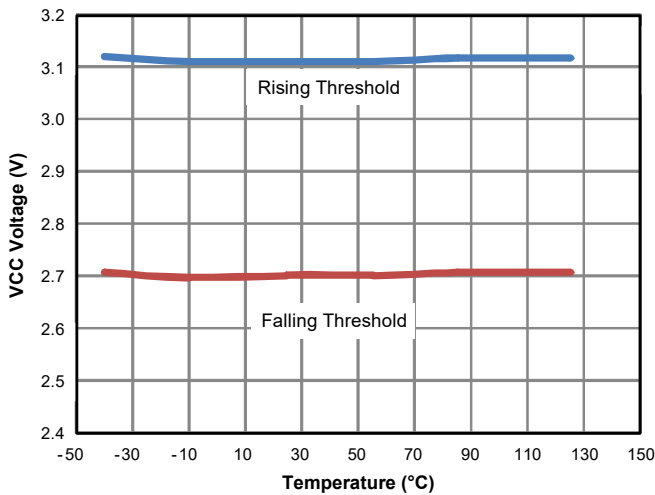


Figure 6. VCC Threshold vs. Temperature

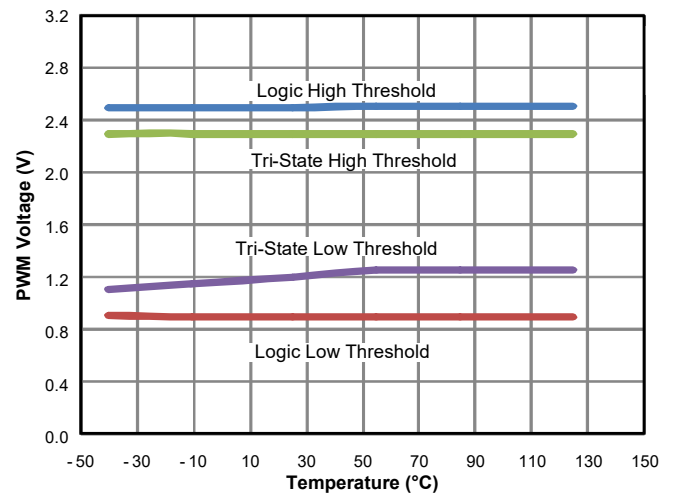


Figure 7. PWM Threshold vs. Temperature

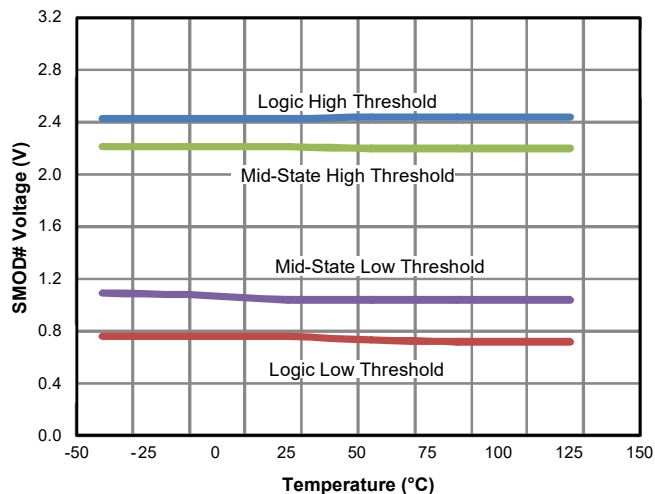


Figure 8. SMOD# vs. Temperature

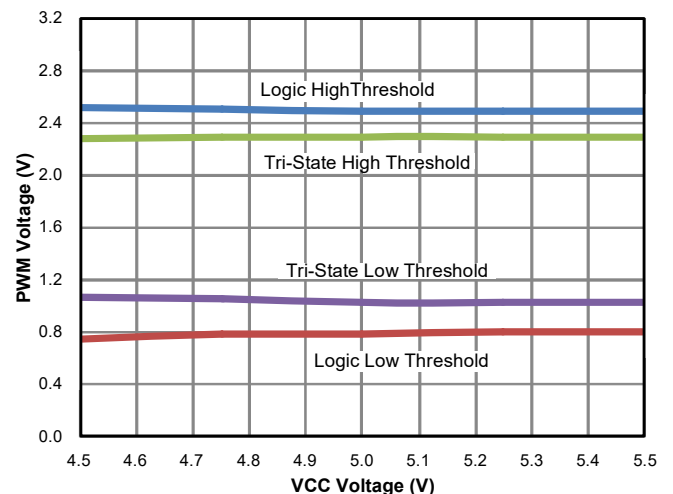


Figure 9. PWM Threshold vs. VCC Voltage

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $PVCC = VCC = DISB\# = 5\text{V}$, unless otherwise specified.

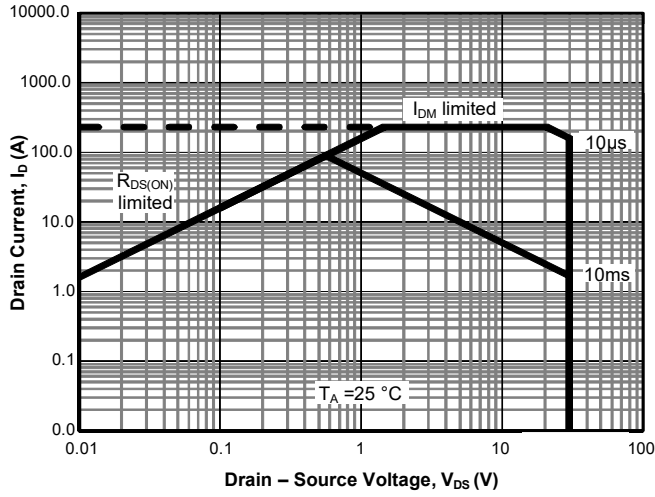


Figure 10. High-Side MOSFET SOA

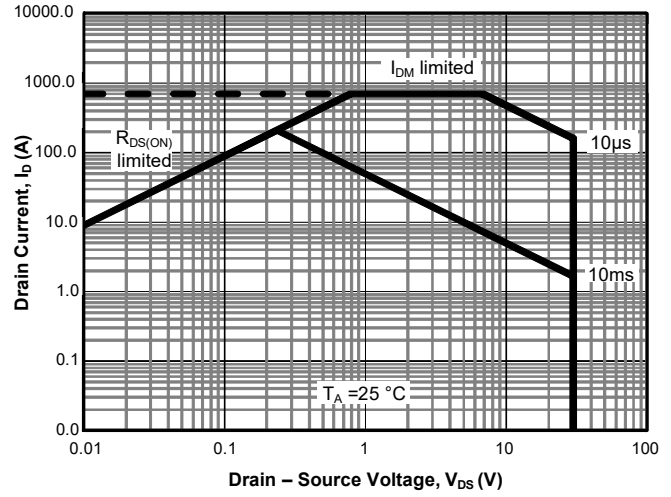


Figure 11. Low-Side MOSFET SOA

Application Information

AOZ5118QI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on both High-Side and Low-Side for a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Powering the Module and the Gate Drives

An external supply $PVCC = 5V$ is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate threshold voltages to achieve the most advantageous compromise between high switching speed and minimal power loss. The integrated gate driver is capable of supplying large peak current into the Low-Side MOSFET to achieve fast switching. A ceramic bypass capacitor of $1\mu F$ or higher is recommended from $PVCC$ (Pin 29) to $PGND$ (Pin 28). The control logic supply VCC (Pin 3) can be derived from the gate drive supply $PVCC$ (Pin 29) through an RC filter to bypass the switching noise (See Typical Application Circuit).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between the $BOOT$ (Pin 5) and the switching node $PHASE$ (Pin 7). It is recommended that this capacitor C_{BOOT} should be connected to the device across Pin 5 and Pin 7 as closely as possible. A bootstrap switch is integrated into the device to reduce external component count. An optional resistor R_{BOOT} in series with C_{BOOT} between 1Ω to 5Ω can be used to slow down the turn on speed of the High-Side MOSFET to achieve both short switching time and low V_{SWH} switching node spikes at the same time.

Under-voltage LockOut

AOZ5118QI starts up to normal operation when VCC rises above the Under-Voltage LockOut (UVLO) threshold voltage. The UVLO release is set at 3.1V typically. Since the PWM control signal is provided from an external controller or a digital processor, extra caution must be taken during start up. AOZ5118QI must be powered up before PWM input is applied.

Normal system operation begins with a soft start sequence by the controller to minimize in-rush current during start-up. Powering the module with a full duty cycle PWM signal may lead to many undesirable consequences due to excessive power. AOZ5118QI provides some protections such as UVLO and thermal monitor. For system level protection, the PWM controller should monitor the current output and protect the load under all possible operating and transient conditions.

Disable (DISB#) Function

The AOZ5118QI can be enabled and disabled through $DISB\#$ (Pin 30). The driver output is disabled when $DISB\#$ input is connected to $AGND$. The module would be in standby mode with low quiescent current of less than $1\mu A$. The module will be active when $DISB\#$ is connected to VCC Supply. The driver output will follow PWM input signal. A weak pull-down resistor is connected between $DISB\#$ and $AGND$.

Power up sequence design must be implemented to ensure proper coordination between the module and external PWM controller for soft start and system enable/disable. It is recommended that the AOZ5118QI should be disabled before the PWM controller is disabled. This would ensure AOZ5118QI will be operating under the recommended conditions.

Input Voltage V_{IN}

AOZ5118QI is rated to operate over a wide input range from 4.5V to 25V. For high current synchronous buck converter applications, large pulse current at high frequency and high current slew rates (di/dt) will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor very close to the package leads at the input supply (V_{IN}). Both X7R or X5R quality surface mount ceramic capacitors are suitable.

The High-Side MOSFET is optimized for fast switching by using a low gate charge (Q_G) device. When the module is operated at high duty cycle ratio, conduction loss from the High-Side MOSFET will be higher. The total power loss for the module is still relatively low but the High-Side MOSFET higher conduction loss may have higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. It is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure that they are operating within Safe Operating Area (SOA).

PWM Input

AOZ5118QI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected, both High-Side and Low-Side MOSFETs are turned off and V_{SWH} is in high impedance state. Table 2 shows the thresholds level for high-to-low and low-to-high transitions as well as Tri-State window.

There is a Holdoff Delay between the corresponding PWM Tri-State signal and the MOSFET gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches. The Holdoff Delay is typically 330ns.

Table 2: PWM Input and Tri-State Thresholds

| Thresholds → | V _{PWMH} | V _{PWML} | V _{TRIH} | V _{TRIL} |
|--------------|-------------------|-------------------|-------------------|-------------------|
| AOZ5118QI | 2.65V | 0.70V | 1.40V | 2.00V |

Note: See Figure 2 for propagation delays and Tri-State window.

Diode Mode Emulation of Low-Side MOSFET (SMOD#)

AOZ5118QI can be operated in the diode emulation or pulse skipping mode using SMOD# (Pin 2). This enables the converter to operate in asynchronous mode during start up, light load, or under pre-bias conditions.

When SMOD# is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction. When PWM input is at Tri-State level, the driver logic will enter ZCD mode to turn off Low-Side MOSFET if load current crosses zero level.

Table 3: Logic Table when SMOD# = High

| PWM | SMOD# | GH | GL |
|-----------|-------|----|-----|
| H | H | H | L |
| Tri-State | H | L | ZCD |
| L | H | L | H |

When SMOD# is low, the module can operate in Discontinuous Conduction Mode (DCM). The High-Side MOSFET gate drive output is not affected but Low-Side MOSFET will enter diode emulation mode. The Low-Side MOSFET signal is dependent on the PWM signal level and not responding to ZCD signal. Side MOSFET signal is dependent on the PWM signal level and not responding to ZCD signal.

Table 4: Logic Table when SMOD# = Low

| PWM | SMOD# | GH | GL |
|-----------|-------|----|----|
| H | H | H | L |
| Tri-State | H | L | L |
| L | H | L | H |

Gate Drives

AOZ5118QI has an internal high current high speed driver that generates the floating gate driver for the High-Side MOSFET and a complementary driver for the Low-Side MOSFET. An internal shoot through protection scheme is implemented to ensure that both MOSFETs cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

1) PWM from logic Low to logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

2) PWM from logic High to logic Low

When the falling edge of switching node VSWH goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on.

This mechanism prevents cross conduction across the input bus line VIN and PGND. The anti-overlap circuit monitors the switching node VSWH to ensure a smooth transition between the two MOSFETs under any load transient conditions.

Thermal Warning (THWN)

The driver IC temperature is internally monitored and a thermal warning flag at THWN (Pin 31) is asserted if it exceeds 150°C. This warning flag is reset when the temperature drops back to 120°C. THWN is an open drain output that is pulled to AGND to indicate an over-temperature condition. It should be connected to VCC through a resistor for monitoring purposes. The device will not power down during the over-temperature condition.

PCB Layout Guidelines

AOZ5118QI is a high current module rated for operation up to 2MHz. This requires high switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor C_{IN} . The PCB design is greatly simplified by the optimization of the AOZ5118QI pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors C_{IN} should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor L1, and output capacitor C_{OUT} is the next critical requirement. This requires second layer or "Inner 1" to be the PGND plane. VIAs should then be placed near PGND pads.

While AOZ5118QI is a highly efficient module, it still dissipates a significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

As shown on Figure 12, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop which runs along VIN pad originating from the input capacitors C10, C11, and C12 that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

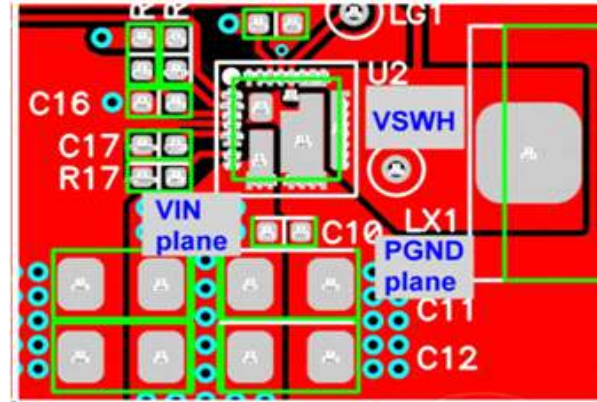


Figure 12. Top Layer of Demo Board, VIN, VSWH and PGND Copper Pads

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spikes appear at the VSWH terminal which are caused by the large internal di/dt produced by the package parasitic. To minimize the effects of this interference at the VSWH terminal, at which the main inductor L1 is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this VSWH terminal, only enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers. Refer to Figure 13.

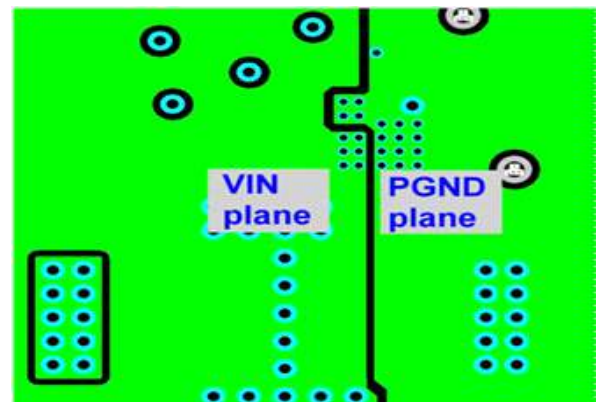


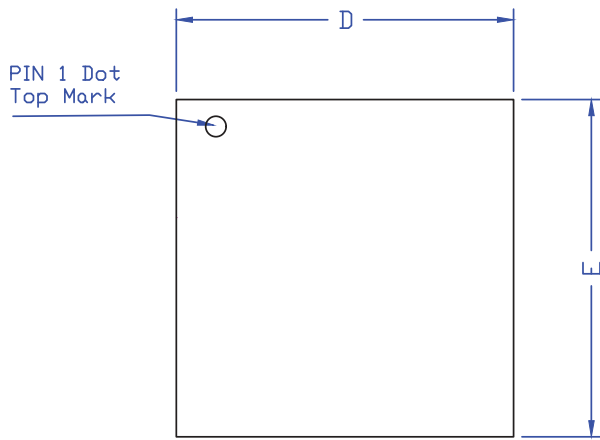
Figure 13. Bottom layer of PCB

Positioning VIAs through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build-up and spread the heat much more quickly

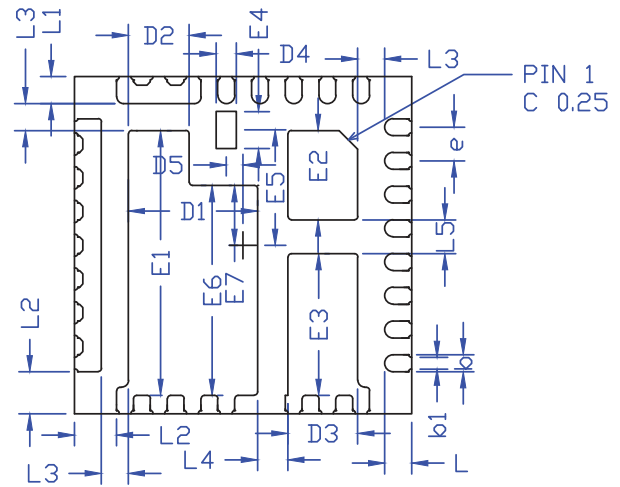
towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter VIAs. 10mil diameter is a commonly used VIA diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in case of solder overflow, which could potentially short with the adjacent exposed thermal pad.

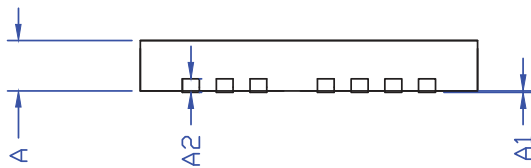
Package Dimensions, QFN5x5-31L



TOP VIEW

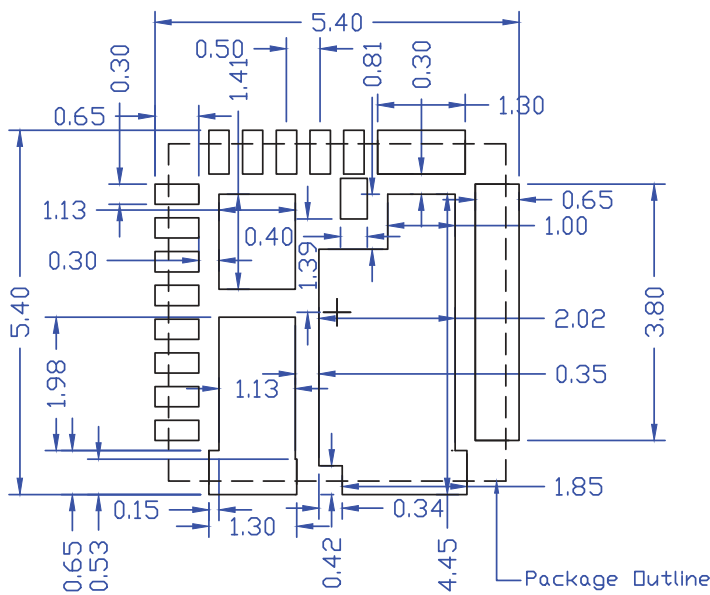


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



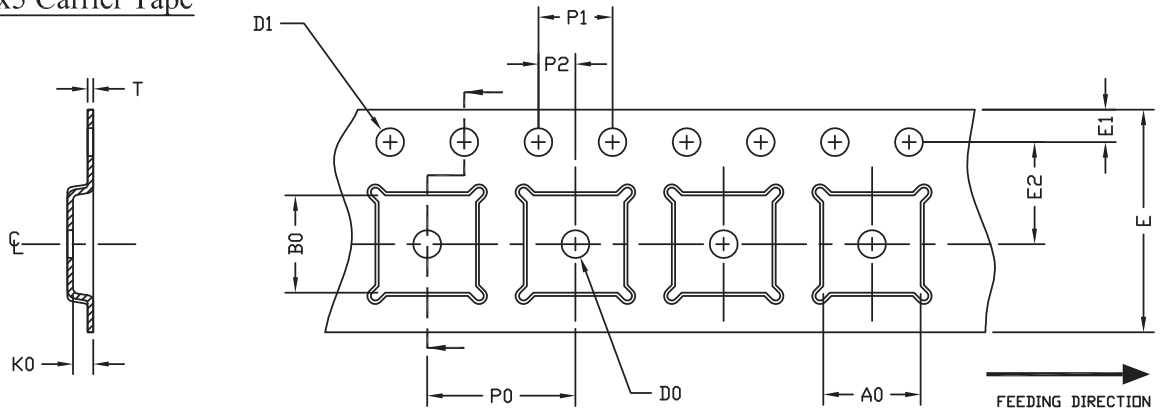
UNIT: mm

| SYMBOLS | DIMENSION IN MM | | | DIMENSION IN INCHES | | |
|---------|-----------------|------|------|---------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| A2 | 0.20REF | | | 0.008REF | | |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| D1 | 1.87 | 1.92 | 1.97 | 0.074 | 0.076 | 0.078 |
| D2 | 0.85 | 0.90 | 0.95 | 0.033 | 0.035 | 0.037 |
| D3 | 0.99 | 1.04 | 1.09 | 0.039 | 0.041 | 0.043 |
| D4 | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| D5 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| E1 | 3.88 | 3.93 | 3.98 | 0.153 | 0.155 | 0.156 |
| E2 | 1.27 | 1.32 | 1.37 | 0.050 | 0.052 | 0.054 |
| E3 | 2.05 | 2.10 | 2.15 | 0.081 | 0.083 | 0.085 |
| E4 | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| E5 | 1.66 | 1.71 | 1.76 | 0.065 | 0.067 | 0.069 |
| E6 | 3.06 | 3.11 | 3.16 | 0.121 | 0.122 | 0.124 |
| E7 | 0.84 | 0.89 | 0.94 | 0.033 | 0.035 | 0.037 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L1 | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L2 | 0.58 | 0.63 | 0.68 | 0.023 | 0.025 | 0.027 |
| L3 | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L4 | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| L5 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| b1 | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| e | 0.50BSC | | | 0.020BSC | | |

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Drawing, QFN5x5A-31L

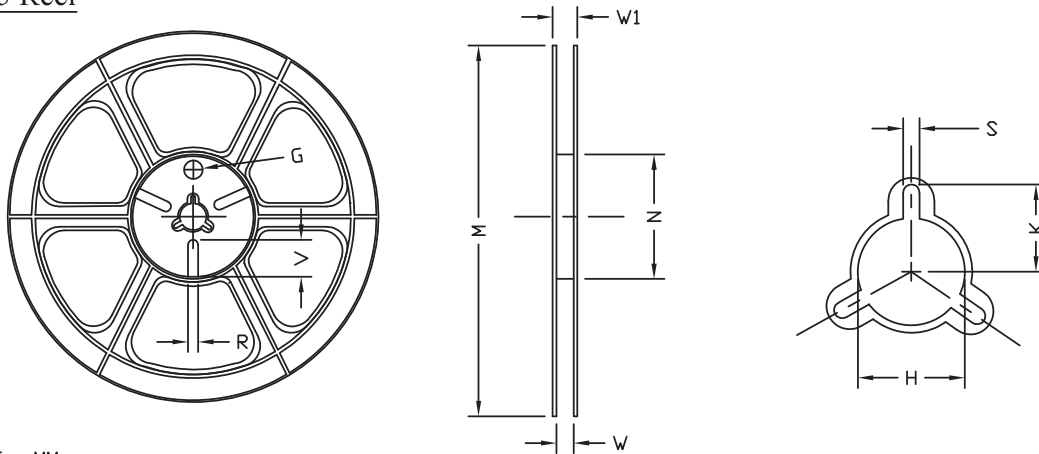
QFN5x5 Carrier Tape



UNIT: MM

| PACKAGE | A0 | B0 | K0 | D0 | D1 | E | E1 | E2 | P0 | P1 | P2 | T |
|-------------------|---------------|---------------|---------------|--------------|---|--------------|---------------|---------------|---------------|---------------|---------------|---------------|
| QFN5x5 (12 mm) | 5.25 ±0.10 | 5.25 ±0.10 | 1.10 ±0.10 | 1.50 MIN. | 1.50 ^{+0.1} _{-0.0} | 12.0 ±0.3 | 1.75 ±0.10 | 5.50 ±0.05 | 8.00 ±0.10 | 4.00 ±0.10 | 2.00 ±0.05 | 0.30 ±0.05 |

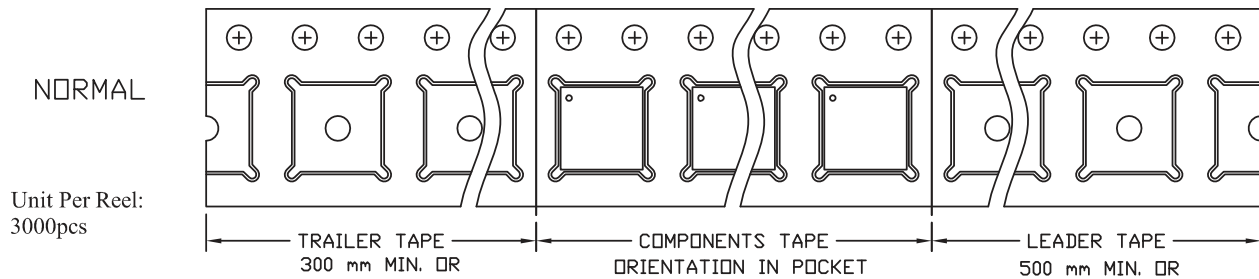
QFN5x5 Reel



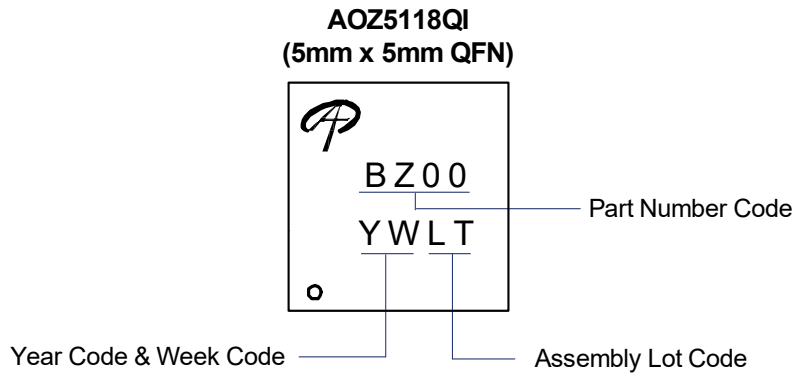
UNIT: MM

| TAPE SIZE | REEL SIZE | M | N | W | W1 | H | K | S | G | R | V |
|-----------|-----------|----------------|---------------|---|---|---------------|--------------|-------------|-----|-----|-----|
| 12 mm | ø330 | ø330.0 ±2.0 | ø79.0 ±1.0 | 12.4 ^{+2.0} _{-0.0} | 17.0 ^{+2.6} _{-1.2} | ø13.0 ±0.5 | 10.5 ±0.2 | 2.0 ±0.5 | --- | --- | --- |

Leader / Trailer
& Orientation



Part Marking



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- | | |
|---|---|
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|---|---|