Comparison Between CY62256NLL-70 and AS6C62256-55 256Kb LP-SRAMs

Part number	CY62256NLL-70SNXC CY62256NLL-70SNXCT CY62256NLL-70PXC	AS6C62256-55SCN AS6C62256-55SCNTR AS6C62256-55PCN	**Comparison result**
Power supply	4.5V – 5.5V	2.7V – 5.5V	Alliance Memory offers a wider voltage range, which covers the range for the Cypress parts
Typical power dissipation under normal operation	Speed: 70ns Average operating power supply current Icc = 50mA (max.) Icc = 25mA (typ.) Standby power (µA) Supply current -TTL inputs ISB1 = 0.5mA (max.) ISB1 = 0.3mA (typ.) -CMOS inputs ISB2 = 5µA (max., C temp.) ISB2 = 10µA (max., I temp.) ISB2 = 0.1µA (typ. C/I temp)	Speed: 55ns Average operating power supply current Icc = 45mA (max.) Icc = 15mA (typ.) Icc1 = 10mA (max.) Icc1 = 3mA (typ.) Standby power (µA) Supply current -TTL inputs ISB = 3mA (max.) ISB = 1mA (typ.) ISB1 = 30µA (max., I temp.) ISB1 = 15µA (max., C temp.) ISB1 = 1µA (typ., C/I temp.)	The AS6C62256-55's faster speed covers the Cypress parts, and there is a supply current difference
Operating temperature	Industrial: -40℃ to +85℃ Commercial: 0℃ to +70℃	Industrial: -40℃ to +85℃ Commercial: 0℃ to +70℃	Same
Max. operating speed	70ns	55ns	Same
Interface (input/output) capacitance	Input capacitance CIN: <6pF Output capacitance CO: <8pF	Input capacitance CIN: <6pF Output capacitance CO: <8pF	Same
Interface definition	Omit (see datasheet)	Omit (see datasheet)	Same. They are pin-to-pin compatible
Timing parameters	Refer to "Annex 1"	Refer to "Annex 1"	Compatible
Timing diagram and command	Omit (see datasheet)	Omit (see datasheet)	Same
Capacity	256Kb	256Kb	Same
Package	28-pin, 300-mil SOP 28-pin, 600-mil PDIP	28-pin, 330-mil SOP 28-pin, 600 mil PDIP	They are pin-to-pin compatible.
Truth table	Omit (see datasheet)	Omit (see datasheet)	Same

Annex 1: Comparison Between the AC Electrical Characteristics of the CY62256NLL-70 and AS6C62256-55

Read Cycle				
Parameter	**Symbol**	**CY62256NLL-70**	**AS6C62256-55**	**Unit**

		Min.	Max.	Min.	Max.	
Read cycle time	tRC	70	-	55	-	ns
Address access time	tAA	-	70	-	55	ns
Chip enable access time	tACE	-	70	-	55	ns
Output enable access time	tOE	-	35	-	30	ns
Chip enable to output in low-Z	tCLZ*	5	-	10	-	ns
Output enable to output in low-Z	tOLZ*	5	-	5	-	ns
Chip disable to output in high-Z	tCHZ*	-	25	-	20	ns
Output disable to output in high-Z	tOHZ*	-	25	-	20	ns
Output hold from address change	tOH	5	-	10	-	ns
Write Cycle						
Parameter	**Symbol**	**CY62256NLL-70**		**AS6C62256-55**		**Unit**
		Min.	**Max.**	**Min.**	**Max.**	
Write cycle time	tWC	70	-	55	-	ns
Address valid to end of write	tAW	60	-	50	-	ns
Chip enable to end of write	tCW	60	-	50	-	ns
Address set-up time	tAS	0	-	0	-	ns
Write pulse width	tWP	50	-	45	-	ns
Write recovery time	tWR	0	-	0	-	ns
Data to write time overlap	tDW	30	-	25	-	ns
Data hold from end of write time	tDH	0	-	0	-	ns
Output active from end of write	tOW*	5	-	5	-	ns
Write to output in high-Z	tWHZ*	-	25	-	20	ns